

494/494P

SPECTRUM ANALYZER

OPTIONS INCLUDED
VOLUME 1

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

*Please Check for
CHANGE INFORMATION
at the Rear of This Manual*

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SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Do Not Wear Jewelry

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages and currents.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

X-Radiation

X-ray emission generated within this instrument has been sufficiently shielded. Do not modify or otherwise alter the high voltage circuitry or the CRT enclosure.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual



This symbol indicates where applicable cautionary or other information is to be found.

As Marked On Equipment



DANGER—High Voltage.



Protective ground (earth) terminal.



ATTENTION—Refer to manual.



Refer to manual.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors, see the General Information and Specifications section in Volume 1 of the 494/494P Service manual.

Refer cord and connector changes to qualified service personnel.

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The 494P Spectrum Analyzer.

GENERAL INFORMATION

INTRODUCTION

The service instructions for this product consists of two volumes. Volume 1 contains the written information such as specifications, maintenance, and calibration. Volume 2 contains the diagrams and parts lists. Our intent is to provide both accurate and complete information for this product. The Table of Contents, at the beginning of this manual, lists the location and contents of each section that make up the two volume service manuals.

Change information that involves manual corrections and/or additions, pending manual reprint and bind, is located at the back of each service manual as a CHANGE INFORMATION section.

History

History information, with the updated data, is integrated into the text or diagrams. When a page is updated, the revised pages are identified by a revision date in the lower inside corner of the page. When a diagram is updated, the revision date is placed at the lower center of the diagram. History information is indicated with a gray tint. When a component value is changed, the designator on the drawing is boxed with a grey outline. When a circuit is deleted or changed, the original configuration is shown in grey, drawn either at its original location or to the side of the drawing. If you have a manual other than the one that came with your instrument it may contain revisions that do not apply to your instrument; however all history information that pertains to the earlier instruments is retained.

When a major modification has been made to an assembly or circuit board, the data for the replaced assembly will follow the new information and will be identified with appropriate titles or headings; such as instrument serial number range, or the assembly or board part numbers.

Level of Competence

It is assumed that whoever uses these instructions is familiar with basic digital, analog, and RF circuitry. Circuit analysis is mostly functional and should provide the technician with the information necessary to isolate the majority of malfunctions to a board or block of circuitry. The technician

should then be able, with the aid of test equipment, to isolate the malfunction to a specific component or components.

This instrument contains internal firmware which provides a complete instrument check during power up and during operation, and if needed, guides the user through a front panel calibration procedure. If calibration cannot be achieved, a diagnostic test detects and isolates most problems to the system, such as 1st LO. The technician can then run trouble shooting diagnostic to further isolate the problem to the board or in some cases to the IC level. Refer to the Diagnostic part of the Maintenance section.

Standards and Conventions Used

Most terminology is in accordance with those standards adapted by IEEE and IEC. A glossary of terms is provided as an appendix. Abbreviations in the documentation are in accordance with ANSI Y1.1-1972, with exceptions and additions explained in parentheses after the abbreviation. Graphic symbols comply with ANSI Y32.2-1975. Logic symbology is based on ANSI Y32.14-1973 and the manufacturer's data description. GPIB functions for the programmable version conforms to IEEE 488-1978 Standard. A copy of ANSI and IEEE standards may be obtained from, the Institute of Electrical and Electronic Engineers Inc., 345 East 47th Street, New York, N.Y. 10017.

Conformance to Industry Standards

The 494/494P complies with the following Industry Safety Standards and Regulatory Requirements:

Safety.

CSA—Electrical Bulletin

FM—Electrical Utilization Standard Class 3820

ANSI C39.5—Safety Requirements for Electrical and Electronic Measuring and Controlling Instrumentation.

IEC 348 (2nd addition)—Safety Requirements for Electronic Measuring Apparatus.

Regulatory Requirements

VDE 0871 Class B—Regulations for RFI Suppression of High Frequency Apparatus and Installations.

Product Description

The 494 and the 494P programmable instruments are high performance, compact, portable spectrum analyzers. Microcomputer control of most functions simplifies and enhances operation. Its features synthesizer frequency accuracy and stability, precision signal counting ability, precise amplitude measurement capability, digital storage display, battery-powered memory to retain front panel settings and displays, and crt message readout that describes function of the front panel controls and selectors along with messages that explain operating errors. Some of the options provide a second language for display messages, waveguide mixers to extend the frequency range to 325 GHz, rackmount and benchtop versions, and enhanced measurement capability for digital microwave radio.

The frequency range is 10 kHz to 21 GHz with the internal mixer, and up to 325 GHz when using external waveguide mixers. A minimum resolution bandwidth of 30 Hz, with a minimum span of 50 Hz/div, provides measurement resolution that is commensurate with the frequency accuracy. Digital storage provides flicker free displays plus functions such as SAVE A, B—SAVE A, MAX HOLD with which to compare and subtract displays, save maximum values. In addition to the conventional digital storage feature, up to nine separate displays with their parameter readouts, can be stored in battery-powered memory, then later recalled for additional analysis and comparison. Up to ten different front-panel control setups can also be stored for future recall.

Center frequency may be selected by means of the front-panel tuning knob or directly entered via the Data Entry keyboard. When using the keyboard, it is not necessary to alter the Span/Div setting regardless of the frequency selected. Other parameters, such as vertical display and reference level, may also be keyboard selected with the flexibility previously available only under GPIB program control. Counter accuracy to 1 Hz resolution is available.

In addition, the 494/494P requires only a short warm-up time for stable operation. In 15 minutes or less, the frequency drift is less than 500 Hz per minute of sweep time. After one hour, it is less than 50 Hz per minute of sweep time. Display dynamic range is 80 dB, with calibrated reference level readout from -117 dBm to $+30$ dBm, in selectable steps from 1 to 15 dB, and 0.25 dB for a ΔA (amplitude) mode. When the vertical display is selected with the Data Entry keyboard, the reference level steps correspond to the display mode (see Operating instructions). Sensitivity at 30 Hz resolution bandwidth is -121 dBm to 7.1 GHz, decreasing to -96 dBm at 21 GHz.

The 494P adds remote control capability to the standard instrument features of the 494. The front-panel controls (except those intended for local use, such as INTENSITY) can be remotely operated through the GPIB port, which allows the 494P to be used with a variety of systems and controllers. This operation is described in detail in the Programmers manual.

Product Service

To assure adequate product service and maintenance for our instruments, Tektronix has established Field Offices and Service Centers at strategic points throughout the United States and in countries where our products are sold. Several types of maintenance or repair agreements are available. For example; for a fixed fee, a maintenance agreement program provides maintenance and re calibration on a regular basis. Tektronix will remind you when a product is due for recalibration and perform the service within a specified time. Contact your local Service Center, representative, or sales engineer for details regarding: Warranty, Calibration, Emergency Repair, Repair Parts, Scheduled Maintenance, Maintenance Agreements, Pickup and Delivery, On-Site Service for fixed installations, and other services available through these centers.

Tektronix emergency repair service provides immediate attention to instrument malfunctions if you are in an emergency situation such as a field trip. Again, contact any Tektronix Service Center for assistance to get you on your way within a minimum of time.

Instrument Construction

The modular construction of the 494/494P instrument provides ready access to the major circuits. Circuit boards that contain sensitive circuits are either mounted on metal extrusions, each of which provides shielding between adjacent modules, or they are mounted within honeycomb-like extrusions, with feedthrough connectors through the wall of the compartment. All boards and assemblies plug onto a common mother board which provides the interconnection for these boards and assemblies. Most adjustments and test points are accessible while the instrument is operational and the modules or assemblies secured in their normal position. Extenders are provided with an optional Service Kit (see Maintenance section under Service Fixtures and Tools for Maintenance).

Any module or board can be removed without disturbing the structural or functional integrity of the other modules. The extenders allow most circuit board assemblies to function in an extended position for service or adjustment. The circuit boards mounted on the metal extrusion can be removed by removing the securing screws. All other circuit boards (which should require minimal service) are accessible by removing a cover plate over the assembly or module.

NOTE

Disassembly of some modules may require special tools and procedures. These procedures will be found in the Maintenance section.

To obtain and maintain the frequency stability, sensitivity, and EMI characteristics, circuits are completely RF isolated to ensure spurious free response; yet the close proximity minimizes losses or interactions with other functions. All compartments are enclosed on both sides by metal plates and all interconnections between compartments are made by feedthrough terminals rather than cables. If the compartments are opened, be sure that the shields and covers are properly reinstalled before operating.

Elapsed Time Meter

A 5000 hour elapsed time indicator, graduated in 500 hour increments, is installed on the Z Axis/RF Interface circuit board. This provides a convenient way to check operating time. The meter on new instruments may indicate from 200 to 300 hours elapsed time. Most instruments go through a factory burn-in time to improve reliability. This is similar to using aged components to improve reliability and operating stability.

Installation, Preparation for Use, and Repackaging

This section provides unpacking information and the procedures to prepare the instrument for use. It also includes repackaging information.

Changing Power Input Range

The procedure for changing the input voltage range is described under the Installation and Repackaging section.

The power cord that is supplied with the instrument and the instrument power voltage requirements depend on the available power source (see Specification section). Power cord options are described in the Installation and Preparation for Use section and the Options section.

Standard Accessories

Standard accessories for the 494/494P and rackmount/benchtop versions are listed in Table 1-1 and in Volume 2 of the Service Instructions, following the Replaceable Mechanical Parts list. The list in Volume 2 of the Service instructions provides part numbers for these accessories.

Options

Options for the 494/494P are described in the Options section of the manuals including rackmount/benchtop versions.

Optional Accessories

Optional accessories that play a significant role in the full operational applications and servicing of the 494/494P are referenced, where appropriate, throughout these instructions as well as the operating instructions.

Selected Components

Some components, such as microcircuits, are selected to meet Tektronix specifications. These components are indicated in the parts list and carry a Tektronix Part Number under the Mfr. Part Number column.

Selected value components that compensate for parameter differences between active components are identified on the circuit diagram and in the parts list as a "SEL" value. The component description lists either the nominal value or a range of value. If the procedure for selection is not obvious, such as setting the gain or response of a stage, the criteria for selection is explained in the Adjustment or Maintenance section of the manual.

Component Circuit Numbering Scheme

In this instrument, circuit numbers were assigned according to the physical location of the component on the board. For example, a resistor, located within row 2 column 08, is R2080. The fourth digit of the number is an expander used to designate two or more common components within a given grid, such as R2080, R2082, etc. Chassis mounted components are assigned a three digit number. This identifies these components from the board mounted components.

The Replaceable Electrical Parts list prefixes these circuit numbers with an assembly number. R2080 on assembly A20 becomes A20R2080. Assembly and subassembly numbers are assigned in numerical order by location within the instrument.

Firmware Version and Error Message Readout

This feature of the 492/492P provides readout of the firmware version when the power on/off is cycled. During initial power-up cycle, the firmware version flashes on screen for approximately two seconds. The Replaceable Electrical Parts list section, under Memory Board (A54), lists the ROM's and their Tektronix part number for each firmware version.

An additional feature is error message readout. When a routine fails, a message comes on screen describing the error and what can be done to bypass the problem if it can not be corrected.

Rackmount/Benchtop Versions

A rackmount version of the 492/492P Spectrum Analyzer is available to install the instrument in a standard 19 inch rack. The benchtop version is the same as the rackmount with the exception of the side rails. Complete information can be found in the Options section of this manual.

Replacing Fuses

Refer to the Installation and Preparation for Use section for line fuse replacement and the Maintenance section for replacing the power supply fuses.

Options For Power Cord Configuration

Tektronix has implemented options that provide internationally approved power cord and plug configurations. These are illustrated and described in Installation and Preparation for Use section and the Options section.

**Table 1-1
STANDARD ACCESSORIES**

Nomenclature	Qty.	Storage
50 Ω coax cable, N to N connector, 6 ft	1	Cover or Drawer
50 Ω coax cable, bnc to bnc connector, 18 inches	1	Cover or Drawer
Visor Crt	1	
Manual, Operators Handbook	1	Cover or Drawer
Manual, Operators	1	
Manual, Service Vol. 1	1	
Manual, Service Vol. 2	1	
Manual, Programmers (494P only)	1	
Adapter, N male to bnc female	1	Cover or Drawer
^a Fuses, 4A, Fast	2	Cover or Drawer
^a Power cord	1	
Cord clamp	1	
Crt Light Filter, Amber	1	Cover or Drawer
Crt Light Filter, Gray	1	Cover or Drawer
Crt Mesh Filter	1	Cover or Drawer
^b Diplexer Assembly	1	Cover or Drawer
1-Adapter, TNC to SMA	1	(Part of Diplexer Assembly)
1-Cable, semi-rigid coax	1	(Part of Diplexer Assembly)
Cable, GPIB Interconnect (494P only)	1	

^a The power cord (161-0104-00) and fuses are replaced with an appropriate power cord, for the international power cord options (A1, A2, A3, A4, and A5) and the fuses are replaced with 2A slow blow.

Option 52 (North American configuration for 220 V with standard power cord) also replaces fuses with 2A slow blow.

^bDeleted with Option 08

SPECIFICATION

Introduction

This section includes electrical, physical, environmental, and safety characteristics of this instrument. Changes to this specification, due to options are listed in the Options section.

ELECTRICAL CHARACTERISTICS

The following tables of electrical characteristics and features apply to the 494/494P Spectrum Analyzer after a 30-minute warmup, except as noted. The Performance Requirement column defines some characteristics in quantitative terms and in limit form. The Supplemental column explains performance requirements or provides performance information. Statements in this column are not considered to be guaranteed performance and are not ordinarily supported by a performance check procedure. Procedure to verify performance requirements are provided in the Performance section of the service manual.

The instrument microprocessor performs an internal calibration check each time power is turned on and verifies that the instrument frequency and amplitude performance is as specified. An operation or functional check procedure, which does not require external test equipment or technical expertise, is provided in the operators instructions to satisfy most incoming inspections and help familiarize the operator with the capabilities of the instrument.

Verification of Tolerance Values

Compliance tests of specified limits, listed in the Performance Requirement column, shall be performed after sufficient warmup time and preliminary preparation (such as front panel adjustments). Measurement shall be made by instruments that do not affect the values measured. Measurement tolerance of test equipment should be negligible in comparison to the specified tolerance and when not negligible, the error of the measuring device shall be added to the tolerance specified.

Table 2-1
FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Center Frequency Range (internal mixer)		10 kHz to 21 GHz. Tuned by the front panel knob or front panel Data Entry keyboard.
Accuracy (after the front panel CAL has been performed)		Accuracy of the center frequency is a function of the accuracy to which the center frequency is set between sweeps (covered by CF accuracy specification), and the amount of center frequency drift during a sweep. Center frequency drift can be significant during the first 30 min. after turn-on, or after a change in ambient temperature.
Bands 1 & 5-12 with Span/Div >200 kHz, and Bands 2-4, with Span/Div >100 kHz	$\pm[(20\% \text{ of Span/Div or Resoln Bandwidth, whichever is greater}) + (CF \times \text{ref freq error}) + (N \times 15 \text{ kHz})]$	Refer to "IF Frequency, LO Range, and Harmonic Number" specification for value of N. The 1st LO is unlocked in these spans. When the center frequency is changed within a band, a settling time of 1 s/GHz change in center frequency, divided by N should be allowed.
Bands 1 & 5-12 with Span/Div \leq 200 kHz and bands 2-4 with Span/Div \leq 100 kHz	$\pm[(20\% \text{ of Span/Div or Resoln Bandwidth, whichever is greater}) + (CF \times \text{ref freq error}) + (2N + 25 \text{ Hz})]$	The 1st LO is phase locked in these spans

Table 2-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
CF Drift (constant ambient temperature and fixed center frequency) After 30 minute warmup: Bands 1 & 5-12 with Span/Div >200 kHz, and Bands 2-4 with Span/Div >100 kHz		Since the center frequency is corrected before each sweep the only error observed is during sweep time. $\leq (25 \text{ kHz})N$ per minute of sweep time
Bands 1 & 5-12 with Span/Div ≤ 200 kHz Bands 2-4 with Span/Div ≤ 100 kHz		≤ 150 Hz per minute of sweep time
After 1 hour warmup: Bands 1 & 5-12 with Span/Div >200 kHz and Bands 2-4 with Span/Div >100 kHz		$\leq (5 \text{ kHz}) N$ per minute of sweep time
Bands 1 & 5-12 with Span/Div ≤ 200 kHz and Bands 2-4 with Span/Div ≤ 100 kHz	≤ 50 Hz per minute of sweep time	
Readout Resolution		At least 10% of Span/Div
Signal Counter Accuracy	$\pm [(\text{Counter frequency} \times \text{frequency reference error}) + (10 + 2N)\text{Hz} + 1 \text{ LSD}]$	
Sensitivity	Signal level at center screen must 20 dB or more above the average noise level and within 60 dB of the Reference Level	
Readout Resolution		1 Hz through 1 GHz, selectable with COUNT RESOLN control
Reference Frequency Error Aging Rate		1×10^{-7} for first six months then less than 1×10^{-7} per year
Accuracy during warmup at 25°C (ambient) and 30 minutes after power on		Within 5×10^{-8} of the frequency after 24 hours
Temperature sensitivity		Within 2×10^{-8} over the instrument operating range of -15°C to $+55^\circ\text{C}$, referenced to $+25^\circ\text{C}$
Residual FM (short term) after 1 hour warmup: Bands 1 & 5-12 with Span/Div >200 kHz, and bands 2-4 with Span/Div >100 kHz	$\leq (7 \text{ kHz})N$ total excursion in 20 ms	
Bands 1 & 5-12 with Span/Div ≤ 200 kHz Bands 2-4 with Span/Div ≤ 100 kHz	$\leq (10 + 2N)\text{Hz}$ total excursion in 20 ms	

Table 2-1 (cont)

Characteristic	Performance Requirement	Supplemental Information		
"Static" Resolution Bandwidth (6 dB down)	30 Hz then 100 Hz to 1 MHz in decade steps plus an AUTO position. Resolution bandwidth is within 20% of the selected bandwidth.	In AUTO position the bandwidth is automatically selected by an internal computer whose output depends on the setting of the SPAN/DIV, TIME/DIV, Vertical Display, and Video Filter selectors. When the RESOLUTION BANDWIDTH and TIME/DIV selectors are set to AUTO the microcomputer selects the optimum resolution for the SPAN/DIV settings.		
Shape Factor (60 dB/6 dB)	7.5:1 or less, and 15:1 or less for 30 Hz resolution bandwidth.			
Noise Sidebands	At least -75 dBc at 30 times the resolution offset (-70 dBc for resolution bandwidths ≤ 100 Hz).			
Video Filter Narrow		Reduces video bandwidth to approximately 1/300 of the selected resolution bandwidth and 1/100 for 30 Hz bandwidth.		
Wide		Reduces video bandwidth to approximately 1/30 of the selected resolution bandwidth and 1/10 for 30 Hz bandwidth.		
Pulse Stretcher Fall-time		30 μs/div (± 50%)		
Frequency Span/Div Range—in a 1-2-5 sequence with the SPAN/DIV control, or by two significant digits from the Data Entry keyboard		Band	Narrow Span/Div	Wide Span/Div
		1-3 (0-7.1 GHz)	50 Hz	200 MHz
		4-5 (5.4-21 GHz)	50 Hz	500 MHz
		6 (18-26 GHz)	50 Hz	1 GHz
		7-9 (26-90 GHz)	50 Hz	2 GHz
		10 (75-140 GHz)	50 Hz	5 GHz
		11-12 (110-325 GHz)	50 Hz	10 GHz
		Two additional positions provide full band (MAX Span) display or 0 Hz (Zero Span) display.		
Accuracy/Linearity	Within 5%, of the selected Span/Div over the center 8 divisions of a 10 division display.			

Table 2-1 (cont)

Characteristic	Performance Requirement		Supplemental Information
^a Frequency Response	About the mid-point (mean) between two extremes Referenced to 100 MHz		Frequency response is measured with 10 dB of RF attenuation and Peaking optimized for each center frequency setting, when applicable. Response includes the effect of input vswr, mixing mode (N), gain variation, pre-selector, and mixer. Digital storage typically increases errors by $\pm 0.5\%$. Display flatness is typically 1 dB greater than frequency response. Refer to Rackmount/Benchtop data (Option 30, 31, and 32) in the Options section for variance.
Coaxial (direct) Input			
Band 1 50 kHz-1.8 GHz 10 kHz-1.8 GHz	± 1.5 dB ± 2.0	± 2.5 dB ± 3.0 dB	
Band 2 1.7-5.5 GHz	± 2.5 dB	± 3.5 dB	
Band 3 3.0-7.1 GHz	± 2.5 dB	± 3.5 dB	
Band 4 5.4-18.0 GHz	± 3.5 dB	± 4.5 dB	
Band 5 15.0-21.0 GHz	± 5.0 dB	± 6.5 dB	
External Tektronix High Performance Waveguide Mixers			
Band 6 18.0-26 GHz	± 3.0 dB	± 6.0 dB	
Band 7 26.0-40.0 GHz	± 3.0 dB	± 6.0 dB	
Band 8 33.0-60.0 GHz	± 3.0 dB	± 6.0 dB	
Band 9 50.0-90.0 GHz	Typically ± 3 dB over any 5 GHz bandwidth		
Band 10 75.0-140.0 GHz	Typically ± 3 dB over any 5 GHz bandwidth		
Band 11 110-220 GHz	Typically ± 3 dB over any 5 GHz bandwidth		
Band 12 170-325 GHz	Typically ± 3 dB over any 5 GHz bandwidth		

^aRefer to "Verification of Tolerance Limits" at the beginning of this specification.

Table 2-2
IF Frequency, LO Range, and Harmonic Number (N)

Band and Freq Range		LO Range and Harmonic (N)	1st IF (MHz)
1 (0—1.8 GHz)		2072-3872 (1 -)	2072
2 (1.7—5.5 GHz)		2529-6329 (1 -)	829
3 (3.0—7.1 GHz)		2171-6271 (1 +)	829
4 (5.4—18.0 GHz)		2072-6276 (3 -)	829
5 (15—21 GHz)		4309-6309 (3 +)	2072
6 (18—26 GHz)		2655-4071 (6 +)	2072
7 (26—40 GHz)		2443-3793 (10 +)	2072
8 (33—60 GHz)		3792-5790 (10 +)	2072
9 (50—90 GHz)		3195-5862 (15 +)	2072
10 (75—140 GHz)		3170-6000 (23 +)	2072
11 (110—220 GHz)		2917-5790 (37 +)	2072
12 (170—325 GHz)		2998-5841 (56 +)	2072

Table 2-3
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Vertical Display Modes		10 dB/Div, 2 dB/Div, and linear. Any integer between 1-15 dB/Div can also be selected with the Data Entry keyboard.
Reference Level (full screen) Range		-117 dBm to +40 dBm; +40 dBm includes 10 dB of IF gain reduction, +30 dBm is the maximum safe input for log mode. In LIN mode, range is 50 nV/Div to 2 V/Div, 1 W maximum safe input
Steps		In the 10 dB/DIV display mode, steps are 10 dB for the coarse mode and 1 dB for the FINE mode. In the 2 dB/DIV mode, steps are 1 dB for coarse and 0.25 dB for FINE. When the dB/Div is set through the Data Entry keyboard, the coarse steps correspond to the display mode. The FINE steps are 1 dB when the mode is 5 dB/Div or more and 0.25 dB/Div for display modes of 4 dB/Div or less (referred to as ΔA mode). In LIN mode the steps are in equivalent 1 dB increments for FINE and in a 1-2-5 Volts/Div sequence for coarse.

Table 2-3 (cont)

Characteristic	Performance Requirement	Supplemental Information
Accuracy		Accuracy is a function of RF attenuation, IF gain, resolution bandwidth, display mode, calibrating source (i.e., internal calibrator), frequency band and response. Refer to accuracies of these characteristics. When the CAL button is activated the processor runs a calibrating routine, which if completed, reduces the REF LEVEL error between different resolution bandwidths. Also, if the instrument ambient temperature is changed after a calibration is run, the REF LEVEL error typically can change ± 0.05 dB/°C but may increase to ± 0.15 dB/°C with some instrument settings. The input RF attenuator steps 10 dB for reference level changes above -30 dBm (-20 dBm when MIN NOISE is active) unless the MIN RF ATTEN setting is greater than zero. The IF gain increases 10 dB for each 10 dB reference level change below -30 dBm (-20 dBm for MIN NOISE mode).
Display Dynamic Range		80 dB maximum, for log mode, and 8 divisions linear
Accuracy	± 1.0 dB/10 dB to a maximum cumulative error of ± 2.0 dB over 80 dB range ± 0.4 dB/2 dB to a maximum cumulative error of ± 1.0 dB over 16 dB range LIN mode is $\pm 5\%$ of full scale	
RF Attenuator Range		0-60 dB in 10 dB steps
Accuracy °Dc to 4 GHz	Within 0.3 dB/10 dB to a maximum of 0.7 dB over the 60 dB range	
4 GHz to 18 GHz	Within 0.5 dB/10 dB to a maximum of 1.4 dB over the 60 dB range	
IF Gain Range		87 dB of gain increase, 10 dB of gain decrease (MIN NOISE activated), in 10 dB and 1 dB steps.
Accuracy	Gain steps are monotonic (same direction) with the following limits: Within 0.2 dB/dB to a maximum of 0.5 dB/9 dB, except at the decade transistions of -19 to -20 dBm, -29 to -30 dBm, -39 to -40 dBm, -49 to -50 dBm, and -59 to -60 dBm; where an additional 0.5 dB can occur, for a total of 1.0 dB per decade. Maximum deviation over the 97 dB range is within ± 2 dB.	

Table 2-3 (cont)

Characteristic	Performance Requirement	Supplemental Information		
Gain Variation between Resolution Bandwidths; (after CAL routine has been run)		Measured at -20 dBm MIN DISTORTION mode		
With respect to 1 MHz filter	Less than ± 0.4 dB			
Between any two filters	Less than 0.8 dB			
Differential Amplitude Measurement		ΔA mode provides differential measurements in 0.25 dB increments.		
Range		0 dB above to 48 dB below the reference level established when the ΔA mode was activated. DO NOT USE ΔA mode above +30 dBm reference level.		
Accuracy		dB Difference	Steps	Error
		0.25	1	0.15 dB
		2	8	0.4 dB
		10	40	1.0 dB
		50	200	2.0 dB
Spurious Responses Residual (no input signal), referenced to mixer input, and fundamental mixing for bands 1-3.	-100 dBm or less			
Intermodulation products 50 kHz to 1.8 GHz (Band 1 and 1.8 to 21.0 GHz for Bands 2-4)	At least -70 dBc from any two on screen signals within any frequency span	≥ -100 dBc when signals are separated 100 MHz or more in preselected bands		
1.7-1.8 GHz (Band 2 only)	At least -70 dBc from any two -40 dBm signals within any frequency span			
Harmonic Distortion 50 kHz-1.8 GHz (Band 1)	At least -60 dBc below a full screen signal in MIN DISTORTION mode			
1.7-21 GHz	At least -100 dBc			
LO Emission, with no (0) RF attenuation	Less than -70 dBm to 21 GHz			

*Refer to "Verification of Tolerance Limits" at the beginning of this specification.

Table 2-4
SENSITIVITY

Equivalent maximum input noise for each resolution bandwidth, using the internal mixer for bands 1–5 (50 kHz–18 GHz), and Tektronix High Performance Waveguide Mixers for bands 6–12 (18–325 GHz).

Band/Frequency	Equivalent Input Noise in dBm versus Resolution Bandwidth					
	30 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz
Band 1 50 kHz–1.8 GHz	–121	–118	–110	–100	–90	–80
Bands 2 & 3 1.7–7.1 GHz	–121	–118	–110	–100	–90	–80
Band 4 5.4–12.0 GHz	–106	–103	–95	–85	–75	–65
Band 4 12.0–18.0 GHz	–101	–98	–90	–80	–70	–60
Band 5 15.0–21.0 GHz	–96	–93	–85	–75	–65	–55
^a Band 6 18.0–26.5 GHz	–111	–108	–100	–90	–80	–70
^a Band 7 26.5–40.0 GHz	–106	–103	–95	–85	–75	–65
^a Band 8 33.0–60.0 GHz	–106	–103	–95	–85	–75	–65
^a Band 9 50.0–90.0 GHz	Typically –95 dBm for 1 kHz bandwidth at 50 GHz, degrading to –85 dBm at 90 GHz					
^a Band 10 75.0–140 GHz	Typically –90 dBm for 1 kHz bandwidth at 75 GHz, degrading to –75 dBm at 140 GHz					
^a Band 11 110–220 GHz	Typically –80 dBm for 1 kHz resolution bandwidth at 110 GHz, degrading to –65 dBm at 220 GHz					
^a Band 12 170–325 GHz	Typically –70 dBm for 1 kHz resolution bandwidth at 170 GHz, degrading to –55 dBm at 325 GHz					

^aTektronix High Performance Waveguide Mixers

<http://manomanskill.com>

Table 2-5
INPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
RF INPUT		Type N female connector, specified to 21 GHz.
Input Impedance		50 Ω ; vswr with RF attenuation ≥ 10 dB: 50 kHz–2.5 GHz; 1.3:1 (typically 1.2:1) 2.5–6.0 GHz; 1.7:1 (typically 1.5:1) 6.0–18 GHz; 2.3:1 (typically 1.9:1) 18–21 GHz; 3.5:1 (typically 2.7:1)
Maximum Safe Input		+30 dBm (1 W) continuous, 75 W peak, pulse width 1 μ s or less with a maximum duty factor of 0.001 (attenuator limit). DO NOT APPLY DC VOLTAGE TO THE RF INPUT
1 dB Compression Point (minimum)		
1.7–2.0 GHz	–28 dBm	With no RF attenuation
Otherwise	–18 dBm	With no RF attenuation
Optimum level for linear operation		–30 dBm, referenced to input mixer. This is achieved in MIN DISTORTION mode when not exceeding full screen display.
External Mixer		Input for an IF signal and the source of bias for external waveguide mixers. Bias range +1.0 to –2.0 V, 70 Ω source.
EXTERNAL REFERENCE		
Frequency	1, 2, 5, or 10 MHz, ± 5 ppm	
Power	–15 dBm to +15 dBm.	
Waveshape		Sinewave, ECL or TTL. (Allowable duty cycle symmetry is 40-60%)
Input Impedance		50 Ω ac, 500 Ω dc
HORIZ/TRIG		Dc coupled input for horizontal drive and ac coupled for trigger signal
Input Voltage Range Sweep		0 to +10 V (dc + peak ac) for full screen deflection
Trigger	1.0 V peak, frequency 15 Hz to 1 MHz	Maximum input: 50 V (dc + peak ac). Maximum ac input: 30 Vrms to 10 kHz then derate linearly to 3.5 Vrms at 100 kHz and above. Pulse width is 0.1 μ s minimum.
MARKER/VIDEO		Video, 0 to +4 V, if Ext Video is selected; or, it interfaces with the 1405 TV Sideband Adapter to insert an externally generated marker on internal video. Marker 0 to –10 V
ACCESSORY (J104)		
Pin 1—External Video Select		TTL logic 0 selects the External Video Input
Pin 2—External Preselector Out		± 15 V maximum
Pin 3—External Preselector Return		
Pin 5—Chassis Gnd		

Table 2-6
OUTPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Calibrator (CAL OUT)	-20 dBm ± 0.3 dB at 100 MHz (phase locked to reference oscillator)	100 MHz comb of markers provide amplitude calibration at 100 MHz and markers for frequency and span calibration, to 1.0 GHz
1st LO and 2nd LO		Provides access to the output of the respective local oscillators. 1st LO +7.5 dBm minimum, to a maximum of +15 dBm; 2nd LO -22 dBm minimum, to a maximum of +15 dBm. THESE PORTS MUST BE TERMINATED IN 50 Ω AT ALL TIMES.
EXTERNAL MIXER		In the EXTERNAL MIXER mode, bias range is +1.0 to -2.0 V; or, with change of internal straps, -1.0 to +2.0 V.
VERTical		Provides 0.5 V ±5% of signal per division of video that is above and below the centerline. Source impedance approximately 1 kΩ.
HORIZ Out		Provides 0.5 V/div either side of center. Full range -2.5 V to +2.5 V. Source impedance approximately 1 kΩ.
PEN LIFT		TTL compatible, nominal +5 volts to lift pen.
10 MHz IF		Access to the 10 MHz IF. Output level is approximately -5 dBm for a full screen signal at -30 dBm reference level. Nominal impedance approximately 50 Ω.

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Table 2-7
GENERAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
IEEE Std 488-1978 Port (GPIB) 494P		In accordance with IEEE 488 standard, and Tektronix codes and format standard Version 81.1
PROBE POWER		Provides operating voltages for active probes. Output voltages are: Pin 1, +5 V @ 100 mA max. Pin 2, ground. Pin 3, -15 V @ 100 mA max. Pin 4, +15 V @ 100 mA max. (see Figure 2-1)
Sweep Sweep Time	20 μ s/Div to 5 s/Div in 1-2-5 sequence (10 s/Div available in AUTO).	Triggered, auto, manual, and external.
Accuracy	$\pm 5\%$.	
Triggering	2 division or more of signal for internal; and 1.0 V peak, minimum, for external	
Crt Readout		Displays: Reference level, frequency, vertical display mode, frequency span/div, frequency range, resolution bandwidth, RF attenuation, internal or external frequency reference, and GPIB states (494P only)
Non-volatile Memory		Instrument settings, displays, calibration offsets, and preselector peaking codes for each band are stored in back-up battery powered CMOS RAM. Battery life @ +55°C instrument ambient temperature, is 1-2 years. At +25°C, life should be greater than 5 years. Retention of data in non-volatile memory will occur over the range of -15°C to +55°C operating, and -30 to +85°C non-operating.

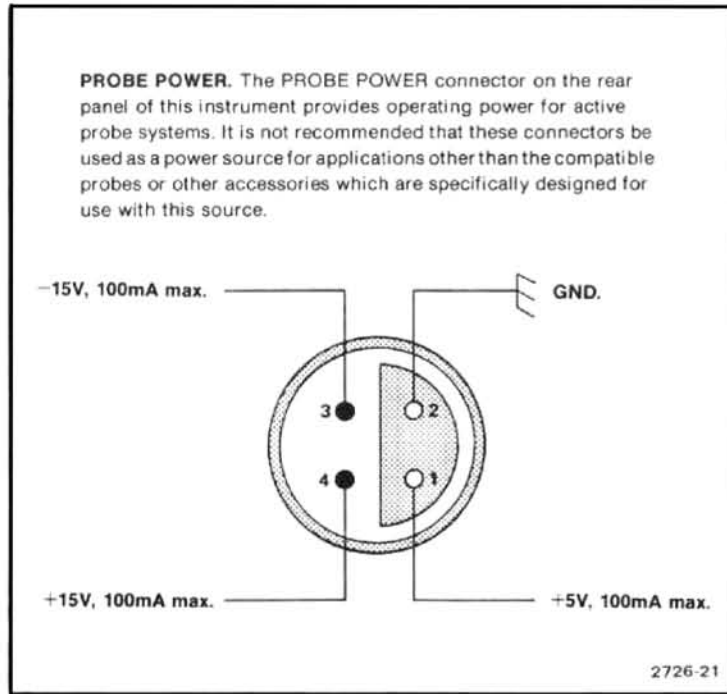


Figure 2-1. Probe Power connector pin out.

**Table 2-8
POWER REQUIREMENTS**

Characteristic	Description
Input Voltage	90 to 132 Vac or 180 to 250 Vac, 48 to 440 Hz.
Power	At 115 V, 60 Hz; 210 watts maximum, 3.2 amperes.
Leakage Current	5 mA maximum

NOTE

If power to this instrument is interrupted, it may be necessary to re-initialize the microcomputer; when power is restored, turn the POWER switch OFF for 5 seconds then back ON.

**Table 2-9
ENVIRONMENTAL CHARACTERISTICS**

Meets MIL T-28800C, type III class 3, style C specifications, comprised of the following:

Characteristic	Description
Temperature	
Operating and Humidity	- 10 to +55°C/95% (+5%, -0%) relative humidity. (Instrument is tested and meets - 15 to +55°C)
Non-operating	- 62 to +85°C.

Table 2-9 (cont)

Characteristic	Description	
<i>NOTE</i>		
<i>After storage at temperatures below the operating range, the microcomputer may not initialize on power-up. If so, allow the instrument to warm up for 15 minutes and re-initialize the microcomputer by turning the POWER Off for 5 seconds then back On.</i>		
Altitude		
Operating	15,000 feet	
Non-operating	40,000 feet	
Humidity (Non-operating)	Five cycles (120 hours) in accordance with Mil-Std-810	
Vibration		
Operating (instrument secured to a vibration platform during test)	MIL-Std-810, Method 514 Procedure X (modified). Resonant searches along all three axis at 0.020 inch displacement, frequency varied from 5-55 Hz for 15 minutes. All major resonances must be minimum/axis plus dwell at the resonant frequency, or 55 Hz if no resonance is found for 10 minutes minimum. Total vibration time about 75 minutes.	
Shock (operating and non-operating)	Three shocks of 30 g, one-half sine, 11 ms duration each direction along each major axis. Guillotine-type shocks. Total of 18 shocks.	
Transit drop (free fall)	8 inch, one per each of six faces and eight corners. (Instrument is tested and meets drop height of 12 inches.)	
Electromagnetic Interference (EMI)	Meets requirements described in Mil-Std-461B Part 4, except as noted	
	Test Method	Remarks
Conducted Emissions	CEO1—60 Hz to 15 kHz.	1 kHz to 15 kHz only.
	CEO3—15 kHz to 50 MHz power leads.	15 kHz to 50 kHz, relaxed by 15 dB.
Conducted Susceptibility	CSO1—30 Hz to 50 kHz power leads.	Full limits.
	CSO2—50 kHz to 400 MHz power leads.	Full limits.
	CSO6—spike power leads.	Full limits.
Radiated Emissions	REO1—30 Hz to 50 kHz magnetic field.	Relaxed by 10 dB for fundamental to 10th harmonic of power line. Excepted, 30 kHz to 36 kHz.
	REO2—14 kHz to 10 GHz.	Full limit.
Radiated Susceptibility	RSO1—30 Hz to 50 kHz.	Full limit.
	RSO2—Magnetic Induction	To 5 A only
	RSO3—14 kHz to 10 GHz	Up to 1 GHz

Table 2-10
PHYSICAL CHARACTERISTICS

Characteristic	Description
Weight (standard accessories and cover, except manuals)	52 pounds (24 kg) maximum
Dimensions	
Without front cover, handle, or feet	6.9 X 12.87 X 19.65 inches (175 X 327 X 499 millimeters)
With front cover, feet, and handle	9.15 X 15.05 X 23.1 inches (232 X 382 X 587 millimeters) with the handle folded back over the instrument, 28.85 inches (732.8 mm) with the handle fully extended

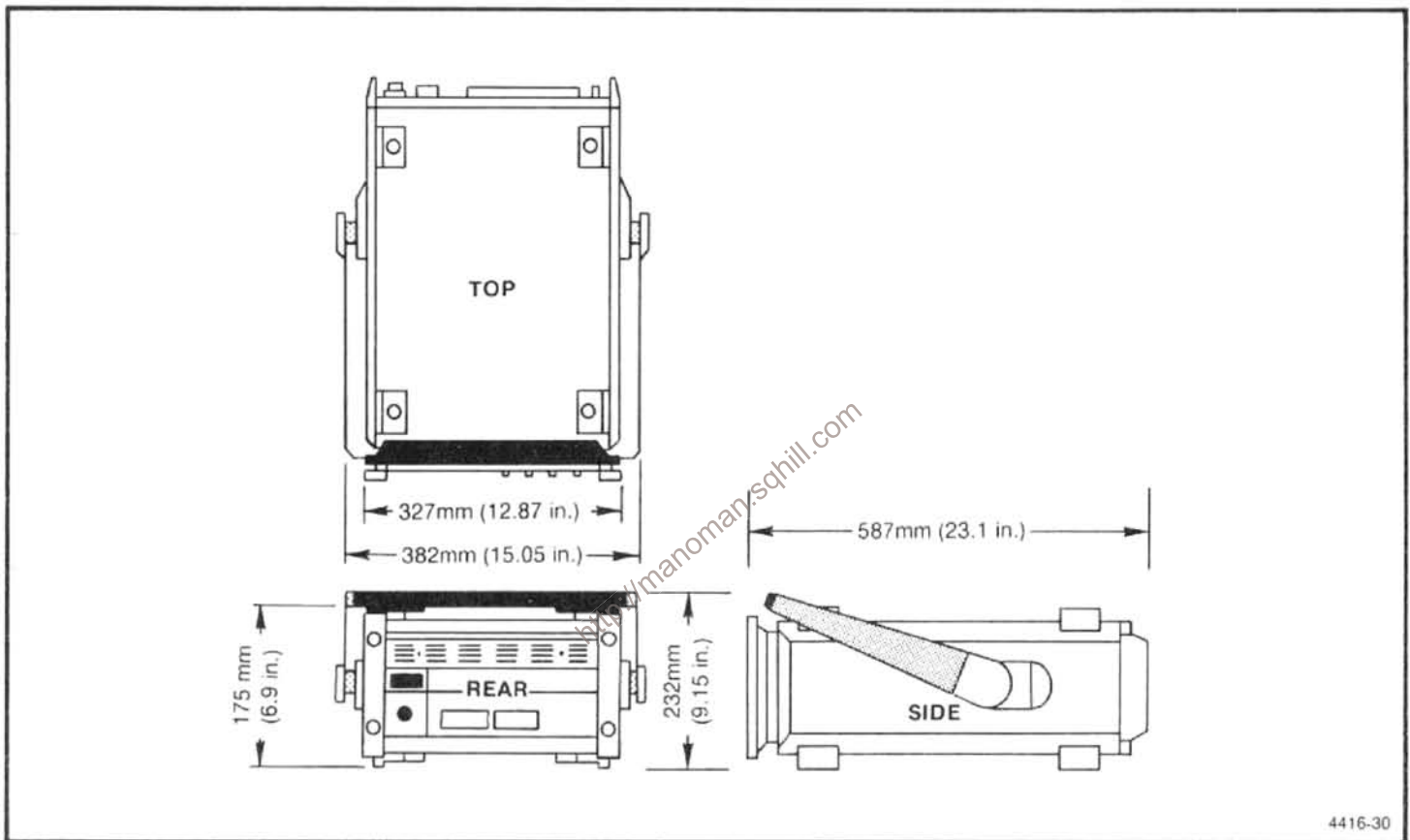


Figure 2-2. 494/494P Dimensions.

Table 2-11
494/494P SAFETY STANDARD AND REGULATORY REQUIREMENT CONFORMANCE

Subject	Description
Safety Standards	
CSA	Electrical Bulletin
FM	Electrical Utilization Standard Class 3820
ANSI C39.5	Safety Requirements for Electrical and Electronic Measuring and Controlling Instrumentation
IEC 348 (2nd edition)	Safety Requirements for Electronic Measuring Apparatus
Regulatory Requirement	
VDE 0871 Class B	Regulations for RFI Suppression of High Frequency Apparatus and Installations

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INSTALLATION, PREPARATION FOR USE, REPACKAGING AND STORAGE

INTRODUCTION

This section contains unpacking, installation, power requirements, repackaging information, and long- and short-term storage for the 494/494P Spectrum Analyzer.

UNPACKING AND INITIAL INSPECTION

Before unpacking the 494/494P from its shipping container or carton, inspect for signs of external damage. If the carton is damaged, notify the carrier. The shipping carton contains the basic instrument and its standard accessories. Refer to the Standard Accessories list in Section 1 of either the Operators or Service Vol. 1, manual. The list with illustrations is also in Volume 2 of the Service manual following the Mechanical Parts Replacement listing.

If the contents of the shipping container are incomplete, if there is mechanical damage or defect, or if the instrument does not meet operational check requirements, contact your local Tektronix Field Office or representative. If the shipping container is damaged, notify the carrier as well as Tektronix, Inc.

The instrument was inspected both mechanically and electrically before shipment. It should be free of mechanical damage and meet or exceed all electrical specifications. Procedures to check functional or operational performance are in the Operation section. Performing the functional check procedure verifies instrument is operating properly. This check should satisfy the requirements for most receiving or incoming inspections. A detailed electrical performance verification procedure in the Service instructions provides a check of all specified performance requirements, as listed in the Specification section.

The 494/494P can be installed in any position that allows air flow in the bottom and out the rear of the instrument. Feet on the four corners allow ample clearance even if the instrument is stacked with other instruments. A fan draws air in through the bottom and expels air out the back. Avoid locating the instrument where paper, plastic, or like material might block the air intake.

The front panel cover provides a dust-tight seal and convenient place to store accessories and external waveguide mixers. Use the cover to protect the front panel when storing or transporting the instrument. The cover is removed by first pulling up and in on the two release latches, then pull up on the cover. The door to the accessories compartment is unlatched and opened by pressing the latch to the side and lifting the cover.

The handle of the 494/494P can be positioned at several angles to serve as a tilt stand, or it can be positioned at the top rear of the instrument between the feet and the rear panel, so instruments can be stacked. To position the handle, press in at both pivot points and rotate the handle to the desired position.

CAUTION

Removing or replacing the cabinet on the instrument can be hazardous. The cabinet should only be removed by qualified service personnel. Removal instructions are contained in the Maintenance section.

Installation instructions for the rackmount/benchtop versions of the instrument are described in the Options Section of this manual. Refer installation to qualified service personnel.

CAUTION

If the rackmount version is extended out of the rack and tipped up to gain access to the bottom or back panels of the cabinet, it can fall back into the rack unless it is held. Use care when doing this to avoid damaging the front panel or equipment that may be mounted above the 494/494P.

POWER SOURCE AND POWER REQUIREMENTS

The 494/494P is designed to operate from a single-phase power source that has one of its current-carrying conductors (neutral) at ground (earth) potential. Operating from power sources where both current-carrying conductors are isolated or above ground potential (such as phase-to-phase on a multi-phase system or across the legs of a 110-220 V single-phase, three-wire system) is not recommended, since only the line conductor has over-current (fuse) protection within the unit. Refer to the Safety Summary at the front of this manual.

The ac power connector is a three-wire polarized plug with the ground (earth) lead connected directly to the instrument frame to provide electrical shock protection. If the unit is connected to any other power source, the unit frame must be connected to an earth ground.

The 494/494P can be operated from either 115 Vac or 230 Vac nominal line voltage with a range of 90 to 132 or 180 to 250 Vac, at 48 to 440 Hz. Power and voltage requirements are printed on a back-panel plate mounted below the power input jack.

WARNING

Only qualified service personnel should attempt to change the power input requirements. Unfamiliarity with safety procedures can result in personal injury. Refer to the Safety Summary at the front of this manual.

Input power requirements are changed with a switch on the back panel (see Figure 3-1) and the replacement of the input line fuse, F301. F301 is a 4A fast blow for 115 Vac nominal, and 2A slow blow for 220 Vac nominal.

Remove the protective cover and position the switch to the desired setting.

Remove the holder and line fuse and replace with a fuse that is rated according to the input voltage specification.

The power cord should also be replaced. Figure 3-2 illustrates these power cord options and the following table lists their part number.

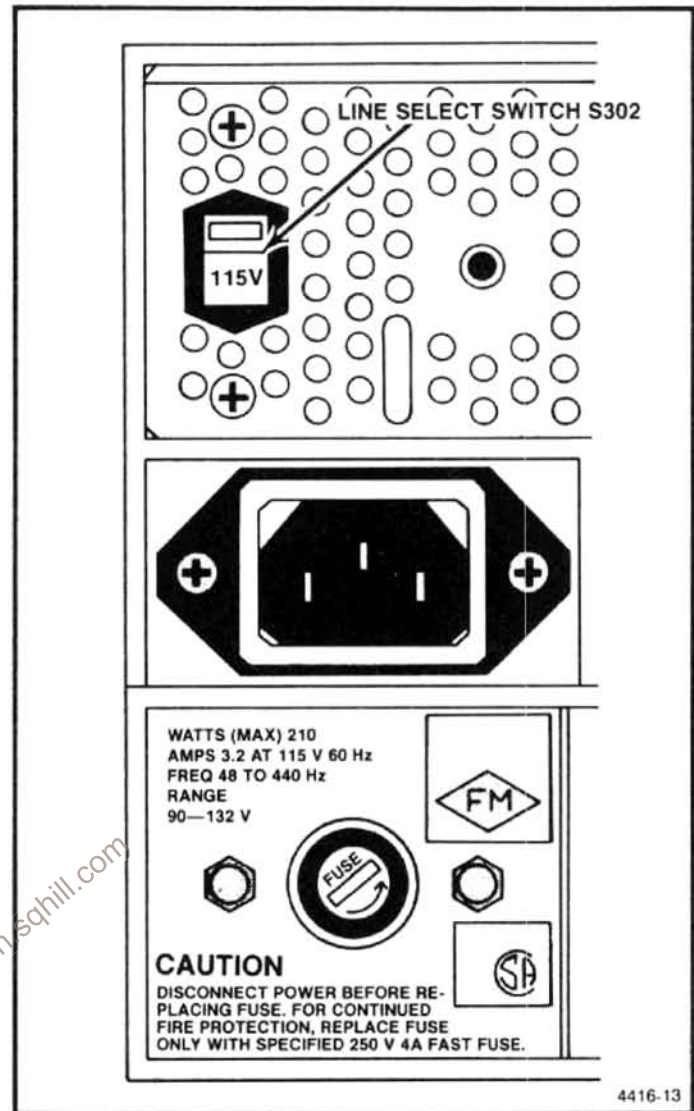


Figure 3-1. Location of input power selector switch and line fuse.

Power Cord Options

Option	Description	P/N
A1	Universal Euro, 220 V/50 Hz @ 16A	161-0132-00
A2	United Kingdom U.K., 240 V/50 Hz @ 13A	161-0133-00
A3	Australian, 240 V/50 Hz, @ 10A	161-0135-00
A4	North American, 240 V/60 Hz, @ 12A	161-0134-00
A5	Swiss, 250 V/50 Hz, @ 6A	161-0167-00

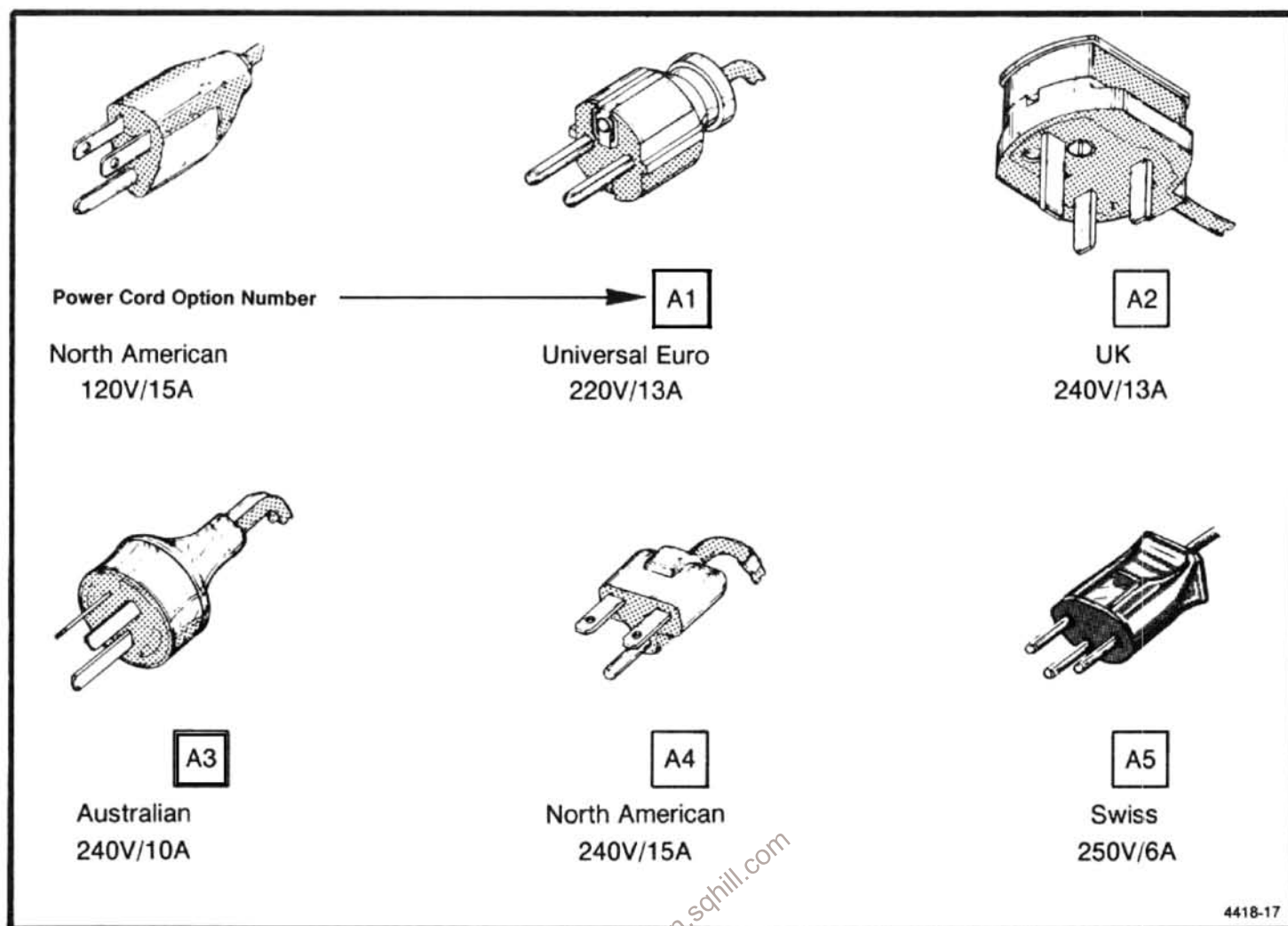


Figure 3-2. International power cord and plug configuration for the 494/494P.

REPACKAGING FOR SHIPMENT

When the 494/494P is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner and address, name of individual at your firm that can be contacted, complete serial number, and a description of the service required. If the original package is unfit for use or not available, repackage the equipment as follows:

1. Obtain a carton of corrugated cardboard having inside dimensions that are at least six inches more than the equipment dimensions, to allow for cushioning. Table 3-1 lists instrument weights and the carton strength requirements.

2. Install the front cover and surround the instrument with polyethylene sheeting to protect the finish.

3. Cushion the equipment on all sides with packing material or urethane foam between the carton and the sides of the instrument.

4. Seal with shipping tape or industrial stapler.

Table 3-1
SHIPPING CARTON TEST STRENGTH

Gross Weight		Carton Test Strength	
Pounds	Kilograms	Pounds	Kilograms
0-10	0-3.73	200	74.6
10-30	3.73-11.19	275	102.5
30-120	11.19-44.76	375	140.0
120-140	44.76-52.22	500	186.5
140-160	52.22-59.68	600	223.8

If you have any questions, contact your local Tektronix Field Office or representative.

STORAGE

Short Term

There are no requirements for short term storage (less than 90 days) other than store the instrument in an environment that meets the non-operating environmental specifications.

Long Term

If you plan to store the instrument for more than 90 days, retain the shipping container to repackage the instrument. The battery in the instrument is lithium, which does not require removal. Package the instrument in a vapor bag with desiccant and store in a location that meets the environmental non-operating specifications.

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PERFORMANCE CHECK

INTRODUCTION

The procedures in this section verify that the instrument is performing according to the characteristics that have limits and performance requirements as specified under the Performance Requirement column in the Specifications section. Some of the non-specified parameters and instrument functions are also checked. This check verifies that the instrument is calibrated and will perform as described. All tests can be performed without access to the interior of the instrument.

Checks should be performed in sequence because some tests rely on the satisfactory performance of related circuits, and the procedures are arranged to minimize test equipment setup. If a performance measurement is marginal or below specification, an adjustment procedure to optimize the circuit performance will be found, under a similar heading, in the Adjustment section. After adjustment, recheck the performance. We recommend adjusting only those circuits that do not meet performance criteria.

If adjustment fails to return the circuit to specified performance, refer to the Maintenance section for troubleshooting and repair procedures.

Procedures that are unique to instrument options, are described as a sub-part of the step within this section.

INCOMING INSPECTION TEST

The Operators manual contains an operational or functional check that checks all functions of the 494/494P. This check is recommended for incoming inspections because it requires no external equipment or special expertise and is a reliable indication that the instrument is performing properly.

VERIFICATION OF TOLERANCE VALUES

Compliance tests, of those limits listed in the Performance Requirement column of the instrument specifica-

tions, shall be performed after sufficient warm-up time and completion of preliminary preparation steps (such as front-panel adjustments). Measurements shall be performed by instruments that do not affect the values measured.

Measurement tolerance of test equipment should be negligible in comparison to the specified tolerance; and, when not negligible, the error of the measuring apparatus shall be added to the tolerance specified.

HISTORY INFORMATION

The instrument and manual are periodically evaluated and updated. If modifications require changes in the procedures, information applicable to earlier instruments will be included within a step or as a sub-part to a step.

EQUIPMENT REQUIRED

Table 4-1 lists the test equipment and calibration fixtures recommended for the Performance Check. This equipment is also applicable for the adjustment procedures in the next section. The characteristics specified are the minimum required for the checks. Substitute equipment must meet or exceed these characteristics. Special calibration fixtures are listed because they facilitate the procedure. These fixtures are available from Tektronix, Inc., and may be ordered through your local Tektronix Field Office or representative.

Because some characteristics may require sophisticated tests equipment and/or procedures to accurately measure which may not be practical. In this case a compromise may be made in these procedures to facilitate checking the characteristic. If this is the case a statement or footnote to this fact is added to the step. The more exact method of measuring the characteristic can be supplied by your Tektronix Service Center.

Table 4-1
EQUIPMENT REQUIRED

Equipment or Test Fixture	Characteristics	Recommendation and Use
PERFORMANCE CHECK		
Test Oscilloscope	Vertical sensitivity, 50 mV/Div to 5 V/Div	Any TEKTRONIX 7000-Series oscilloscope with plug-in units for real-time display such as: 7A11/7B50A, and P6108 1X Probe (used to monitor signal and voltage levels)
Two (2) Time Mark Generators	Marker output, 1 s to 1 μ s; accuracy 0.001%	TEKTRONIX TG 501 with TM 500-Series Power Module (used to check time/div and span accuracy)
Digital Counter	0 to 200 MHz, 1 Hz resolution, 25 mV sensitivity. Must have an internal or external reference oscillator with an absolute accuracy that is better than 10^{-9}	TEKTRONIX DC 510 or 5010 with TM 504 Power Module, or Hewlett-Packard 5316A (used to measure Calibrator frequency)
Function or Sine-Wave Generator	1 Hz to 1 MHz; 0 to 20 V - p-p	TEKTRONIX FG 503 Function Generator (used to check external trigger and horizontal input requirements)
Signal Generator(s)	10 Hz to 10 MHz, constant output. 250 kHz-110 MHz, leveled output Two (2) 500 kHz to 2.0 GHz generators calibrated and leveled. Output, -100 dBm to +10 dBm; spectral purity 60 dB or more below the fundamental.	Hewlett-Packard Model 654A (used to check attenuator and gain accuracy) TEKTRONIX SG 504, Hewlett-Packard Model 8640A/B and Model 8614A generators (used to check frequency response; and as a signal source for IM and display accuracy checks)
Sweep Oscillator	.01 to 21 GHz; frequency response, ± 1.0 dB, or 2.0 to 21 GHz (with 500 kHz to 2.0 GHz generators)	Hewlett-Packard Model 8350A with Model 83595A Option 002 Plug-in; or, 8620C and 86290B Option 40 Plug-in (used to check frequency response and flatness)
Power Divider	Dc to 22 GHz	Wienchel Model 1579B
Coaxial Detector	.01 to 26 GHz	Hewlett-Packard Model 8473C
Power Meter with Power Sensors	-60 dBm to -20 dBm full scale; 100 kHz to 26 GHz	Hewlett-Packard Model 435A or 436A with 8482A and 8485A Power Sensors
Vector Voltmeter or Power Meter with Low-pass Filter	Frequency to 100 MHz Measure -20 dBm, within ± 0.1 dB. The filter must have rolloff of 40 dB or more at 200 MHz.	Hewlett-Packard Model 8405A (used to check CALibrator OUTPUT) Hewlett-Packard Model 435A with 8482A Sensor (used to check CALibrator Output). Filter: Texscan or Lark

Table 4-1 (cont)

Equipment or Test Fixture	Characteristics	Recommendation and Use
PERFORMANCE CHECK (cont)		
UHF Comb Generator	Provide comb line to 18 MHz; accuracy 0.0%	TEKTRONIX Calibration Fixture 067-0885-00 with TM 500 Power Module (used to check frequency readout accuracy)
Spectrum Analyzer	Frequency range, 50 kHz - 2.2 GHz	TEKTRONIX 492, 494, or 7L18, 7L14 Option 39 (used to check compression point)
One 10 dB and One 1 dB Step Attenuator	Range, 0-110 dB, in 10 dB and 1 dB steps; accuracy ± 0.1 dB; frequency range, dc - 18 GHz	Step attenuator; such as Hewlett Packard 8494B and 8496B with 11716A inter connect kit, calibrated by precision standard attenuators; such as Weinchel Model AS-6 attenuator (used to check RF attenuator)
Step Attenuator One (1)	Range, 0 - 12 dB, in 1 dB steps; dc - 1 GHz, accuracy ± 0.25 dB to 0.5 GHz	Hewlett Packard 355C (used to check input compression)
Attenuator (SMA connectors)	3 dB, 50 Ω ; dc to 20 GHz	Weinchel Model 4M. Tektronix connectors) Part No. 015-1053-00
Two attenuators (bnc connectors)	20 dB, 50 Ω ; dc to 2.0 GHz	Tektronix Part No. 011-0059-02
Coaxial cable (50 Ω , 5 ns, sma connectors)		Tektronix Part No. 015-1006-00
Adapter (N male to sma male)		Tektronix Part 015-0369-00
Adapter (N male to No. bnc female)		Tektronix Part 103-0045-00
"T" Connector (bnc)		Tektronix Part No. 103-0030-00
Coaxial Cables (50 Ω) two required		Tektronix Part No. 012-0482-00

ADJUSTMENTS

All the items listed above plus the following are required for the Adjustment Procedure.

Return Loss Bridge	10 MHz to 1 GHz, 50 Ω	Wiltron VSWR Bridge Model 62BF50
Microwave Frequency Counter	10 Hz to 10 GHz, -20 dBm sensitivity	Hewlett-Packard Microwave Counter Frequency Counter 5342A (used to measure the 2nd LO frequency)
Attenuator (3 dB miniature)	Frequency to 5 GHz; connectors 5 mm	Weinchel Model 4M, Tektronix Part No. 015-1053-00

Table 4-1 (cont)

Equipment or Test Fixture	Characteristics	Recommendation and Use
ADJUSTMENTS (cont)		
Autotransformer	Capable of varying line voltage from 90 to 130 V _{ac}	General Radio Variac Type W10MT3
Digital Multimeter Dc Block	10 μ V to 350 V dc	TEKTRONIX DM 501A or DM 502A. Tektronix Part No. 015-0221-00
Adapter (Seaelectro male to male)		Tektronix Part 103-0098-00; Seaelectro Part No.51-072-0000
Adapter (bnc female to Seaelectro male)		Tektronix Part No. 103-0180-00
Three Extension Cables (Seaelectro female to Seaelectro male)		Tektronix Part No. 175-2902-00
Adapter (bnc to No. Seaelectro)		Tektronix Part No. 175-2412-00
Adapter (bnc female to sma male)		Tektronix Part No. 015-1018-00
Cable (20"), Tip plugs to bnc		Tektronix Part No. 175-1178-00
Coaxial cable (8")		Tektronix Part No. 012-0208-00
Screwdriver, tuning		Tektronix Part No. 003-0675-00
Alignment tool		Tektronix Part No. 003-0968-00 (square-pin adjustment tool for VR calibration)
Screwdriver, flat, 6" with 1/8" tip		
Screwdriver, Phillips No. 1		
Allen wrenches (3), 3/32", 5/64", 7/64"		
Service Kit (Extender boards) ^a		Tektronix Part No. 672-0865-00.

^a These fixtures are part of the Service Kit 006-3286-00 listed in the Maintenance section.

PRELIMINARY PREPARATION

1. Firmware Version

During initial turn-on or power-up cycle, the instrument and the front panel processor firmware versions are displayed on the crt for approximately two seconds. The Replacement Parts List in the Service manual, Volume 2, lists the ROMs used for each version. The service manual also lists the firmware operating notes associated with each firmware version.

2. Error Message Readout

If the microcomputer detects a hardware failure, a failure report will come on screen and remain for about 2 seconds. A status message will then appear and remain for the duration of the failure. Press HELP to obtain an error message that explains the impact of the failure on instrument operation. If the processor cannot set the oscillator frequency, due to a hardware failure, it will continue to try each sweep. The sweep holdoff time will increase substantially as it tries. To disable attempted oscillator corrections, press <SHIFT> and then FREE RUN. Center frequency accuracy specifications will not be met in this mode. Pressing <SHIFT> FREE RUN again will re-enable oscillator correction routines. Another failure message will appear if the failure has not been corrected. The following are other error messages that may appear:

CALIBRATION FAILED — see Reference Level and Frequency Calibration part of the CAL routine.

COUNTER FAILURE — either a hardware problem will not allow the counter to work or there is insufficient signal level for a count.

POWER SUPPLY FAILURE — one or more of the power supplies is out of regulation.

NON-VOLATILE RAM CHECK SUM ERROR — a checksum error on data in this memory has occurred. Either the CMOS RAM has not been initialized with data for the first time or the battery or the RAM has failed.

3. Initial Turn-on

a. Connect the 494/494P power cord to an appropriate power source (see "Power Requirements" under Installation and Repackaging, in Section 3) and switch POWER on.

b. When POWER is switched on (power up), the processor will run a memory and I/O test. If a problem exists, a failure message will appear on screen. By pressing the continue key, as directed in the message, the operator can bypass the failed test and attempt to use the instrument; however, performance may not be as specified. The program will complete in about 6 seconds and the instrument will be ready to operate if there is not a problem. Note that the crt readout is functioning.

4. Calibrate Center Frequency, Reference Level, and Dynamic Range

NOTE

When the <SHIFT> CAL function is activated, the 494/494P microcomputer performs a center frequency and reference level calibration. This calibration is required before the instrument will meet its center frequency and reference level accuracy performance specifications. A recalibration should be done any time the ambient temperature changes from the last calibration and at regular intervals to ensure that the instrument frequency and amplitude measurements are accurate. An explanation of Reference Level Accuracy, with respect to ambient temperature, is described in the Specifications section.

After the microcomputer has completed a calibration routine, the results can be observed by pressing <SHIFT> MIN NOISE. The "Internal Calibration Result" message shows the correction factor used to center the resolution bandwidth filters and to bring the amplitude level within 0.4 dB of the 1 MHz filter.

a. Press the <SHIFT> CAL to start the calibration routine. A message on the crt will direct the user how to adjust the Vertical and Horizontal POSITION, AMPL and LOG CAL potentiometers. This sets the absolute Reference Level for the 1 MHz resolution bandwidth filter. An automatic calibration is then run by the microcomputer, which measures and corrects frequency and amplitude errors of the other filters with respect to the 1 MHz filter and the reference frequency. As stated above, these correction factors are held in non-volatile memory. Press FINE to continue or <SHIFT> to exit the routine.

b. If the processor can complete the routine, the instrument control settings will return for normal operation. If a CALIBRATION FAILED message appears, refer to the correction factors by pressing <SHIFT> MIN NOISE.

If any amplitude correction factor, at room temperature, for a filter is greater than 1 dB, the filter in the VR assembly should be readjusted. Refer to the Adjustment Procedure section.

PERFORMANCE CHECK PROCEDURE

1. Check Operation of Front Panel Pushbuttons and Controls

Shift Functions — In the shift mode, those buttons with two or more functions, indicated by the blue and/or orange lettered nomenclature beside the button, activate the shift function when pressed. In some cases a parameter or command is entered followed by data, via the Data Entry keyboard, then terminated with a multiplier, unit value, or display scale factor.

The following procedures check the operation of all front panel pushbuttons, selectors, and controls. The buttons should illuminate when the function is active.

a. Set the FREQUENCY to 100 MHz, REF LEVEL to -20 dBm, and FREQ SPAN/DIV to 20 kHz. Apply the CAL OUT signal to the RF INPUT, by using the 50 Ω cable and bnc-to-N adapter, then change the Vertical Display to 2 dB/DIV.

b. Note that the following pushbuttons and controls operate as described when they are activated.

INTENSITY — Rotate the control through its range and note crt beam brightness change.

READOUT — When this button is not illuminated, off mode, crt readout is off. In the active state (button illuminated), there is crt readout of REF LEVEL, FREQUENCY, FREQ SPAN/DIV, VERT DISPLAY, RF ATTEN, FREQ RANGE, REFERENCE OSCILLATOR, and RESOLUTION BANDWIDTH. The INTENSITY control changes the brightness of readout characters as well as the display.

GRAT ILLUM — When activated (active state) the graticule is illuminated. In the off mode the graticule lights are dim.

BASELINE CLIP — When activated (illuminated) the baseline of the display, up to about one graticule division, is clipped (blanked).

Triggering — Triggering mode is activated by pressing one of four pushbuttons. Button illuminates when in the active state. Pressing any one of the buttons cancels or deactivates the other mode.

FREE RUN — Trace free runs.

INT — Sweep is triggered when noise level or modulation amplitude of a signal is ≥ 2.0 division. Triggering is checked near the end of this procedure.

LINE — Trace is triggered at power line frequency. Switch Triggering mode to LINE and note sweep is triggered.

EXT — The trace runs only when an external signal, ≥ 1.0 V peak, is applied to the back panel External HORIZ/TRIG connector. Since external test equipment is required to check this function, a check is not included at this time.

SINGLE SWEEP — When activated, single sweep aborts the current sweep; pressing the button again will arm the sweep generator and light the READY indicator. The indicator will remain lit until the sweep has run. When triggering conditions are met, after the circuit is armed, the analyzer will make only one sweep. Single sweep mode is canceled when any Triggering button is pressed. The effect of SINGLE SWEEP may be more apparent with digital storage off.

a. Press FREE RUN Triggering and set the TIME/DIV to 0.5 s.

b. Press SINGLE SWEEP and note that the sweep aborts.

c. Press SINGLE SWEEP again and note that the READY indicator lights and the sweep runs.

d. Press FREE RUN to cancel single sweep and return the TIME/DIV to AUTO position.

TIME/DIV — This control selects sweep rate, manual scan, and external sweep operation. In the MNL position, MANUAL SCAN control should move the crt beam across the full frequency span or horizontal axis of the crt graticule. In the EXT position a voltage of 0 to +10 V, applied to the rear panel HORIZ/TRIG connector, should deflect the crt beam across the full 10 division screen.

Vertical Display — Display modes are activated by three pushbuttons. Pressing any of these buttons cancels the other mode.

10 dB/DIV — When this button is activated, the display is a calibrated 10 dB/division with an 80 dB dynamic range.

(a) With a REF LEVEL of -20 dBm, activate 10 dB/DIV and AUTO RESOLN. Set the FREQ SPAN/DIV to 20 kHz and tune the calibrator signal to center screen.

(b) Change REF LEVEL and note that the display steps in one division increments, representing 10 dB/division. Return the REF LEVEL to -20 dBm.

2 dB/DIV — When this button is pressed, the display is a calibrated 2 dB/division with 16 dB of dynamic range.

(a) Activate the 2 dB/DIV mode and change the REF LEVEL to -6 dBm.

(b) Note that the display steps 1.0 division for each two steps of the REFERENCE LEVEL control.

(c) Return the REF LEVEL to -20 dBm.

LIN — When this button is activated, the display is linear between the reference level (top of graticule) and zero volt (bottom of graticule); the crt VERT DISPLAY reads out in volts/division.

Activate the LIN mode and note that the Vertical Display readout changes to 2.80 mV/division.

PULSE STRETCHER — When activated, the fall-time of video signals increases so narrow video pulses will show on the display. This function is checked later with external test equipment.

Video Filter — Two filters can be independently selected to provide, WIDE or NARROW (1/30th or 1/300th of the resolution bandwidth) filtering to average the noise.

(1) Change the FREQ SPAN/DIV to 500 kHz, activate 10 dB/DIV and AUTO RESOLN, and tune the calibrator signal to center screen.

(2) Activate WIDE and NARROW Video Filters and note the reduction in noise as each filter is switched in (see Figure 4-1). The NARROW filter will have a more pronounced effect on noise reduction. Also note the change in sweep rate, if the TIME/DIV selector is in the AUTO position.

(3) Switch both Video Filters off.

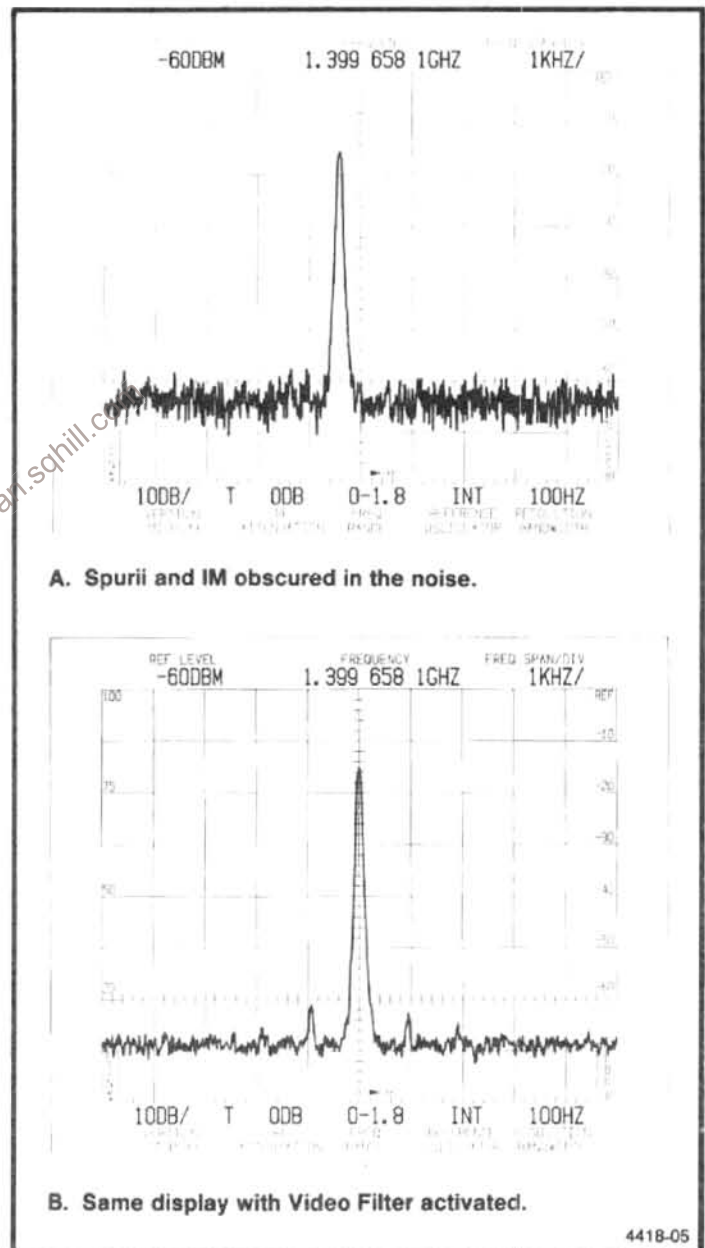


Figure 4-1. Video Filter effect on noise.

DIGITAL STORAGE — Either one or both the "A" and "B" waveforms, from digital storage, can be selected. The amplitude of a signal should remain constant when digital storage is switched on (VIEW A or VIEW B activated). The PEAK/AVERAGE control positions a cursor over the vertical window of the screen Noise and signal level will be averaged below the cursor and peaked above the cursor. Check operation according to the following description.

VIEW A — When pressed, the "A" waveform, from digital storage, is displayed. With SAVE A off, the "A" waveform is updated each sweep as the beam travels from left to right. With SAVE A on, the waveform and readout are not updated.

VIEW B — When activated, the "B" waveform is displayed. When both VIEW A and VIEW B are active, the "A" and "B" waveform are interlaced and displayed. Both waveforms are updated each sweep. Update of the "A" waveform depends on the state of SAVE A.

SAVE A — When activated, the "A" waveform, with its readout, is saved. In this mode the data for "A" waveform is not updated each sweep. Switch VIEW B off then change REF LEVEL and note that the "A" display does not change. The readout for the saved waveform will be displayed anytime SAVE A is on and VIEW B and B—SAVE A are off. If either VIEW B or B—SAVE A is on, the readout reflects current analyzer setup.

MAX HOLD — When on, the maximum signal amplitude at each memory location is stored. The waveform is updated only when signal data is greater than that previously stored. Verify operation by changing FREQUENCY or REF LEVEL and note that the maximum level at each location is retained.

B—SAVE A — The arithmetic difference between an updated "B" waveform and a SAVE A waveform is displayed. SAVE A function is also activated when B—SAVE A is pressed.

Press B—SAVE A then change the REF LEVEL so the difference between the "B" and SAVE A waveform is displayed with VIEW A and VIEW B off. The reference (zero difference) level is factory set at graticule center. The position of this reference level can be changed by qualified service personnel. Positive differences between the two displays appear above and negative differences below the line.

PEAK/AVERAGE — When digital storage is on, this control positions a horizontal line or cursor over the vertical graticule window. Signals above the cursor are peak detected, signals below the cursor are averaged by the digital storage. Verify operation by moving the cursor within the noise level and note the noise amplitude change as the cursor is positioned.

IDENTify — When the identify function is activated, every other sweep, with its waveform, is vertically displaced from the other. The frequencies of the 1st and 2nd local oscillators are moved such that true signals are not displaced horizontally on alternate sweeps while spurious signals are shifted 100 MHz or more, which is off screen for the narrower spans. The FREQ SPAN/DIV must be 50 kHz or less for the coaxial bands and 50 MHz or less for the waveguide bands (21 GHz or more) before the processor will activate the Identify mode.

(1) With the 500 MHz marker tuned to center frequency, decrease the FREQ SPAN/DIV to 50 kHz or less and press IDENT.

(2) Note that there is no horizontal displacement of the 500 MHz signal on alternate sweeps. To help determine if the signal is true or false, decrease the sweep rate or activate SAVE A, with both VIEW A and VIEW B on, so a comparison is easily observed (see Figure 4-2).

(3) Switch IDENT off.

AUTO RESOLN — When this function is on, resolution bandwidth automatically changes to maintain a calibrated display, as FREQ SPAN/DIV and TIME/DIV are changed. Check operation by changing FREQ SPAN/DIV or TIME/DIV settings and note the RESOLUTION BANDWIDTH change. UNCAL indicator should not light over the FREQ SPAN/DIV range if the TIME/DIV selector is in AUTO position.

MAX SPAN — When this function is activated, the span switches to maximum and the analyzer sweeps the full band. When deactivated, the span/div will return to its previous setting.

ZERO SPAN — When this button is activated, the span should shift to zero for a time-domain display. When deactivated, the span returns to its previous setting.

FREQUENCY SPAN/DIV — As this control is rotated, the Span/Div should change from Max to 0, counter clockwise from MAX position, in a 2, 1, 5 sequence. The display should indicate this change.

RESOLUTION BANDWIDTH — As this control is rotated from the 30 Hz position, the resolution bandwidth should change from 30 Hz to 100 Hz and then in decade steps to 1 MHz.

REFERENCE LEVEL — In the 10 dB/DIV Vertical Display mode, with FINE off, the REF LEVEL should step in 10 dB increments as the control is rotated. When FINE is activated, the steps are 1 dB. In the 2 dB/DIV mode, the

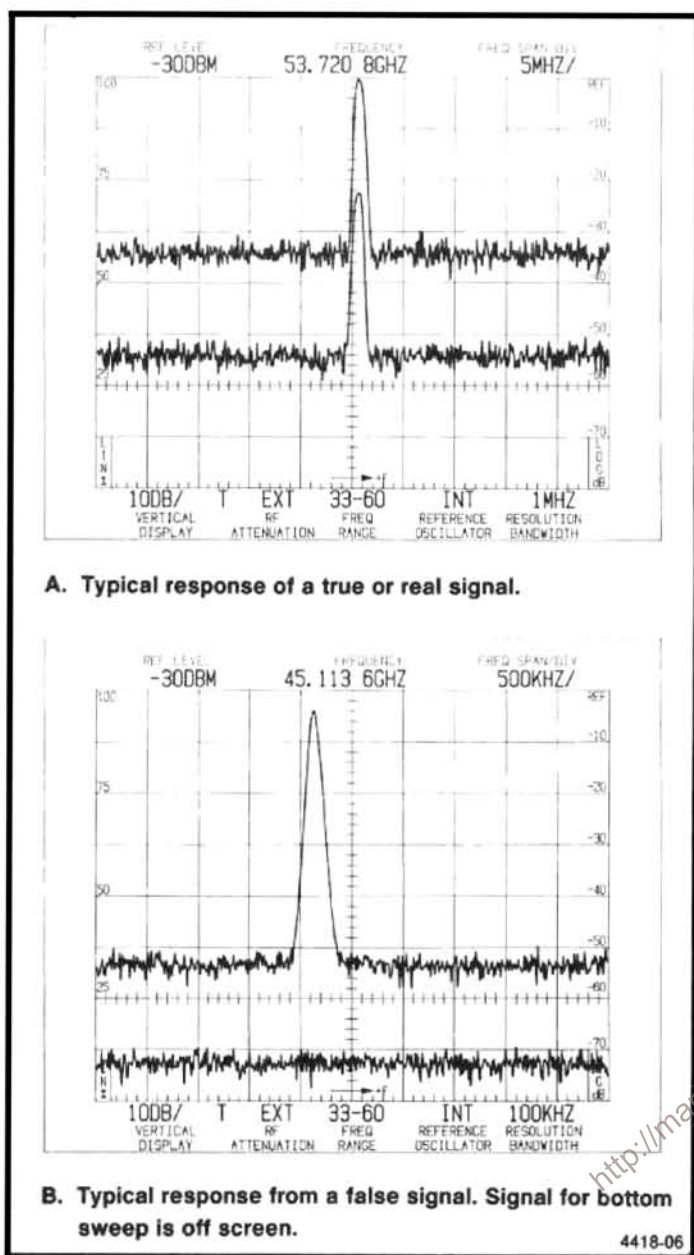


Figure 4-2. Typical display with SAVE A on to observe IDENTify mode.

steps are 1 dB, with FINE off, and 0.25 dB with FINE active. When the Vertical Display factor is 4 dB/div or less, with FINE on, the analyzer should switch to the delta A mode where the REF LEVEL readout goes to 0.00 dB then steps in 0.25 dB increments as the REFERENCE LEVEL control is rotated in a clockwise direction. Note, the REF LEVEL dB reading does not go above 0.00 dB if the control is rotated counterclockwise.

(1) Set the MIN RF ATTEN to 0 dB, Vertical Display to 10 dB/DIV, and rotate the REFERENCE LEVEL control counterclockwise to +30 dBm then clockwise to -110 dBm.

(2) Note that the REF LEVEL readout changes in 10 dB increments.

(3) Press FINE and rotate the REFERENCE LEVEL counterclockwise to -117 dBm. Note the REF LEVEL now steps in 1 dB increments.

(4) Press <SHIFT> REF LEVEL and select -30 dBm with the Data Entry keyboard, then press <SHIFT> dB/DIV and enter 4 dB, with the Data Entry keyboard. Press FINE and note that the REF LEVEL goes to 0.00 dB.

(5) Rotate the REFERENCE LEVEL control clockwise and note the REF LEVEL now steps in 0.25 dB increments from the 0.00 dB reference.

(6) Continue turning the control until the REF LEVEL reads -10 dBm then press 10 dB/DIV and deactivate FINE.

(7) Return the REF LEVEL to -20 dBm and note that 10 dB of RF ATTEN is switched in at a REF LEVEL of -20 dBm. This prevents signal compression of any signals whose amplitude is within the graticule area.

MIN RF ATTEN — This control sets the minimum amount of RF attenuation in the signal path, regardless of the REF LEVEL setting. Verify proper operation by setting the MIN RF ATTEN dB selector to 20 and change the REF LEVEL settings. Note that the RF ATTEN readout does not go below 20 dB.

FINE — When this button is activated, the REFERENCE LEVEL steps decrease to the Fine mode as described and checked under Reference Level.

MIN NOISE/MIN DISTORTION — This button selects one of two algorithms that select attenuator and IF gain. MIN NOISE (button illuminated) reduces the noise level by reducing the RF attenuation 10 dB and decreasing IF gain 10 dB. MIN DISTORTION reduces IM distortion due to input mixer overload. The normal mode of operation is with minimum distortion. To observe any change, the amount of RF ATTEN, displayed by the crt readout, must be 10 dB higher than the MIN RF ATTEN selector setting.

(1) Set the REF LEVEL to -20 dBm and the MIN RF ATTEN at 0 dB. Note that the RF ATTEN readout indicates 10 dB.

(2) Activate MIN NOISE and note that the noise floor drops approximately 10 dB and the RF ATTEN readout changes to 0 dB. Deactivate MIN NOISE mode.

UNCAL — This indicator lights when the display is uncalibrated.

(1) Set the TIME/DIV to 50 ms, deactivate the AUTO RESOLUTION, and set the RESOLUTION BANDWIDTH to 10 kHz.

(2) UNCAL indicator should light and remain lit until the FREQ SPAN/DIV is reduced to 200 kHz or the RESOLUTION BANDWIDTH is increased to 1 MHz.

(3) Return the TIME/DIV to AUTO, press AUTO RESOLN, and set the FREQ SPAN/DIV to 100 MHz.

SHIFT — Pressing this button shifts those pushbuttons with more than one function, to their secondary function. The function of this secondary mode is nomenclated in blue or orange lettering next to the pushbutton. The shift mode deactivates after the function has been performed. SHIFT is also used to abort from menus or other multi-key functions.

HELP — When activated, pressing or operating any control or selector produces a help message on the crt that explains the function. Help messages will also prompt the user to the next operational move or explain any error message that may appear. Activate this mode and press various buttons to observe the applicable crt messages. Press the button again to cancel. <SHIFT> HELP lists current errors.

RECALL SETTINGS/STORE — When pressed in the "Recall Settings" mode, this button will produce a listing of the memory registers and the center frequency of the setup stored. The 0 register retains the power-down settings. All can be recalled after power-up. In the <SHIFT> STORE mode, the existing front panel setup is stored in one of nine selected locations. A listing of all registers with the center frequency of the stored setup is displayed. A blank entry indicates no settings stored.

(1) Press <SHIFT> STORE, then select register number 1 to store the current front panel setup.

(2) Change front panel control and selector settings.

(3) Press RECALL and select the Data Entry key 1, to recall the setup.

(4) Note that the instrument front panel set-up returns to that previously entered.

COUNT/COUNT RESOLN — A count for any signal below the dot marker, that is 20 dB above the noise floor and no more than 60 dB down from the REF LEVEL, is made between each sweep with the counter on (button illuminated). The counted signal frequency appears in place of the center frequency. <SHIFT> COUNT RESOLN allows the selection of the counter resolution to 1 Hz, via the Data Entry keyboard.

(1) Set the FREQUENCY to 100 MHz. Establish a counter resolution of 100 Hz by pressing <SHIFT> COUNT RESOLN and enter 100 Hz, via the Data Entry keyboard.

(2) Tune to any signal that is 20 dB or more above the noise level and less than 60 dB down from the REF LEVEL. Activate COUNTER and note that the frequency readout has a resolution of 100 Hz.

ΔF — When the ΔF function is activated, center FREQUENCY readout initializes to 0.0 MHz or 0.00 kHz depending on the FREQ SPAN/DIV setting. The frequency difference to another point in the span can now be determined by tuning that point to center screen and noting the readout. Check, by measuring the difference between calibrator markers. If the frequency is tuned below "0.0" the readout will indicate (–) sign. Deactivate and note that the readout returns to the previous center FREQUENCY.

COUNT→CF — This button is used when a close-in analysis of a signal, in narrow spans, is desired. When this pushbutton is pressed, the signal under the frequency dot is counted once (even if the COUNTER mode is inactive) then the Center Frequency is shifted to the counted frequency. Any Freq Span/Div can now be selected and the signal will remain centered on screen. The count resolution and the resulting accuracy of the tuning is equal to the current counter resolution.

(1) Decrease the FREQ SPAN/DIV and increase the RESOLUTION BANDWIDTH so the calibrator signal spans 3 or 4 divisions on the screen. Tune the signal so approximately 20 dB of signal level, above the noise floor, is under the dot.

(2) Press COUNT→CF and note that the signal moves under the frequency dot and the FREQUENCY readout changes to indicated the frequency of the marker.

FREQUENCY RANGE — These pushbuttons shift the 494/494P frequency range up or down from the current band. Press first one and then the other and note that the frequency bands change accordingly. If the operator selects FREQUENCY via the Data Entry keyboard, the microprocessor will automatically select the appropriate frequency range.

AUTO PEAK/EXT MIXER — Selects Auto Peaking in its primary mode, and External Mixer in the shift mode. When AUTO PEAK is activated (button illuminated) one of two things occur:

(1) If the analyzer is operating in the preselector bands (1.7 - 21 GHz), the preselector initiates a peaking routine on any signal within the center two divisions of

the screen. The algorithm peaks the preselector tuning for this center frequency setting, then stores this setting in non-volatile (battery powered) memory. If a signal is not on screen, the algorithm will revert to the code that was previously stored in memory; or, if there is no setting, to the mid point of the peaking range. After a center frequency setting for a band has been stored, the operator can then switch back to this band with the assurance that the preselector is peaked well enough to track the oscillator and provide reasonable sensitivity.

(2) If the analyzer is operating in the External Mixer mode, the peaking routine sets the external mixer bias so the response is peaked. If a signal is not present, the algorithm reverts to the previous bias setting stored in memory or, if there is no previous setting, it sets the bias voltage mid range.

When <SHIFT> EXT MIXER is pressed, External Mixer operation is initiated, which dc couples the EXTERNAL MIXER port to an internal bias source for external mixers, and ac couples the IF return from the external mixer to the 2nd converter. This bias voltage is either manually set, with the MANUAL PEAK control, or automatically set by the Auto Peak algorithm. When in the External Mixer mode, the crt readout for RF ATTEN reads EXT. To exit this mode, press <SHIFT> EXT MIXER. The REF LEVEL will shift to +30 dBm and the RF ATTEN to 60 dB to protect the internal mixer from high level signals that might be applied to the RF INPUT.

a. Auto Peak

(1) With the Calibrator signal applied to the RF INPUT, select a frequency of 3.0 GHz, by pressing <SHIFT> FREQ then 3 GHz, via the Data Entry keyboard. Select a REF LEVEL of -40 dBm, a FREQ SPAN/DIV of 10 kHz, and a RESOLUTION BANDWIDTH of 1 kHz.

(2) Peak the 3.0 GHz signal with the MANUAL PEAK control.

(3) Press AUTO PEAK. Note the message "PEAKING" on screen and the READY indicator for SINGLE SWEEP mode flash as the processor runs the auto peak routine.

(4) When complete, the signal amplitude should equal or exceed that obtained with manual peaking.

(5) Change bands by increasing or decreasing the FREQUENCY RANGE, then return to band 2. Note that auto peak maintains the setting stored in memory.

b. External Mixer

(1) Press <SHIFT> EXT MIXER, the analyzer should shift to the External Mixer mode (indicated by a readout of EXT above RF ATTEN). If AUTO PEAK mode is still active the button will remain lit as it does not indicate external mixer but auto peak status.

(2) Connect a voltmeter between the EXTERNAL MIXER port and ground. Measure the bias voltage. If in the Auto Peak mode, the bias should be a steady dc voltage. (If Auto Peak has not been run for this band, the bias voltage will read approximately -0.8 V or mid range.)

(3) Switch to the manual peak mode by pressing AUTO PEAK again. The button should not be illuminated and the bias voltage at the EXTERNAL MIXER port should now vary between approximately -2.5 V to +1.0 V, as the MANUAL PEAK control is rotated through its range.

(4) Press <SHIFT> EXT MIXER to deactivate EXTERNAL MIXER mode.

Setting Parameters via the Data Entry Keyboard

(1) Set the FREQ SPAN/DIV to 50 kHz and switch AUTO RESOLN on. Set the center frequency to 2.0 GHz by pressing <SHIFT> FREQ, then enter 2 GHz via the Data Entry keyboard. Note that the FREQUENCY sets to 2.000 GHz. (The number of digits is a function of the span/div or the count resolution if the counter is on.

(2) Enter frequencies of 200 MHz, 200 kHz, and 200 Hz by repeating the above procedure. Note that the FREQUENCY sets to that entered via the Data Entry keyboard.

(3) Set the SPAN/DIV to some setting via the keyboard and note that the entered Span/Div is set.

(4) Enter a REF LEVEL with the keyboard and note that the entry is set.

(5) Enter a desired Vertical Display factor with the keyboard and note that the keyed-in dB/div is set.

STORE DISPLAY and RECALL

Pressing <SHIFT> STORE DISP starts a sequence to store, either the "A" or "B" waveform and its associated readout, in a numbered (0-8) memory register. This informa-

tion is retained in non-volatile memory so it can be recalled at a later time. Informative messages, displayed on the crt, aid the user in completing the multiple button sequence. First a list of the center frequencies of current stored displays is shown. The number of digits in the readout is an indication of the Span/Div of each stored display (a greater resolution indicates a narrower span). A register without an associated frequency is empty. This display includes a prompt for the register number into which the display will be stored. The register is selected, via the Data Entry keyboard, then a prompt asks which display ("A" or "B") to store in the selected register? Selection of the waveform completes the sequence and returns the instrument to normal operation.

To exit Store Display function press the <SHIFT> button. Pressing <SHIFT> RECALL recalls a selected waveform, with its readout, from memory, so it can be sent to the "A" or "B" part of digital storage. To see the display, activate the respective part of digital storage (VIEW A or VIEW B). The readout for the "A" waveform will only be shown if VIEW B and B—SAVE A are off, whereas the readout for a recalled "B" waveform will only be displayed if VIEW B or B—SAVE A are on. When RECALL is activated, SAVE A is also activated to protect the recalled waveform from overwrite if it is placed in "A" and to protect the current waveform if it is placed in "B". SINGLE SWEEP must be activated before a waveform is placed in "B", to prevent an overwrite by the next sweep. VIEW B must be activated to observe the recalled waveform in "B".

(1) Establish a display on the screen. Press <SHIFT> STORE DISPLAY then enter the memory register number (0-8) for the display and select display "A".

(2) Change the current display with the REF LEVEL or FREQUENCY control.

(3) Press <SHIFT> RECALL then select the register number that contains the above display (note the center frequency listing of the stored displays in each register). Press VIEW A and deactivate VIEW B.

(4) The recalled display, with its readout, should now become the "A" display. SAVE A should activate to save the display so the next sweep will not overwrite the recalled display. If VIEW B is on, both the recalled display (VIEW A) and the "B" display will be on screen. Since the most current display is the "B" waveform, the readout will depict the parameters for the "B" display. Switch VIEW B off so the readout will represent the recalled display.

(5) Activate SINGLE SWEEP then repeat part (3) except select "B" for the display. Activate VIEW B to view the recalled waveform.

(6) Repeat part (5) without activating SINGLE SWEEP and note that a message on screen warns that unless SINGLE SWEEP is on, the recalled display will be overwritten by the next sweep.

<SHIFT> PLOT (494P only)

When the 494P is connected to a plotter over the GPIB cable, pressing <SHIFT> PLOT will send the digital storage waveform(s) that are displayed, as well as the graticule and bezel (if GRAT ILLUM is on), and the crt readout (if READOUT is on) to the plotter.

To use or check the plot feature, connect the Digital Plotter to the 494P with a IEEE STD 488 (GPIB) cable and perform the following:

(1) Set the corners of the plot for a 3:2 aspect ratio for Tektronix plotters, or 6:5 for the Hewlett-Packard plotter. The Digital Plotter must be in the Listen Only mode and the 494P must be in either the TALK ONLY or TALK/LISTEN ONLY mode (appropriate switches on the rear panel GPIB ADDRESS switch, closed or in the 1 position).

(2) Set the Plotter Interface switches as follows:

TEKTRONIX 4662 or 4662 Option 31 (rear panel)

- A = 0, 1, 8, or 9
- B = C or D
- C = X (don't care)
- D = X (don't care)

TEKTRONIX 4663

- Interface Select = 1 if Option 04 or 2 if Option 01
- Initial Command/Response Format = 5
- Interface Mode = Listen Only

HEWLETT-PACKARD

Address = 31

(3) Select the plotter type by pressing <SHIFT> SAVE A, on the 494/494P, and answer the type plotter question on the crt message. The selection is stored in battery-powered memory and need not be selected again unless the type plotter is changed. To use a 4663 emulating a 4662, select 0 (4662) for a one-pen configuration or select 1 (4662 Option 31) for a two pen configuration. Select the display and the information that you wish to plot.

The zero level for a B—SAVE A waveform is assumed to be the graticule center line. (Switches within the instrument can set the zero level, contact your service

personnel for this change.) If you desire to shift the zero level for the PLOT only, press <SHIFT>, B—SAVE A, and enter the desired level in display units (25 is bottom graticule line, 25 units/div is required). This zero level is retained in non-volatile memory; however, it is not related to the display zero level since the processor has no way of determining the internally set zero level for the crt display or no way of changing it.

(4) Press <SHIFT> PLOT. During the plot operation, the front panel controls are operational except STORE DISP, RECALL, and AUTO PEAK; so the instrument can be used for other measurements.

This completes the operational check of the front panel controls and selectors.

2. Check Reference Oscillator Accuracy

Reference oscillator accuracy is not a performance requirement; however, it must be checked so the center frequency accuracy can be verified. Since the Calibrator is locked to the reference oscillator this procedure verifies accuracy by counting the frequency of the calibrator signal. Allow 30 minutes or more warm-up time for the oscillator to stabilize before proceeding with this check.

a. Connect the counter to the CAL OUT. Set the counter display resolution to 1 Hz.

b. Check — Frequency of the calibrator must be $100 \text{ MHz} \pm 10 \text{ Hz}$.

c. Disconnect the counter from the CAL OUT connector.

3. Check Counter Accuracy $\pm[(10 + 2N)\text{Hz} + 1\text{LSD}]$

a. Set the FREQUENCY to 500 MHz and the FREQ SPAN/DIV to 20 kHz, via the Data Entry keyboard. Activate 10 dB/DIV Vertical Display, set the TIME/DIV to AUTO, REF LEVEL -30 dBm, and activate AUTO RESOLN.

b. Apply the CAL OUT signal to the RF INPUT and center the 500 MHz marker under the dot marker.

c. Press <SHIFT> COUNT RESOLN and enter 1 Hz via the Data Entry keyboard.

d. Press COUNTER and note that the error over several counts does not exceed 13 Hz.

e. Change FREQ SPAN/DIV to 500 kHz and repeat part d.

f. Press <SHIFT> COUNT RESOLN and enter 1 kHz for a counter resolution of 1 kHz.

g. Press COUNTER and note that the error over several counts does not exceed 1 kHz.

h. Change the FREQ SPAN/DIV to 200 kHz and repeat part g.

i. Set the FREQUENCY to 1.8 or 1.7 GHz and repeat the counter accuracy check for this end of the band.

4. Check Counter Sensitivity

Counter should count a signal that is 20 dB above the noise floor and above a level that is 60 dB down from the REF LEVEL.

a. Test equipment setup is shown in Figure 4-3. Apply the CAL OUT signal through 1 dB and 10 dB step attenuators to the RF INPUT.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 1 MHz, RESOLUTION BANDWIDTH to 1 MHz, REF LEVEL to 0 dBm, and activate NARROW Video Filter.

c. Adjust CENTER FREQUENCY to position the peak of the 100 MHz signal directly below the dot marker. Add attenuation to reduce the signal amplitude until it is 20 dB above the noise floor.

d. Press <SHIFT> COUNT RESOLN and enter 1 Hz via the Data Entry keyboard.

e. Press COUNTER and note that the counter is counting the signal with the accuracy noted in step 3.

f. Change FREQ SPAN/DIV and RESOLUTION BANDWIDTH to 100 Hz, REF LEVEL to -30 dBm, and activate WIDE Video Filter.

g. Increase the attenuation until the signal amplitude decreases to a level that is 60 dB below the REF LEVEL and adjust CENTER FREQUENCY to place the signal directly under the dot marker.

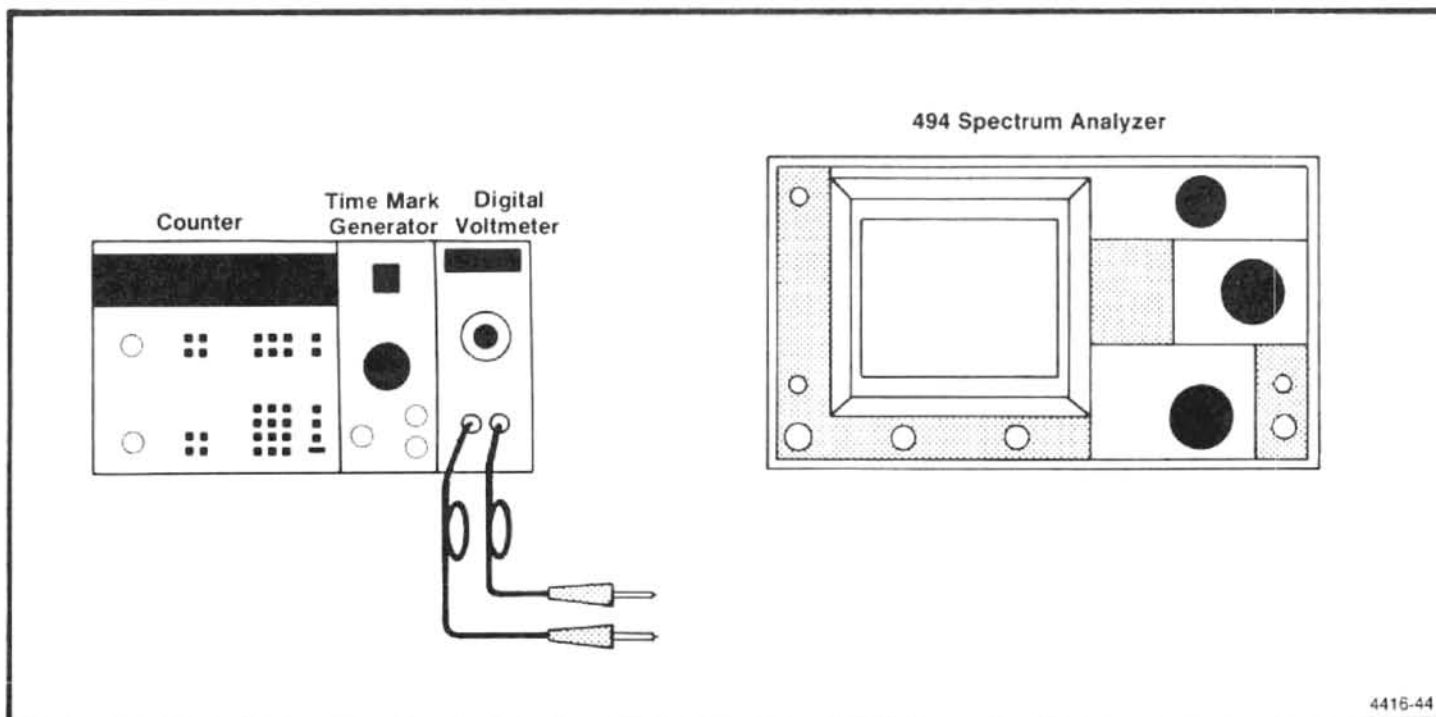


Figure 4-3. Test equipment setup for checking center frequency accuracy.

h. Press COUNTER and note that the counter is counting the signal and the count is accurate.

i. Deactivate COUNTER and WIDE Video Filter. Activate AUTO RESOLN and switch FREQ SPAN/DIV to 200 kHz.

5. Check Center Frequency Accuracy

This is a two part procedure; part 1 checks center frequency accuracy without the 1st LO phase locked, part 2 checks accuracy with the 1st LO phase locked. A front panel CAL should be done before performing this check.

Center frequency accuracy is a function of how accurate the center frequency is set between sweeps and the amount of frequency drift during the sweep. Frequency drift can be significant during the first 30 minutes after turn-on or when the ambient temperature changes. With a span/div of 50 Hz and 30 Hz resolution bandwidth, the sweep rate is slow enough that frequency drift can be noted if the warmup time is insufficient or the ambient temperature is changing. "N" is the 1st LO harmonic number used for the first conversion (refer to IF Frequency, LO Range, and Harmonic Number, in Specifications section for value of N, or activate the HELP message for the (down) FREQUENCY RANGE).

This check is dependent on the performance of the reference oscillator and the counter accuracy (see steps 2 and 3).

Part 1 — 1st LO not phase locked

Accuracy for bands 1 & 5-12 with Span/Div >200 kHz, and bands 2-4 with Span/Div >100 kHz: $\pm[(20\% \text{ of the Span/Div or Resoln Bandwidth, whichever is greater}) + (CF \times \text{reference frequency error}) + (N \times 15 \text{ kHz})]$ A settling time of 1 s/GHz change in center frequency divided by "N" must be allowed before checking accuracy. A front panel CAL should be done before proceeding with this check.

(1) Equipment setup is shown in Figure 4-3

(2) Apply the output of the comb generator to the RF INPUT. Set the FREQUENCY to 500 MHz and the FREQ SPAN/DIV to 210 kHz, via the Data Entry keyboard. Activate AUTO RESOLN, 10 dB/DIV, and set REF LEVEL to +20 dBm

(3) Press COUNT→CF and change the RESOLUTION BANDWIDTH to 10 kHz.

(4) Note that the signal is within $\pm[(20\% \text{ of Span/Div or Resoln Bandwidth}) + (N \times 15 \text{ kHz})]$ or $\pm 57 \text{ kHz}$ (± 1.35 minor div) of the dot marker.

(5) Set the FREQUENCY to 1.0 GHz and RESOLUTION BANDWIDTH to 1 MHz.

(6) Press COUNT→CF and change the RESOLUTION BANDWIDTH to 10 kHz.

(7) Check — that the signal is within 57 kHz of the dot marker.

(8) Repeat the procedure to check accuracy at a center frequency of 1.5 GHz (the upper end of band 1).

(9) Using the above procedure and Table 4-2, check center frequency accuracy to 21 GHz for those span/div settings in which the 1st LO is not phase locked.

(3) Repeat this procedure to check the center frequency accuracy to 1.8 GHz in 100 MHz increments. Adjust the REF LEVEL as necessary to observe the comb of 100 MHz markers at the upper end of the range.

Part 2 — 1st LO phase locked

Accuracy for bands 1 & 5-12 with Span/Div ≤ 200 kHz and bands 2-4 with Span/Div ≤ 100 kHz: $\pm [(20\% \text{ of the Span/Div or Resoln Bandwidth, whichever is greater}) + (\text{CF} \times \text{reference frequency error}) + (2N + 25)]\text{Hz}$.

(1) Apply the CAL OUT signal to the RF INPUT. Press <SHIFT> FREQ and enter 100 MHz via the Data Entry keyboard. Set FREQ SPAN/DIV to 50 Hz and the REF LEVEL to -20 dBm. Activate AUTO RESOLN and 2 dB/DIV, then adjust the REFERENCE LEVEL so the top of the signal is below the dot marker.

(2) Check 100 MHz center frequency accuracy by measuring the deviation of the 100 MHz signal from the dot marker. Error must not exceed $\pm(20\% \text{ of the span/Div}) + (25 + 2N)$ or ± 37 Hz (± 3.7 minor division).

6. Check Center Frequency Drift or Stability

Drift is 50 Hz or less per minute of sweep time, with 1st LO phase locked (FREQ SPAN/DIV 200 kHz or less for bands 1 & 5-12 and 100 kHz or less for bands 2-4) — after 1 hour of warmup, and within a stable ambient temperature.

a. With the Calibrator signal applied to the RF INPUT, set the FREQUENCY to 100 MHz, TIME/DIV to AUTO, FREQ SPAN/DIV at 50 Hz, RESOLUTION BANDWIDTH at 30 HZ, Vertical Display of 2 dB/DIV, and REF LEVEL of -23 dBm. Switch VIEW A and VIEW B on.

b. Adjust the CENTER FREQUENCY control so one side of the signal intersects the sixth division graticule line, from the left edge, then press SINGLE SWEEP. Activate SAVE A to save the display.

Table 4-2
CENTER FREQUENCY ACCURACY CHECK POINTS
FOR UNLOCKED 1st LO

Band	N	Center Freq	Freq Span/Div	Maximum Error	Error Minor Div
1	1	0.5 GHz	210 kHz	± 57 kHz	± 1.35
		1.0 GHz	210 kHz	± 57 kHz	± 1.35
		1.5GHz	210 kHz	± 57 kHz	± 1.35
2	1	2.0 GHz	110 kHz	± 37 kHz	± 1.35
		3.0GHz	110 kHz	± 37 kHz	± 1.35
		4.0 GHz	110 kHz	± 37 kHz	± 1.35
		5.0GHz	110 kHz	± 37 kHz	± 1.35
3	1	6.0 GHz	110 kHz	± 37 kHz	± 1.35
		6.5GHz	110 kHz	± 37 kHz	± 1.35
		7.0 GHz	110 kHz	± 37 kHz	± 1.35
4	3	7.5 GHz	110 kHz	± 67 kHz	± 1.35
		9.5 GHz	110 kHz	± 67 kHz	± 1.35
		11.5GHz	110 kHz	± 67 kHz	± 1.35
		13.5 GHz	110 kHz	± 67 kHz	± 1.35
		15.5GHz	110 kHz	± 67 kHz	± 1.35
		17.5 GHz	110 kHz	± 67 kHz	± 1.35
		18.0GHz	110 kHz	± 67 kHz	± 1.35
5	3	18.5 GHz	210 kHz	± 87 kHz	± 1.35
		20.0GHz	210 kHz	± 87 kHz	± 1.35
		21.0 GHz	210 kHz	± 87 kHz	± 1.35

c. Select the NARROW Video Filter and press SINGLE SWEEP again to start the sweep. The sweep will now run at a 10 s/div rate.

d. Note the frequency difference between the two displays, at the 6th graticule line as Δf .

e. Check — the frequency drift rate/minute. Drift is $(300 \times \Delta f) / (250 + \Delta f)$ per minute. Drift rate must not exceed 50 Hz/min.

7. Check Residual FM

Within $(7 \text{ kHz})N$ over 20 ms, with FREQ SPAN/DIV greater than 200 kHz, and within $(10 + 2 N)$ Hz over 20 ms, with FREQ SPAN/DIV of 200 kHz or less)

a. With the Calibrator signal applied to the RF INPUT, set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 1 MHz, RESOLUTION BANDWIDTH to 100 kHz, Vertical Display to 2 dB/DIV, and REF LEVEL to -23 dBm.

b. Press <SHIFT> FREE RUN. A message "FREQUENCY CORRECTIONS DISABLED" will come on screen, which indicates that the 1st LO synthesis and phase lock are disabled; this is normal. It is now possible to switch the FREQ SPAN/DIV to narrower spans with phase lock disabled.

c. Decrease the FREQ SPAN/DIV and RESOLUTION BANDWIDTH to 100 kHz and keep the 100 MHz calibrator signal centered on screen with the CENTER FREQUENCY control.

d. Switch the Vertical Display to LIN. Position the signal so the slope (horizontal versus vertical excursion) of the response can be determined as illustrated in Figure 4-4A. It may help to determine slope by switching VIEW B off and using SAVE A and VIEW A to freeze the display at a convenient point on the graticule for measurement. Slope should calculate to approximately 8 kHz/division.

e. If SAVE A was used in step d, de-activate SAVE A and VIEW B. Activate ZERO SPAN, set TIME/DIV to 20 ms, and adjust CENTER FREQUENCY control to position the display near center screen as shown in Figure 4-4B. Use SAVE A to freeze the display for ease in measuring the FM. The peak-to-peak amplitude of the display per any horizontal division, scaled to the vertical deflections according to the slope estimated in part d is the FM. Residual FM must not exceed 7 kHz for 20 ms or 7 kHz/division.

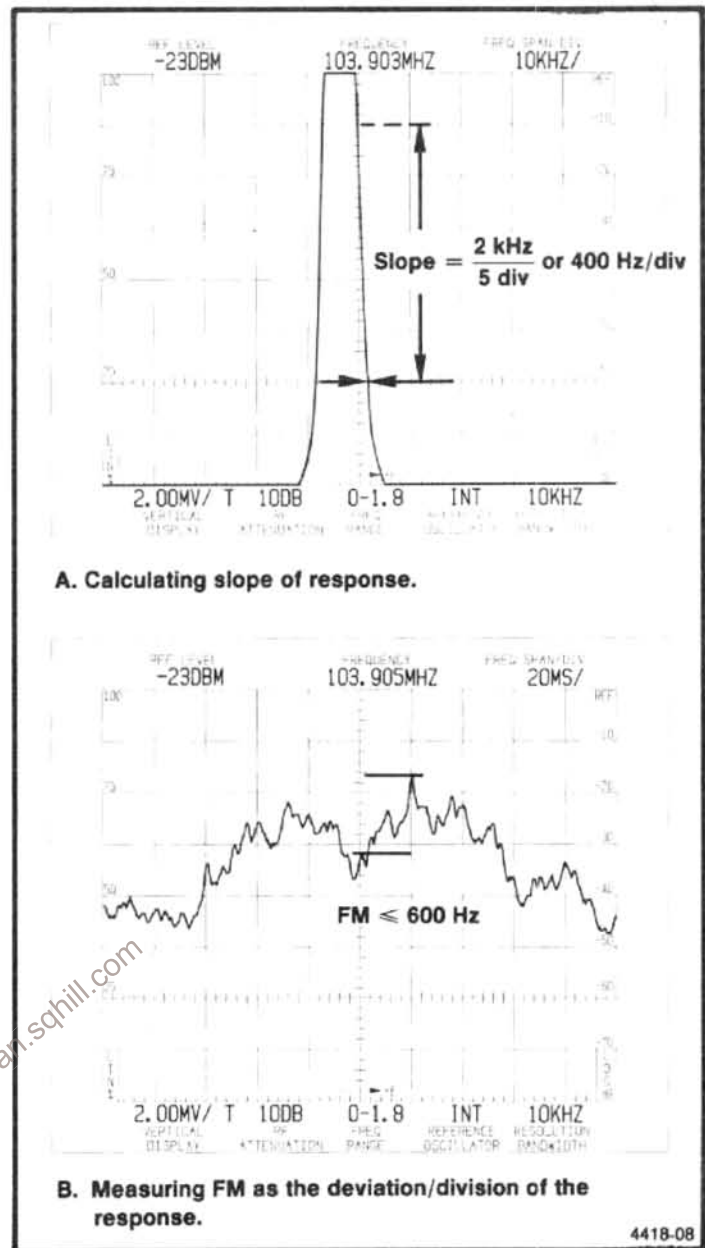


Figure 4-4. Typical display that illustrates how residual FM is measured.

f. Press <SHIFT> FREE RUN to re-enable the phase lock, set the FREQUENCY to 100 MHz and switch the TIME/DIV to AUTO. Reduce the FREQ SPAN/DIV and RESOLUTION BANDWIDTH to 100 Hz.

g. Adjust the CENTER FREQUENCY control to position the signal so its slope can be determined. Again, it will be easier if you use SINGLE SWEEP and SAVE A to freeze the display at a convenient position on the graticule.

h. Deactivate SAVE A and SINGLE SWEEP and switch the TIME/DIV to 20 ms. Activate ZERO SPAN and position the display near center screen so the vertical excursions per horizontal division (20 ms) can be measured. Residual FM must not exceed 12 Hz within any one horizontal division.

8. Check Frequency Span/Div Accuracy $\pm 5\%$ of the selected span/div

Span accuracy is checked by noting the displacement of calibrated markers from their respective graticule line over the center eight divisions of the screen. The frequency span/div accuracy is checked, for all FREQ SPAN/DIV settings on band 1, at 100 kHz/Div on band 2, (2nd LO check) and at 500 MHz/Div on band 4. The accuracy of the 1 GHz, 5 GHz, and 10 GHz span/div selections, for the upper bands, is directly related to the 100 MHz/div and 200 MHz/div selections: therefore, they are not included in this procedure.

FREQUENCY SPAN/DIV range is 50 Hz to 200 MHz for the 0 to 7.1 GHz bands, increasing in a 5, 1, 2, 5 sequence to 10 GHz for bands 11 and 12. Selection is in a 5, 2, 1 sequence with the FREQUENCY SPAN/DIV control and by two significant digits with the Data Entry keyboard.

a. Equipment setup is shown in Figure 4-5.

b. Set the FREQUENCY to 1 GHz, FREQ SPAN/DIV to 200 MHz, RESOLUTION BANDWIDTH to 1 MHz, TIME/DIV at 0.5 s, REF LEVEL to -30 dBm, and Vertical Display to 10 dB/DIV.

c. Apply the CAL OUT signal to the RF INPUT and adjust the FREQUENCY to align the 100 MHz markers so the 200 MHz/div accuracy can be measured over the center eight divisions of the display (two markers per division). It may be necessary to change the REF LEVEL to obtain adequate markers. Maximum deviation (see Figure 4-6) must not exceed 10 MHz (0.25 minor divisions).

d. Change the FREQ SPAN/DIV to 100 MHz and check the span/div accuracy. Error must not exceed 5% of the FREQ SPAN/DIV or 5 MHz.

e. Remove the CAL OUT signal to the RF INPUT and apply the output of the Microwave Comb Generator, as shown in Figure 4-5. Set the FREQUENCY to 10 GHz, (band 4, 5.4 to 18 GHz) FREQ SPAN/DIV to 500 MHz, RESOLUTION BANDWIDTH to 100 kHz, and REF LEVEL to -10 dBm. Peak the response with the MANUAL PEAK control and adjust REF LEVEL for the best marker definition. It may also help to adjust the CENTER FREQUENCY for better marker definition.

f. Tune a marker to center screen then check the accuracy over the center eight divisions of the display. Deviation must not exceed ± 25 MHz.

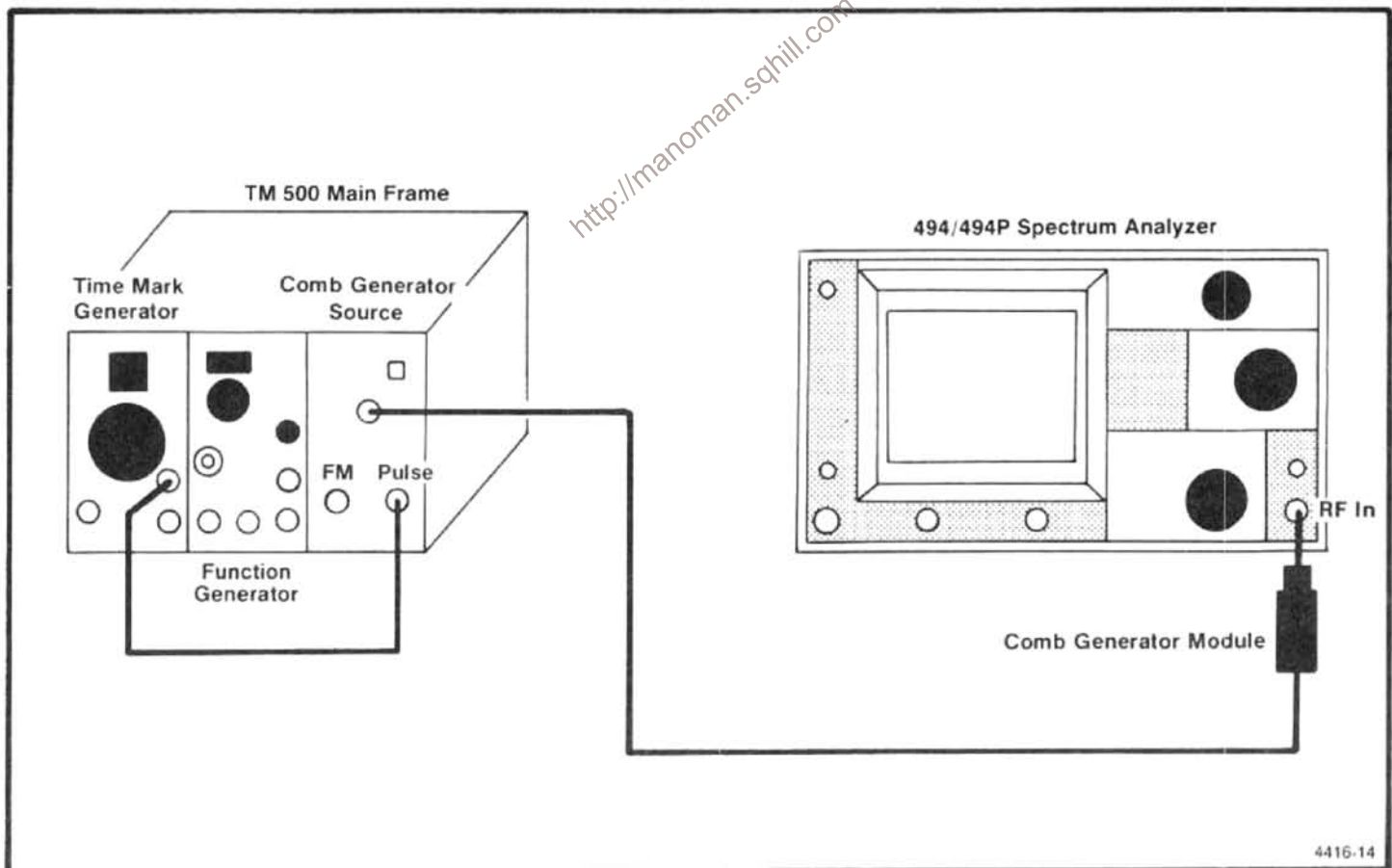


Figure 4-5. Test equipment setup for checking frequency span/div and sweep time/div accuracy.

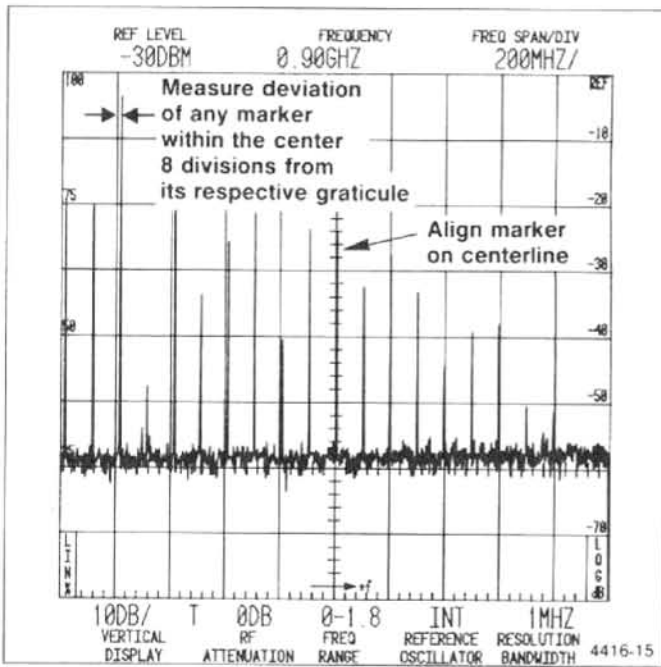


Figure 4-6. Typical marker display that shows how span/div accuracy is measured.

g. Set the FREQUENCY to 2.0 GHz, FREQ SPAN/DIV to 100 kHz, RESOLUTION BANDWIDTH to 1 kHz, TIME/DIV to 50 ms, and REF LEVEL to -20 dBm.

h. Modulate the Comb Generator signal with 10 μs markers, from the Time Mark Generator, by applying the Marker Output to the Pulse Input of the Comb Generator as shown in Figure 4-5. Adjust the MANUAL PEAK control for optimum marker definition.

i. Check FREQ SPAN/DIV accuracy. Error must not exceed ± 5 kHz.

j. Remove the Comb Generator signal from the RF INPUT and connect the Marker Output of the Time Mark Generator to the RF INPUT. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 50 MHz, RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to +20 dBm, and apply 20 ns time markers from the Time Mark Generator.

k. Adjust the REF LEVEL for the best marker definition and the CENTER FREQUENCY to align the markers so span/div accuracy can be checked for the 50 MHz/div.

l. Reduce the FREQ SPAN/DIV to 20 MHz, CENTER FREQUENCY to 100 MHz, and apply 50 ns (20 MHz) markers.

m. Check the 20 MHz FREQ SPAN/DIV accuracy.

n. Repeat the procedure and check the FREQ SPAN/DIV accuracy from 10 MHz down to 200 kHz. Use Table 4-3 as a guide to relate time markers to FREQ SPAN/DIV settings. Reduce RESOLUTION BANDWIDTH and CENTER FREQUENCY as each setting is checked to maintain marker amplitude and definition.

o. Change the TIME/DIV to 0.5 s and RESOLUTION BANDWIDTH to 100 Hz. Repeat the above procedure to check the 100 kHz to 10 kHz FREQ SPAN/DIV selections.

p. Set the FREQUENCY to 100 kHz, RESOLUTION BANDWIDTH to 30 Hz, TIME/DIV to 1 s and REF LEVEL to 0 dBm. Repeat the above procedure to check the 5 kHz to 200 Hz FREQ SPAN/DIV selections.

q. Activate the 2 dB/DIV Vertical Display mode, increase REF LEVEL to approximately -28 dBm. Repeat the procedure to check the 100 Hz and 50 Hz FREQ SPAN/DIV selections.

Table 4-3
SPAN/DIV VERSUS TIME MARKERS FOR
SPAN/DIV ACCURACY CHECK

FREQUENCY SPAN/DIV	Time Mark Generator Marker Output
20 MHz	50 ns
10 MHz	. 1 μs
5 MHz	. 2 μs
2 MHz	. 5 μs
1 MHz	1 μs
500 kHz	2 μs
200 kHz	5 μs
100 kHz	10 μs
50 kHz	20 μs
20 kHz	50 μs
10 kHz	. 1 ms
5 kHz	. 2 ms
2 kHz	. 5 ms
1 kHz	1 ms
500 Hz	2 ms
200 Hz	5 ms
100 Hz	10 ms
50 Hz	20 ms

9. Check Time/Div Accuracy (accuracy within 5% of time selected)

a. Test equipment setup is the same as that required for step 8.

b. Apply the Marker Output from the Time Mark Generator directly to the RF INPUT. Apply the Trigger Output to the 494/494P HORIZ/TRIG connector on the back panel.

c. Activate ZERO SPAN. Set the RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL at 0 dBm, TIME/DIV to 50 ms, MIN RF ATTEN to 20 dB, FREQUENCY to 1 MHz and the Triggering mode to EXT.

d. Apply 50 ms time markers. Adjust CENTER FREQUENCY, if necessary, to display the markers on the time domain display (see Figure 4-7).

e. Use the horizontal position control to align a marker on the 1st graticule line, then check the displacement of markers from their respective positions over the center eight divisions. Individual marker displacement must not exceed 5% or 2 minor divisions.

f. Check the accuracy of the 50 ms to 2 ms TIME/DIV settings, then the position and note the displacement as described in part "e" of this step.

g. Deactivate the VIEW A and VIEW B mode. Change the RESOLUTION BANDWIDTH to 100 kHz, the Vertical Display to 2 dB/DIV, and the REF LEVEL to -10 dBm.

h. Check the accuracy of the 1 ms to 20 μ s TIME/DIV selections.

10. Check Pulse Stretcher

This is an operational check only.

a. With the equipment setup the same as step 9, apply 1 ms time marks, from the Time Mark Generator, to the RF INPUT. Set the TIME/DIV to 0.1 ms, RESOLUTION BANDWIDTH to 100 kHz, Vertical Display to 10 dB/DIV, and REF LEVEL to 0 dBm. Set the FREQUENCY to 2.0 MHz, switch VIEW A and VIEW B off, and activate ZERO SPAN.

b. Activate PULSE STRETCHER and note that this mode extends the fall-time of the markers.

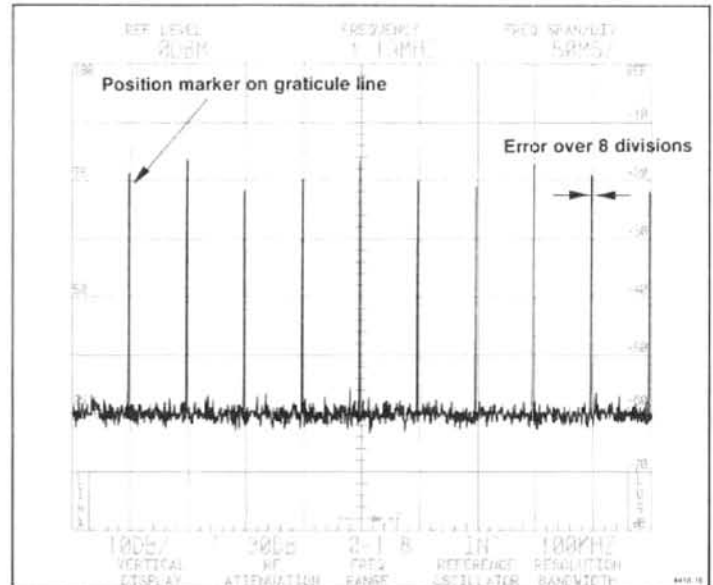


Figure 4-7. Typical display to illustrate how time/div accuracy is measured.

c. Remove the Time Mark Generator outputs to the RF INPUT and HORIZ/TRIG inputs of the 494/494P. Deactivate PULSE STRETCHER, ZERO SPAN and return the MIN RF ATTEN to 0 dB.

11. Check Resolution Bandwidth and Shape Factor

Bandwidth is within 20% of the 1 MHz to 30 Hz range, in decade steps to 100 Hz, then 30 Hz; shape factor is 7.5:1 or less to 100 Hz, and 15:1 or less for the 30 Hz bandwidth.

a. With the Calibrator output applied to the RF INPUT and the FREQUENCY set to 100 MHz, set the REF LEVEL to -20 dBm, FREQ SPAN/DIV to 500 kHz, RESOLUTION BANDWIDTH to 1 MHz, TIME/DIV at AUTO, and Vertical Display to 2 dB/DIV. Activate MIN NOISE.

b. Measure the 6 dB down bandwidth (see Figure 4-8A). Bandwidth should equal 1 MHz \pm 200 kHz.

c. Change the Vertical Display to 10 dB/DIV and measure the 60 dB down bandwidth (see Figure 4-8B).

d. Calculate the shape factor as the ratio of -60 dB/-6 dB bandwidths (see Figure 4-8). Shape factor should equal 7.5:1 or less.

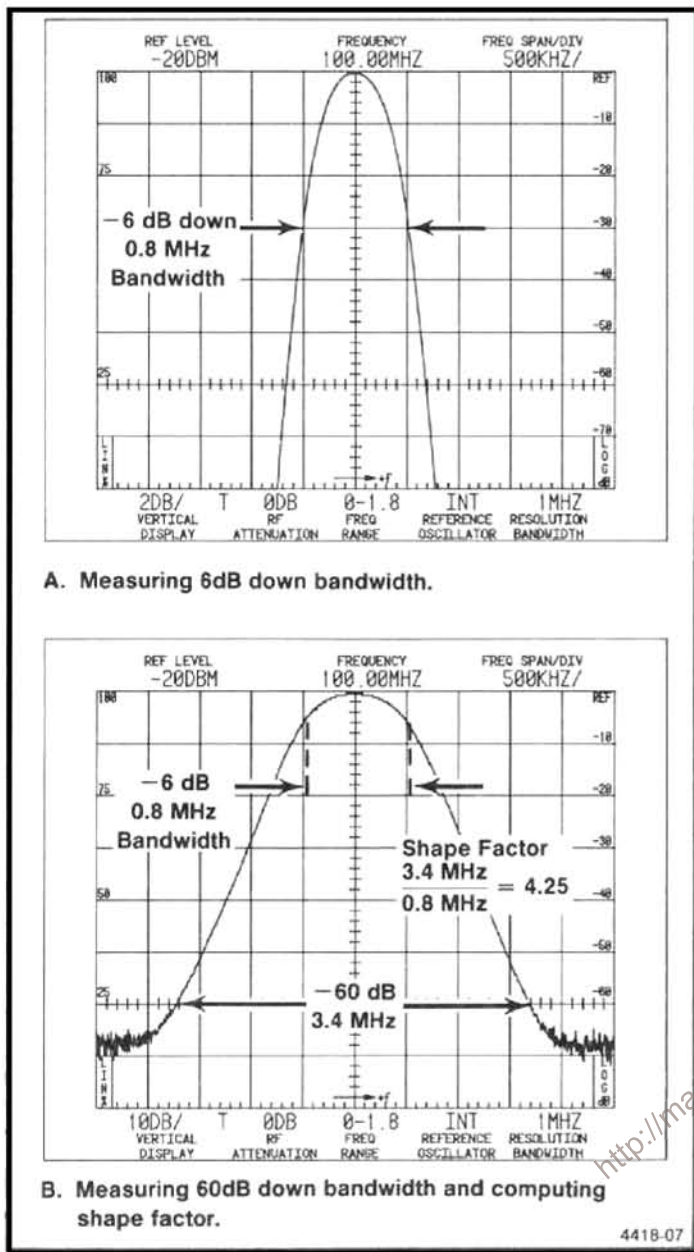


Figure 4-8. Typical display to illustrate how response bandwidth and shape factor are determined.

- e. Change the RESOLUTION BANDWIDTH to 100 kHz and the FREQ SPAN/DIV to 100 kHz.
- f. Check the resolution bandwidth and shape factor of the 100 kHz filter by repeating the above process.
- g. Repeat the process to check the resolution bandwidth and shape factor for the 10 kHz, 1 kHz, 100 Hz, and 30 Hz filters. Shape factor should equal 7.5:1 for all except the 30 Hz filter which is 15:1 or less.

NOTE

Because of residual FM'ing $(10 + 2N)Hz$ in 20 ms, The bandwidth of the 30 Hz filter cannot be measured to $\pm 20\%$ with the above procedure; and additional 12 Hz error must be included with the specification.

12. Check Noise Sidebands

Noise sidebands are -75 dBc or more at 30 times the resolution bandwidth offset, fundamental mixing; and -70 dBc or more for 100 Hz or less resolution bandwidths.

- a. Set FREQUENCY to 100 MHz, FREQ SPAN/DIV to 10 kHz, and REF LEVEL to -20 dBm. Activate 10 dB/DIV, AUTO RESOLN, and WIDE Video Filter.
- b. Apply the CAL OUT signal to the RF INPUT. Change REF LEVEL to -40 dBm to position the signal peak 20 dB above the reference line.
- c. Check the amplitude of the noise sidebands 30 times the resolution bandwidth away from the signal (Figure 4-9). Noise sidebands should be 75 dB or more below the peak signal level or 55 dB below the top of the screen.
- d. Decrease the FREQ SPAN/DIV to 1 kHz and the RESOLUTION BANDWIDTH to 100 Hz.

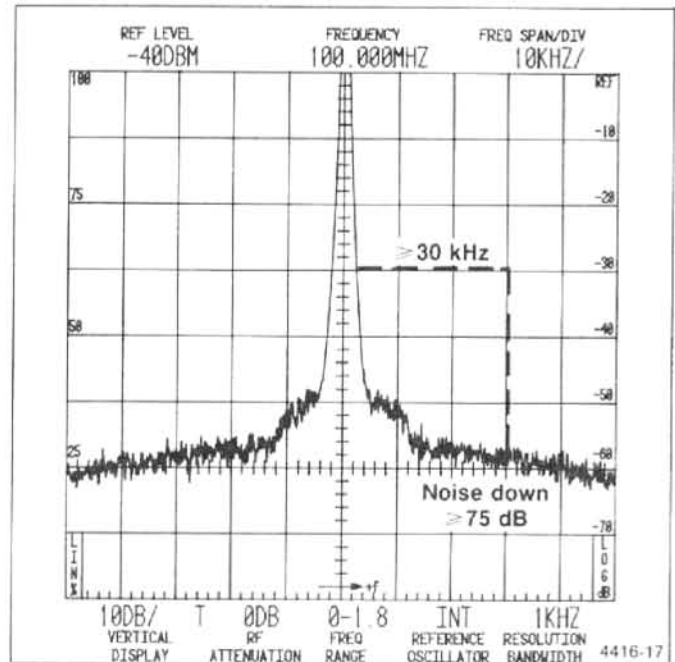


Figure 4-9. Typical display showing how to measure noise sidebands.

e. Check the amplitude of the noise sidebands 3 kHz away from the signal. Noise sidebands should be 70 dB below the signal level or 50 dB below the top of the screen.

13. Check Calibrator Output $-20\text{ dBm} \pm 0.3\text{ dB}$ at 100 MHz

Three procedures for measuring output level are described: vector voltmeter, power meter, and comparison between an accurate -20 dBm source and the Calibrator output.

Vector Voltmeter Method

- (1) Test equipment setup is shown in Figure 4-10.
- (2) Terminate the voltmeter probe with a $50\ \Omega$ feed-through termination and then connect the terminated probe to the CAL OUT connector
- (3) Set the vector voltmeter frequency to 100 MHz.
- (4) Check - for an rms reading between 21.11 mV and 22.69 mV. (22.36 mV rms, across $50\ \Omega$, is -20 dBm .)

Power Meter Measurement

- (1) Test equipment setup is shown in Figure 4-10.

- (2) Connect the power meter sensor through a low-pass filter ($\geq 40\text{ dB}$, at 200 MHz, to remove harmonics of the fundamental) to the CAL OUT connector.

NOTE

Insertion loss of the filter with pads, measured at 100 MHz, must be determined to within 0.05 dB. To ensure a $50\ \Omega$ match, use approximately 3 dB minimum-loss matching pads (attenuator) on both sides of the filter.

- (3) Note the power reading. Reading, plus the loss through the filter and pads, must equal -20 dBm , $\pm 0.3\text{ dB}$.

Signal Substitution Method

NOTE

A power meter is used to verify the output level of the reference signal. Harmonics of the signal source must be greater than 40 dB down.

- (1) Apply a 100 MHz signal from a signal source (signal generator) through a 3 dB attenuator to the power meter. Adjust the output level for -20 dBm reading on the power meter.

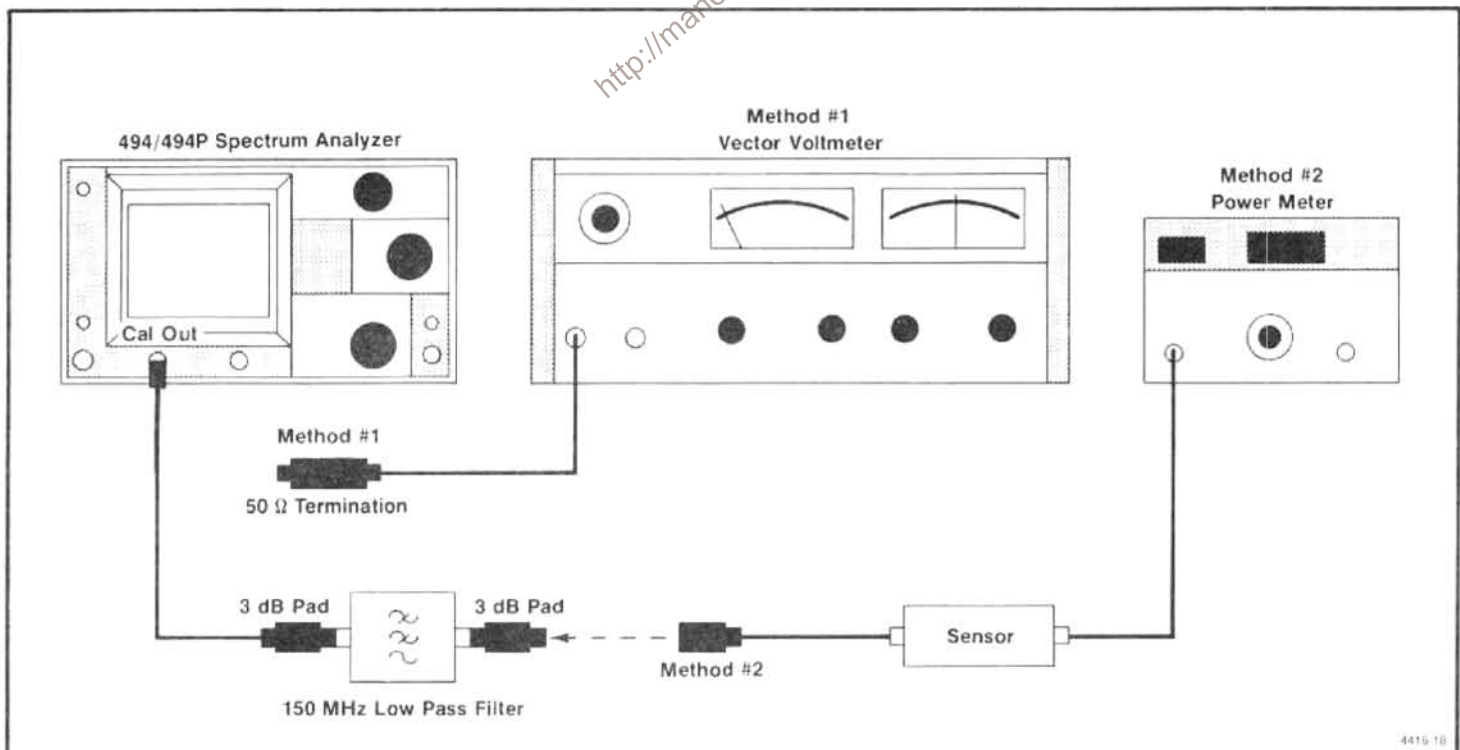


Figure 4-10. Test equipment setup for checking the calibrator output level.

(2) Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 100 kHz, RESOLUTION BANDWIDTH to 1 MHz, and set the REF LEVEL to -18 dBm. Set TIME/DIV to AUTO and turn the PEAK/AVERAGE control fully clockwise

(3) Disconnect the meter and (using the same instrument cable and attenuator) apply the calibrated reference signal to the RF INPUT.

(4) Set the Vertical Display factor to the ΔA mode by pressing FINE. Adjust the REF LEVEL so the top of the signal is on a graticule line near the top of the screen. Reset the REF LEVEL to 0.00 dB by pressing FINE twice. If desired, store the display by activating SAVE A.

(5) Remove the reference signal and apply the CAL OUT signal to the RF INPUT.

(6) Adjust the REF LEVEL until the signal is the same amplitude as the reference established in part 4. Note the displacement, of the CAL signal from the reference, as the ΔA readout.

An alternate method to measure the difference is as follows: Decrease the RESOLUTION BANDWIDTH to 100 kHz, activate B—SAVE A, and note the displacement between the CAL signal and the reference. Displacement must not exceed 0.3 dB.

14. Check Frequency Response

Response, about the midpoint of the two extremes, is: ± 1.5 dB from 50 kHz to 1.8 GHz; ± 2.0 dB from 10 kHz to 1.86 GHz; ± 2.5 dB from 1.7 to 7.1 GHz; ± 3.5 dB from 5.4 to 18 GHz; and ± 5.0 dB from 15 to 21 GHz. Response with respect to 100 MHz: ± 3.5 dB from 1.7 to 7.1 GHz; ± 4.5 dB from 5.4 to 18 GHz; and ± 6.5 dB from 15.0 to 21 GHz.

Frequency response is the peak-to-peak variation of the displayed amplitude over a specified center frequency range, measured at the center frequency. It is measured with 10 dB of RF attenuation, with Peaking optimized, for those bands that are applicable, for each center frequency setting. Response includes the effect of input vswr, mixing mode (N), gain variation, and preselector or mixer. Digital storage typically increases errors by 0.5%.

Accurate measurement requires many small incremental checks across the frequency range. The response at each check point, above band 1, should be peaked with MANUAL PEAK or by activating the AUTO PEAK mode. When checking the external mixer bands the signal must be identified as a true response and peaked.

If your instrument is the rackmount version, with semi-rigid cables to the back panel (Option 31), frequency response may degrade at the higher frequency end (see Rackmount/Benchtop Version, Options section for details).

NOTE

Loss of signal through interconnecting cables becomes significant above 1 GHz; therefore, short (25 inch or less) semi-rigid cable with precision fittings to interconnect the test equipment should be used. Precise matching terminations and power dividers are also used to minimize reflections.

To expedite the measurement, this procedure uses a leveled output sweep oscillator rather than incremental checks. Digital storage is also used to provide a complete display of the swept frequency. VIEW A, VIEW B and MAX HOLD are reactivated for each sweep.

a. Test equipment setup is shown in Figure 4-11. Set the FREQUENCY to 5 MHz, FREQ SPAN/DIV to 1 MHz, TIME/DIV to 20 ms, REF LEVEL to 0 dBm, and MIN RF ATTEN to 30 dB. Activate 1 dB/div and AUTO RESOLN.

b. Apply the output of a constant level and calibrated 10 kHz to 10 MHz Signal Generator to the RF INPUT of the 494/494P. Set the generator frequency to 100 kHz and its output for about -10 dBm.

c. Adjust the REF LEVEL so the amplitude of the 100 kHz signal is about half screen, in the 2 dB/DIV mode. Activate VIEW A, SAVE A, and MAX HOLD.

d. Slowly tune the Signal Generator frequency from 10 kHz to 10 MHz, monitoring the output to ensure it remains constant. Note the frequency response (amplitude deviation above and below the average). Frequency response or amplitude deviation must not exceed ± 1.5 dB from 50 kHz to 10 MHz or ± 2.0 dB from 10 kHz to 10 MHz. (See Figure 4-12 for the average level.)

e. Replace the 10 kHz to 10 MHz signal source with a 0.01 to 2.4 GHz sweep oscillator and connect the test equipment as shown in Figure 4-13. The output of the Sweep Generator is applied through a 3 dB attenuator and high performance coaxial cable to a power divider. Connect one output of the power divider to the RF INPUT of the 494/494P and the other output to the sensor for the power meter or to the ALC input of the sweep oscillator.

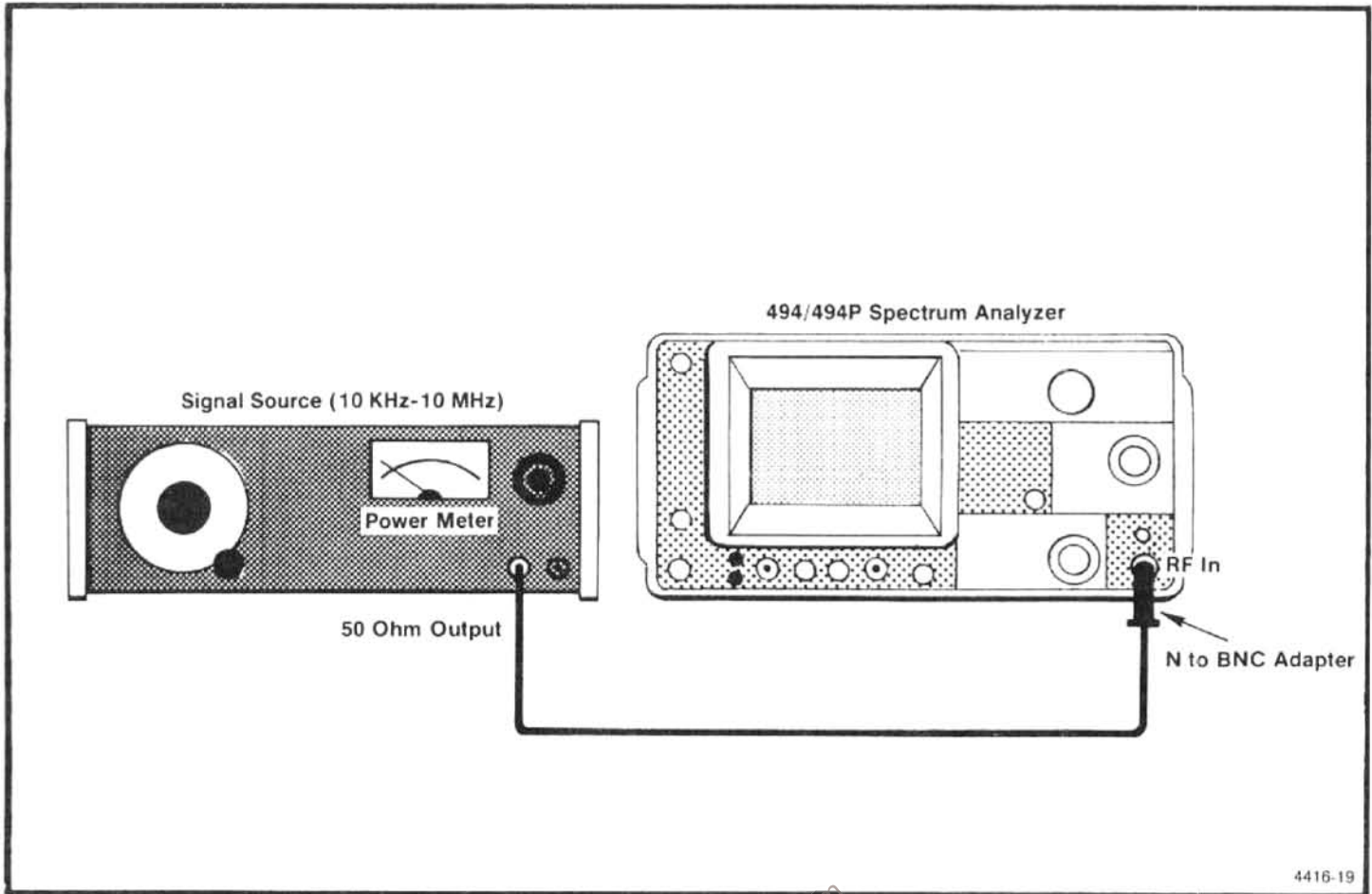


Figure 4-11. Test equipment setup for measuring 10 kHz to 10 MHz frequency response.

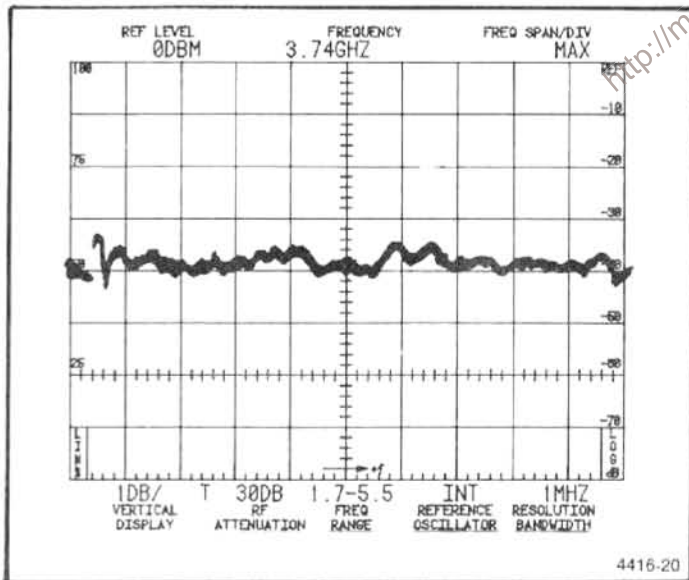


Figure 4-12. Display showing frequency response pattern from a sweeping source.

f. Change the FREQ SPAN/DIV to 200 MHz and the FREQUENCY to approximately 1.0 GHz. On the Sweep Generator, select a 1 GHz cw marker and adjust the output for a -6 dBm reading on the power meter. With the Vertical Display in the 2 dB/DIV mode, adjust the REF LEVEL so the signal amplitude is about half screen.

g. Change the Sweep Generator sweep mode to Automatic Internal Sweep and set the Sweep Time to 100 s for its slowest sweep time.

h. Check the frequency response over the 10 MHz to 1.8 GHz span. Deviation must not exceed ± 1.5 dB (Figure 4-12).

i. Change the FREQUENCY to 2.0 GHz and the FREQ SPAN/DIV to 100 MHz. Switch the Sweep Generator CW Marker on, and set it to 2.0 GHz. Peak the signal response of the 494/494P with the MANUAL PEAK control, or activate AUTO PEAK.

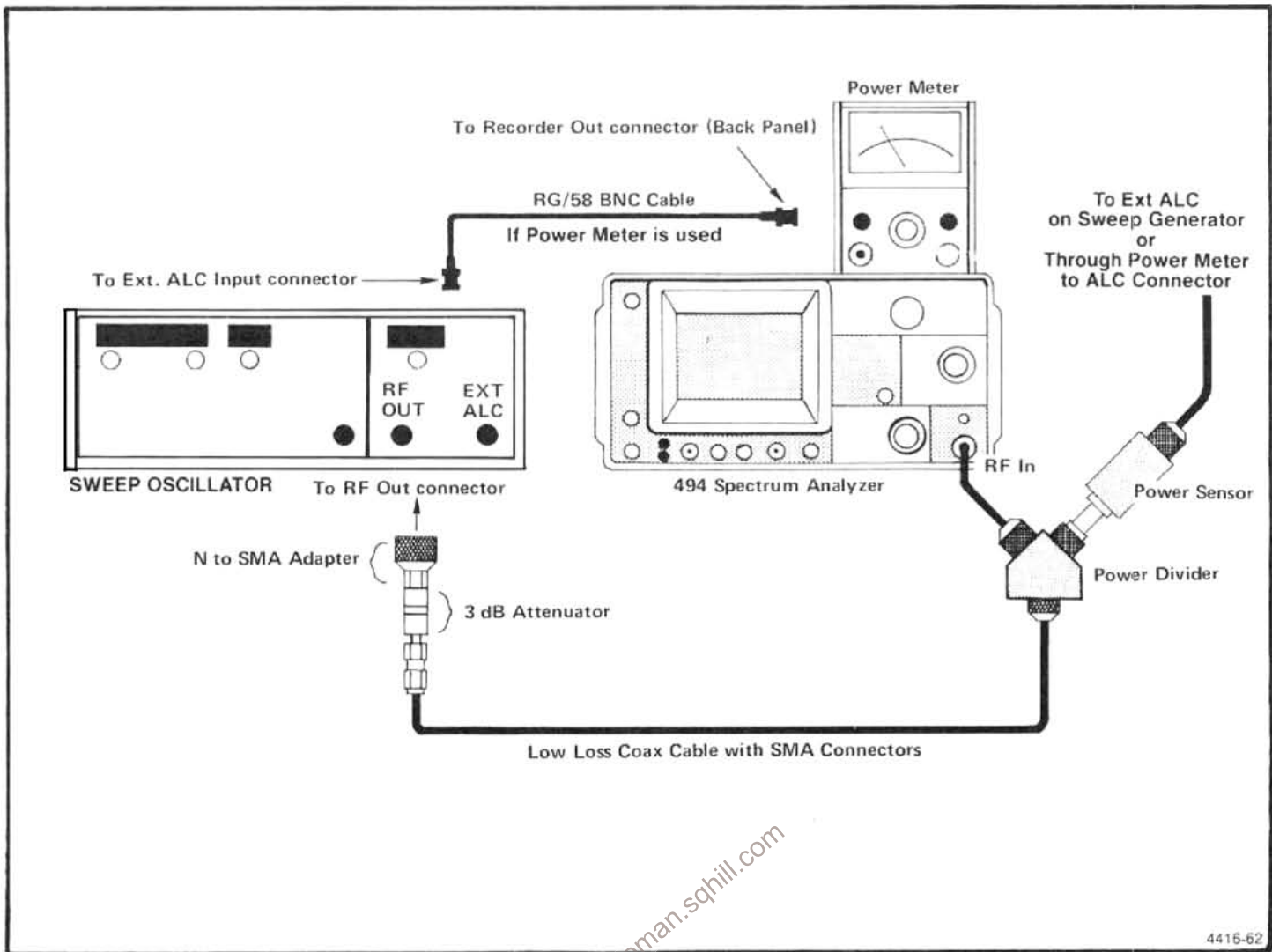


Figure 4-13. Test equipment setup for measuring .01 to 21 GHz frequency response.

j. Return the Sweep Generator to its Sweep mode and set the Start/Stop markers for 1.5 and 2.5 GHz. Sweep the 1.7 to 2.5 GHz span for Band 2 and note the frequency response. Frequency response or deviation must not exceed ± 2.5 dB.

NOTE

If any segment or portion of the span fails to meet the ± 2.5 dB specification, set the FREQUENCY to the center of this portion; apply a cw marker at this center frequency and re-peak with the MANUAL PEAK or AUTO PEAK mode. Decrease the FREQ SPAN/DIV to display that portion and then recheck the frequency response for this portion.

k. Replace the 0.01 to 2.4 GHz sweep source with a sweep oscillator that covers the frequency range to 21 GHz. Connect the test equipment as shown in Figure 4-13. On the RF plug-in, switch the ALC to Mtr position and connect a

coaxial cable between the Recorder Output of the power meter and the Ext ALC Input of the plug-in unit. Decrease the Power Level to approximately -6 dBm then adjust the Gain for stable operation (output stops oscillating).

l. Set the FREQ SPAN/DIV to 200 MHz and the FREQUENCY to 4.0 GHz. Re-peak the response with the peaking controls, then sweep the upper portion of band 2 and check frequency response. If necessary, recheck those portions that do not meet specification after peaking the response at the center of those portions of the frequency spectrum.

m. Increase the FREQUENCY RANGE to the 3.0 to 7.1 GHz band. Tune the CENTER FREQUENCY to approximately 5.0 GHz. Apply a 5.0 GHz cw marker and peak the response. Activate MAX SPAN and check the frequency response by sweeping the 3.0 to 7.1 GHz frequency range. It may be necessary, if the response does not meet the ± 2.5 dB performance, to again peak the response at the

center of those portions that do not meet specifications and recheck frequency response in smaller segments.

n. Repeat the foregoing procedure to check the response of the remaining bands to 21 GHz. Frequency response for band 4 (5.4-18 GHz) is ± 3.5 dB and ± 5.0 dB for band 5 (15.0-21.0 GHz).

15. Check Display Accuracy and Range

80 dB in 10 dB/DIV mode, with an accuracy of ± 1.0 dB/10 dB to a maximum cumulative error of ± 2.0 dB over the 80 dB window; 16 dB in 2 dB/DIV mode with an accuracy of ± 0.4 dB/2 dB to a maximum cumulative error of ± 1.0 dB/dB over the 16 dB window; Lin mode is $\pm 5\%$ of full scale.

a. Test equipment setup is shown in Figure 4-14. Apply a 100 MHz, +10 dBm signal, from the Signal Generator, through external attenuators set to 0 dB, to the RF INPUT.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 20 kHz, Vertical Display to 10 dB/DIV, MIN RF ATTEN at 0 dB, REF LEVEL to +10 dBm, and PEAK/AVERAGE control fully clockwise. Activate AUTO RESOLN and the NARROW Video Filter.

c. Carefully adjust the generator output so the signal level is at the top graticule line.

d. Add 80 dB of external attenuation in 10 dB steps and note that the signal steps down screen in 10 dB (± 1.0 dB) steps. Maximum cumulative error should not exceed 2.0 dB over the display window.

e. Return the external attenuation to 0 dB and change the Vertical Display to 2 dB/DIV. Change the RESOLUTION BANDWIDTH to 100 kHz and set the signal peak at the reference (top) graticule line, with the generator output control.

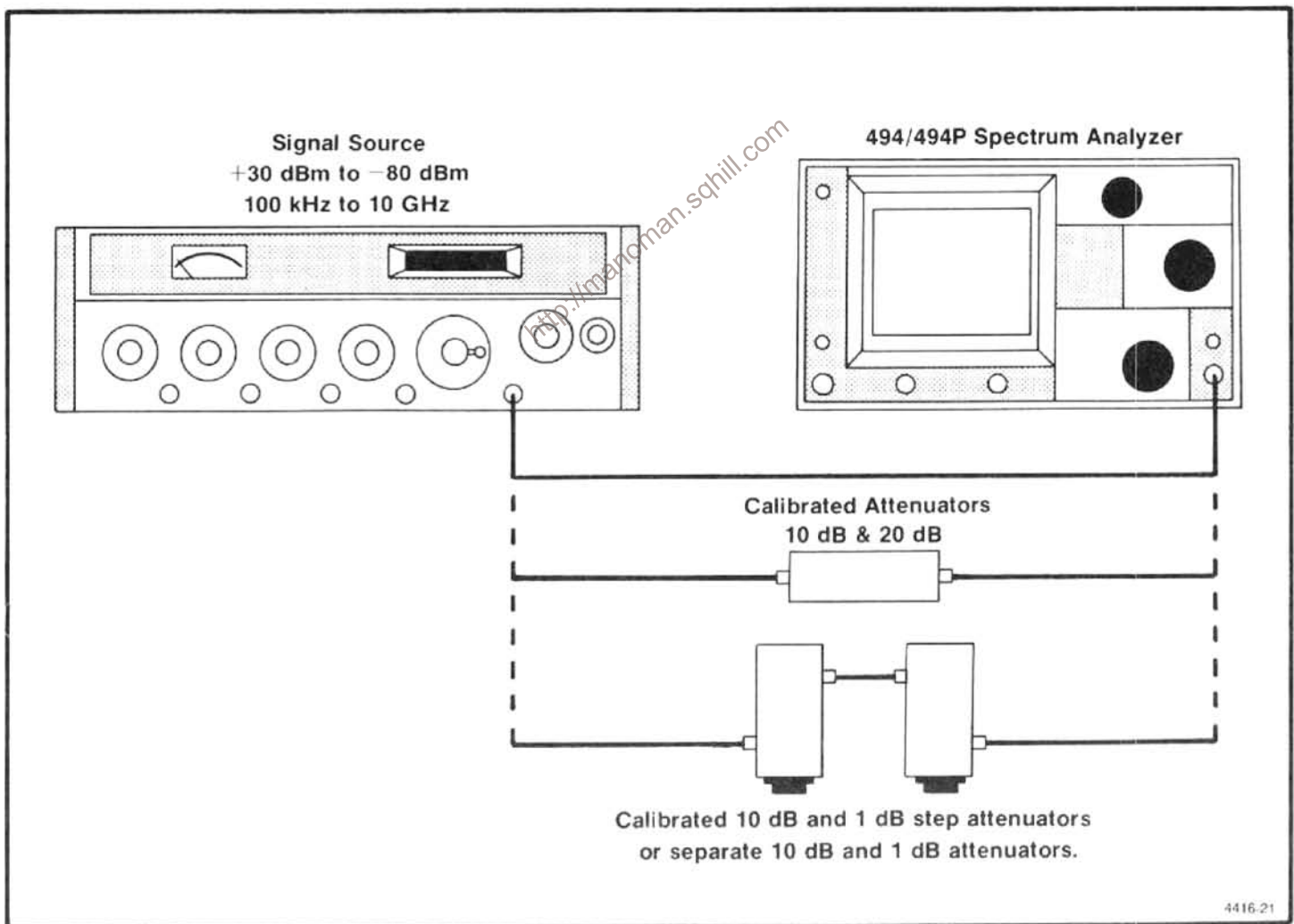


Figure 4-14. Test equipment setup for checking display accuracy, attenuator and gain accuracy, and preselector image rejection.

f. Add 16 dB of external attenuation, in 2 dB steps, and check the display accuracy. Error should not exceed ± 0.4 dB/2 dB or exceed a cumulative deviation of ± 1.0 dB over the 16 dB window.

g. Return the external attenuation to 0 dB. Change the Vertical Display to LIN. Adjust the signal generator output for a full screen signal display.

h. Add 6 dB of external attenuation. Note that the signal amplitude decreases to within ± 0.4 dB of half screen.

i. Add an additional 6 dB of attenuation. Note that the signal amplitude decreases to within ± 0.4 divisions of 1/4 screen or half the previous amplitude.

j. Add an additional 6 dB of attenuation. Signal amplitude should decrease to 1.0 ± 0.4 divisions.

k. Return the Vertical Display to 10 dB/DIV and disconnect the signal to the RF INPUT.

16. Check Preselector Ultimate Rejection

This is a check of preselector operation, not a performance requirement specification.

a. Test equipment setup is shown in Figure 4-14. Apply a 3.5 GHz, -30 dBm, signal from the Signal Generator to the RF INPUT.

b. Set the FREQUENCY to 3.5 GHz, FREQ SPAN/DIV to 10 kHz, REF LEVEL to -30 dBm, MIN RF ATTEN at 0 dB, TIME/DIV to AUTO, and Vertical Display of 10 dB/DIV. Activate AUTO RESOLN and WIDE Video Filter.

c. Adjust the Signal Generator output for a full screen display. Peak the response with the MANUAL PEAK control or AUTO PEAK mode.

d. Change the FREQ RANGE to band 3 (3.0-7.1 GHz).

e. Check the display for any spurious signals. Any spurious above 70 dB down from the level established in part c, is an indication that the YIG-tuned preselector filter could be defective.

17. Check RF Attenuator Accuracy

Error is within 0.3 dB/10 dB to a maximum of 0.7 dB, over the 60 dB range, to 4 GHz; and within 0.5 dB/10 dB to a maximum of 1.4 dB, over the 60 dB range, to 21 GHz

NOTE

The RF Attenuator is factory checked to ensure accuracy. Any change in characteristics should be readily noticed in operation. The Operational Check of the controls and selectors, should detect any defect. In this procedure, external 10 dB, 20 dB, or 30 dB step attenuators, calibrated by the user or manufacturer to within 0.05 dB, are used as a standard to check the attenuation steps of the RF attenuator.

a. Test equipment is shown in Figure 4-14. Apply a 0 dBm, 4 GHz signal, from a Signal Generator through 30 dB of calibrated attenuation, to the RF INPUT.

b. Set the FREQUENCY to 4 GHz, FREQ SPAN/DIV to 20 kHz, RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to -30 dBm, and Vertical Display factor to 10 dB/DIV.

c. Peak the signal response with MANUAL PEAK or AUTO PEAK mode. Activate 1 dB/div, via the Data Entry keyboard, and press NARROW Video Filter. Adjust the Signal Generator output so the top of the signal is on some graticule reference line, such as seven divisions. Activate SAVE A.

d. Change the REFERENCE LEVEL 10 dB by switching to -20 dBm (this will add 10 dB of RF ATTENUATION).

e. Remove 10 dB of external attenuation and activate B—SAVE A. Compare the difference between the reference level and the new level. Variation, plus the calibrated 10 dB external attenuator correction factor, must not exceed 0.3 dB. Deactivate SAVE A and B—SAVE A.

f. Readjust the Signal Generator output to establish a new reference level. Repeat the process to check the 20 dB attenuator by switching the REF LEVEL from -30 dBm to -10 dBm, for 20 dB ATTEN, then remove 20 dB of external attenuation. Attenuation error must not exceed 0.6 dB.

g. Reinstall the 30 dB of external attenuation and set the REF LEVEL to -30 dBm. Re-establish a signal reference level as described above.

h. Check the 30 dB attenuator against the external standard, by switching the REF LEVEL to 0 dBm, for 30 dB RF ATTEN, then remove 30 dB of external attenuation. Error must not exceed 0.7 dB. (Include the calibrated attenuator correction factor.)

i. Since the remaining 60 dB range of the RF ATTENUATOR is obtained by the combination of these three attenuators, this completes the check of the RF attenuator. Error of any combination must not exceed 0.7 dB.

18. Check IF Gain Accuracy ± 0.2 dB/dB and ± 0.5 dB/9 dB to a maximum of ± 2 dB over the full 97 dB range

NOTE

This check requires calibrated attenuators as the standard to check the 10 dB and 1 dB steps. When making signal measurements within 10 dB of the noise floor, a correction factor should be used to correct for the logarithmic addition of noise in the system and analyzer, as shown in Table 4-4.

a. Equipment setup is shown in Figure 4-14. Apply a 100 MHz, -20 dBm signal, from the Signal Generator, through 10 dB and 1 dB step attenuators (set at 0 dB), to the RF INPUT; or, directly to the RF INPUT of the 494/494P, if individual fixed attenuators are to be used as the standard.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 10 kHz, RESOLUTION BANDWIDTH to 10 kHz, REF LEVEL to -20 dBm, and MIN RF ATTENUATOR to 0 dB. Activate 1 dB/div and WIDE Video Filter.

c. Adjust the output of the Signal Generator for a signal amplitude of six divisions, with the top of the signal positioned at the 6th graticule line.

d. Activate MIN NOISE and note signal level shift. Shift must not exceed ± 0.8 dB, or 4 minor divisions (attenuator plus gain accuracies).

e. Adjust the output of the Signal Generator to re-position the signal level to the graticule reference line.

f. Switch the REF LEVEL from -10 dBm to -20 dBm in 1 dB steps, adding 1 dB of external attenuation at each step. Note incremental accuracy and the 10 dB gain accu-

racy. Incremental accuracy must be within 0.2 dB/dB (0.5 minor division). Maximum cumulative error must not exceed 0.5 dB (1.5 minor divisions) except when stepping from the 9 dB to 10 dB increment, where the error could be an additional 0.5 dB. This exception does not apply when stepping from -69 to -70 dBm, -79 to -80 , etc.

g. Deactivate MIN NOISE. Return the 1 dB step attenuator to 0 dB, decrease the Signal Generator output to 10 dB or add 10 dB of external attenuation. Readjust the generator output so the signal level is again at the reference line (6 division amplitude).

h. Change the REF LEVEL from -20 dBm to -30 dBm, in 1 dB increments, with the 1 dB step attenuator, and note incremental and 10 dB step accuracies.

i. Return the 1 dB step attenuator to 0 dB. Decrease the signal level 10 dB, with external attenuation, or with the Signal Generator output level control, then re-establish the signal reference amplitude.

j. Check the -30 dBm to -40 dBm gain accuracies using the above procedure.

k. Repeat the procedure checking gain accuracies to -60 dBm.

l. Establish a signal reference amplitude of -60 dBm, activate NARROW Video Filter, then check gain accuracy to -70 dBm.

m. Decrease the RESOLUTION BANDWIDTH and FREQ SPAN/DIV to 1 kHz. Re-establish a signal reference level of -70 dBm as described previously.

n. Check the -70 dBm to -80 dBm gain accuracies by repeating the process previously described;

o. Decrease the RESOLUTION BANDWIDTH and FREQ SPAN/DIV to 100 Hz or 50 Hz, reestablish the signal reference level and check the -80 dBm to -90 dBm and -90 to -100 dBm gain accuracies. These ranges are directly related to the -60 to -70 dBm check (parts e-o).

19. Check Gain Variation Between Resolution Bandwidths

Variation is less than 0.4 dB with respect to the 1 MHz filter and less than 0.8 dB between any two filters. Before

Table 4-4
CORRECTION FACTOR TO DETERMINE TRUE SIGNAL LEVEL

Ratio in dB of signal plus noise	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0	12.0	14.0
Subtract this correction factor for true signal level	3.0	2.20	1.65	1.26	0.97	0.75	0.58	0.46	0.28	0.18

performing this check, do a front panel CAL procedure (press <SHIFT> CAL and perform the steps called out).

a. Apply the Calibrator signal to the RF INPUT, set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 100 kHz, RESOLUTION BANDWIDTH to 1 MHz, REF LEVEL to -18 dBm, TIME/DIV at AUTO, and Vertical Display to 2 dB/DIV. Activate the MIN NOISE so RF ATTEN is 0 dB.

b. Change the Vertical Display to 1 dB/DIV by pressing <SHIFT> dB/DIV, and enter 1 dB/DIV via the Data Entry keyboard. Press FINE to activate the delta A mode.

c. Adjust the REFERENCE LEVEL for a signal amplitude of six divisions, then change the RESOLUTION BANDWIDTH to 100 kHz and FREQ SPAN/DIV to 10 kHz.

d. Check — The signal amplitude deviation from the 1 MHz reference should not change more than 0.4 dB.

e. Change the RESOLUTION BANDWIDTH to 10 kHz and the FREQ SPAN/DIV to 1 kHz.

f. Check — The signal amplitude should not change more than 0.8 dB from the amplitude at 100 kHz resolution and no more than 0.4 dB from the 1 MHz reference level.

g. Repeat the procedure to check the remaining filters (1 kHz, 100 Hz, and 30 Hz) to verify that the signal amplitude does not change more than 0.4 dB from the 1 MHz filter level or a total of 0.8 dB from any filter.

20. Sensitivity (refer to Table 4-5)

NOTE

Sensitivity is specified according to the input mixer average noise level. The Calibrator signal is the reference used to calibrate the display.

a. Remove the Calibrator signal from the RF INPUT. Set the Vertical Display to 10 dB/DIV, REF LEVEL to -30 dBm, FREQ SPAN/DIV to 5 MHz, RESOLUTION BANDWIDTH to 1 MHz, TIME/DIV at 1 s, and FREQ RANGE 0 - 1.8 GHz. Turn the PEAK/AVERAGE control fully clockwise so the cursor is at the top of the screen and activate the WIDE Video Filter.

b. Check— The noise floor (level) should be -80 dBm or less (as indicated in Table 4-5) or 50 dB down from the -30 dBm REF LEVEL.

c. Change the REF LEVEL to -40 dBm, FREQ SPAN/DIV to 1 MHz, and RESOLUTION BANDWIDTH to 100 kHz.

d. Check — The average noise level should be -90 dBm or less or 50 dB below the REF LEVEL.

e. Change REF LEVEL to -60 dBm, FREQ SPAN/DIV to 10 kHz, TIME/DIV to AUTO, RESOLUTION BANDWIDTH to 1 kHz, and activate the NARROW Video Filter.

f. Check — The average noise level for the 1 kHz resolution bandwidth should be below the level listed in Table 4-5.

g. Change REF LEVEL to -70 dBm, FREQ SPAN/DIV to 200 Hz, and RESOLUTION BANDWIDTH BANDWIDTH to 100 HZ.

h. Check — The noise level for the 100 Hz resolution bandwidth is no more than that listed in Table 4-5.

i. Change RESOLUTION BANDWIDTH to 30 Hz, and FREQ SPAN/DIV to 50 Hz.

j. Check — The noise level for the 30 Hz resolution bandwidth is as listed in Table 4-5.

k. Repeat this procedure for the remaining coaxial input frequency range (0 to 21 GHz). If desired, the sensitivity for the waveguide bands can be checked as per the listings in Table 4-5. The Figures for the 50 GHz to 140 GHz range are typical and not intended as a performance requirement.

21. Check Spurious (Residual) Response

With no input signal, residual spurs are -100 dBm or less, with reference to the mixer input and fundamental mixing for bands 1-3.

a. Remove any signal connected to the RF INPUT. Set the FREQ SPAN/DIV to 10 MHz, RESOLUTION BANDWIDTH to 10 kHz, REF LEVEL to -50 dBm, TIME/DIV at AUTO, and activate 10 dB/DIV.

b. Scan the frequency range of bands 1, 2, or 3 in 100 MHz increments. Note the amplitude of any spurious response. Spurious amplitude must not exceed -100 dBm. (If delta F is activated after each increment, it is easier to determine 100 MHz increments.)

22. Intermodulation Distortion

Third order products, within any frequency span, from 50 kHz to 18 GHz, are 70 dB down from any two on-screen signals; and from 1.7 to 1.8 GHz within any frequency span, IM from any two -40 dBm signals, is at least -70 dBc.

a. Equipment setup is shown in Figure 4-15. Set the FREQ SPAN/DIV to 5 MHz, RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to -30 dBm, and FREQUENCY

Table 4-5
494/494P SENSITIVITY

This table shows the equivalent maximum input noise (average noise for each resolution bandwidth with internal mixer and TEKTRONIX High Performance Waveguide Mixers).

Band/Frequency	Equivalent Input Noise (dBm) versus Resolution Bandwidth					
	1 MHz	100 MHz	10 kHz	1 kHz	100 Hz	30 Hz
Band 1-3 50 kHz-7.1 GHz	-80	-90	-100	-110	-118	-121
Band 4 5.4-12.0 GHz	-65	-75	-85	-95	-103	-106
Band 5 15.0-21.0 GHz	-55	-65	-75	-85	-93	-96
^a Band 6 18.0-26.5 GHz	-70	-80	-90	-100	-108	-111
^a Band 7 26.5-40.0 GHz	-65	-75	-85	-95	-103	-106
^a Band 8 33-60 GHz	-65	-75	-85	-95	-103	-106
^a Band 9 50-90 GHz	Typically -95 dBm for 1 kHz resolution bandwidth at 50 GHz, degrading to -85 dBm at 90 GHz.					
^a Band 10 75-140 GHz	Typically -90 dBm for 1 kHz bandwidth at 75 GHz, degrading to -75 dBm at 140 GHz.					
^a Band 11 110-220 GHz	Typically -80 dBm for 1 kHz bandwidth at 110 GHz, degrading to -65 dBm at 220 GHz.					
^a Band 12 170-325 GHz	Typically -70 dBm for 1 kHz bandwidth at 170 GHz, degrading to -55 dBm at 325 GHz.					

^aTEKTRONIX High Performance Waveguide Mixers

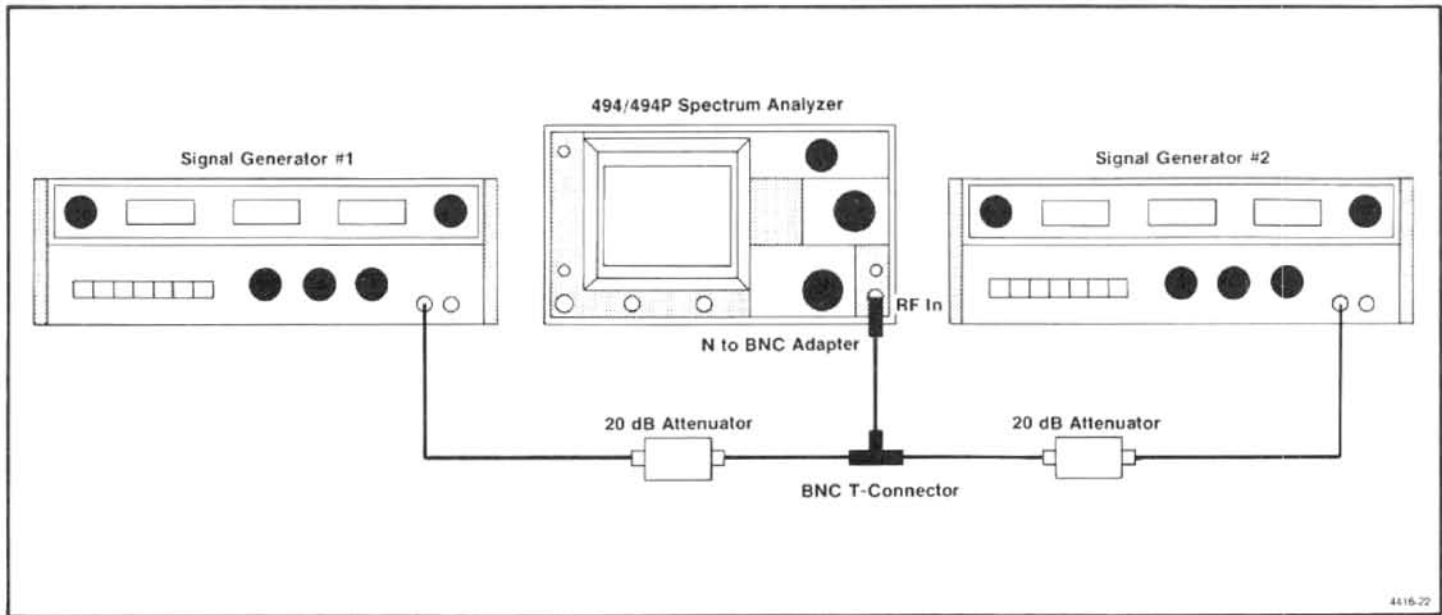


Figure 4-15. Test equipment setup for checking intermodulation distortion.

RANGE to Band 1. Activate 10 dB/DIV, and switch MIN NOISE off.

b. Apply two signals, from two 50 Ω sources, that are separated about 2 MHz and within the frequency range of band 1. Apply the signals through 20 dB attenuators (for isolation), a bnc "T" connector, and bnc-to-n adapter, to the RF INPUT (see Figure 4-15).

c. Adjust the output of the Signal Generators for full screen signals (−10 dBm). Decrease the frequency separation of the signals to 1 MHz and the FREQ SPAN/DIV to 500 kHz. Set the RESOLUTION BANDWIDTH to 10 kHz.

d. Check — that third order intermodulation products (see Figure 4-16) are 70 dB or more down from the input signal level.

NOTE

Use the Video Filter and very slow sweep rates to help resolve these sidebands.

e. Decrease the signal separation and FREQ SPAN/DIV settings and re-check for sidebands. Check for IM products at other spans of the frequency range. IM products should be −70 dBc or more.

f. Change the FREQUENCY RANGE to 1.7 - 5.5 GHz (band 2). FREQ SPAN/DIV to 50 MHz, and RESOLUTION BANDWIDTH to 100 kHz.

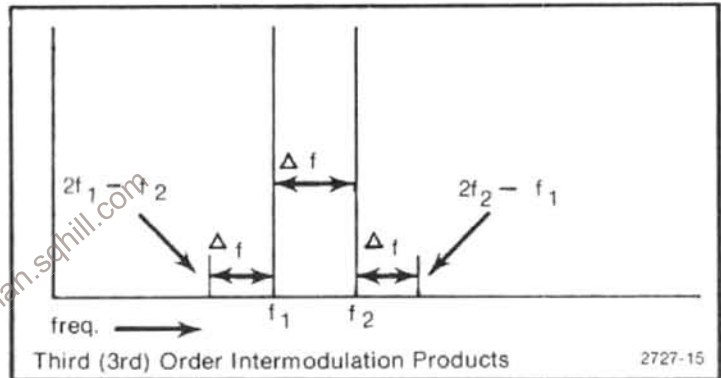


Figure 4-16. Intermodulation products.

g. Apply two full screen (−30 dBm) signals that are above 1.8 GHz to the RF INPUT. Reduce the FREQ SPAN/DIV and RESOLUTION BANDWIDTH so the noise floor is at least 70 dB down from the reference level.

h. Check — to ensure IM products are at least 70 dB down from the input signal level or top of the screen.

i. Change the frequencies of the Signal Generators to frequencies within the 1.7-1.8 GHz range and set the input signal level to −40 dBm by increasing the output of the Signal Generators.

j. Check — that IM products are at least −70 dBc.

23. Check Harmonic Distortion

–60 dBc, 50 kHz – 1.8 GHz; and –100 dBc, 1.7 – 21 GHz; below the level of a full screen signal in MIN DISTORTION mode.

a. Equipment set up is shown in Figure 4-17. Set the FREQ SPAN/DIV to 5 MHz, REF LEVEL to –30 dBm, and RF ATTEN to 0 dB. Activate AUTO RESOLN, 10 dB/DIV, WIDE Video Filter, MIN DISTORTION, and VIEW A, VIEW B.

NOTE

The frequency used must have harmonics between 1.7 – 21 GHz and the signal generator must have low enough FM to produce a signal to measure 100 dB down.

b. Apply the output of a Signal Generator, through a low-pass or band-pass filter (with a minimum of 40 dB

rolloff, to attenuate multiples of the generator frequency) to the RF INPUT. (Frequency of the Signal Generator depends on the frequency characteristics of the filter.)

c. Set the 494/494P FREQUENCY to that of the applied signal frequency and adjust the generator output for a full screen (–30 dBm) signal.

d. Press Δ F and adjust the CENTER FREQUENCY to the 2nd multiple of the input frequency. Set the REF LEVEL to –50 dBm, the FREQ SPAN/DIV to 500 kHz, and the RESOLUTION BANDWIDTH to 10 kHz.

e. Check — the display for harmonic response of the input signal. Harmonic spuri must be down at least 40 dB from the top of the screen or 60 dB below the –30 dBm carrier.

f. Set the CENTER FREQUENCY to the 3rd harmonic.

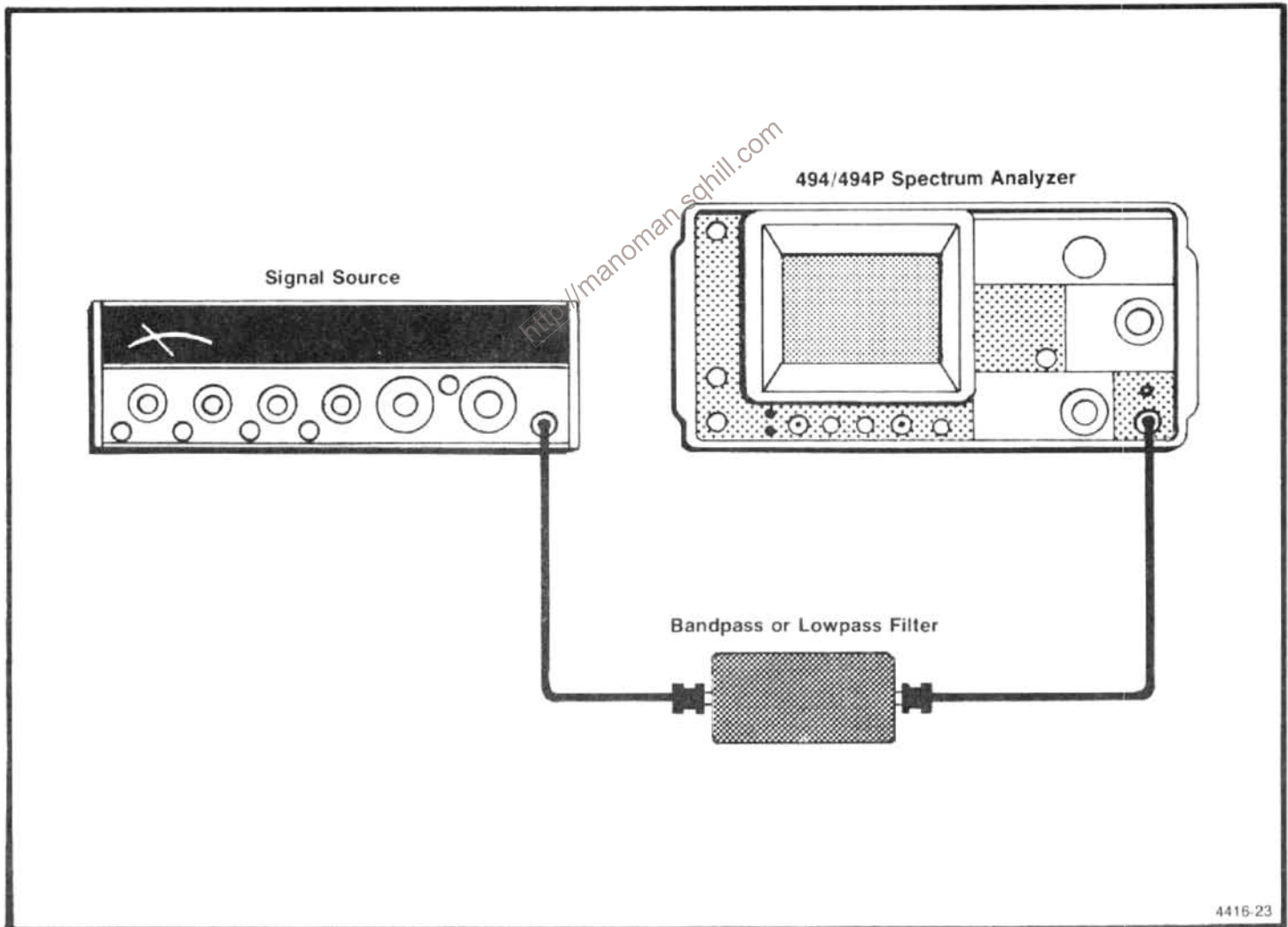


Figure 4-17. Equipment setup for checking harmonic distortion.

g. Check — for harmonic spuri. Again, responses must be at least 40 dB down from the top of the screen or -60 dBc from the fundamental.

h. Set the REF LEVEL to -70 dBm, the FREQ SPAN/DIV to 2 kHz, and the RESOLUTION BANDWIDTH to 100 Hz. Deactivate the WIDE Video Filter.

i. Check — that harmonic spuri are at least 60 dB down from the top of the screen (-100 dBc).

24. Check LO Emission Out the RF Input

Emission is no more than -70 dBm.

a. Connect a sensitive power meter to the RF INPUT so emissions can be measured directly, or connect a high frequency Spectrum Analyzer, set to observe the 2 GHz to 6 GHz range, to the RF INPUT.

b. Set the TIME/DIV to MNL.

c. Check — for any indication of LO emission. Any emission must be less than -70 dBm.

25. Check 1 dB Compression Point

1 dB compression, 1.7 - 2.0 GHz, is -28 dBm or more, otherwise -18 dBm.

a. Equipment setup is shown in Figure 4-18.

b. Connect the power meter with its sensor to the Calibrated Output of the Signal Generator. Set the generator to 1.7 GHz and adjust the output for 0 dBm, as indicated on the power meter.

NOTE

Calibrate the power meter before making this measurement.

c. Disconnect the power meter from the Signal Generator and connect the generator output through 1 dB and 10 dB step attenuators to the RF INPUT of the 494/494P. Set the attenuators for 20 dB of attenuation (10 dB per attenuator).

d. Connect the 10 MHz IF output (on the rear panel of the 494/494P) through a 1 dB step attenuator, to the RF

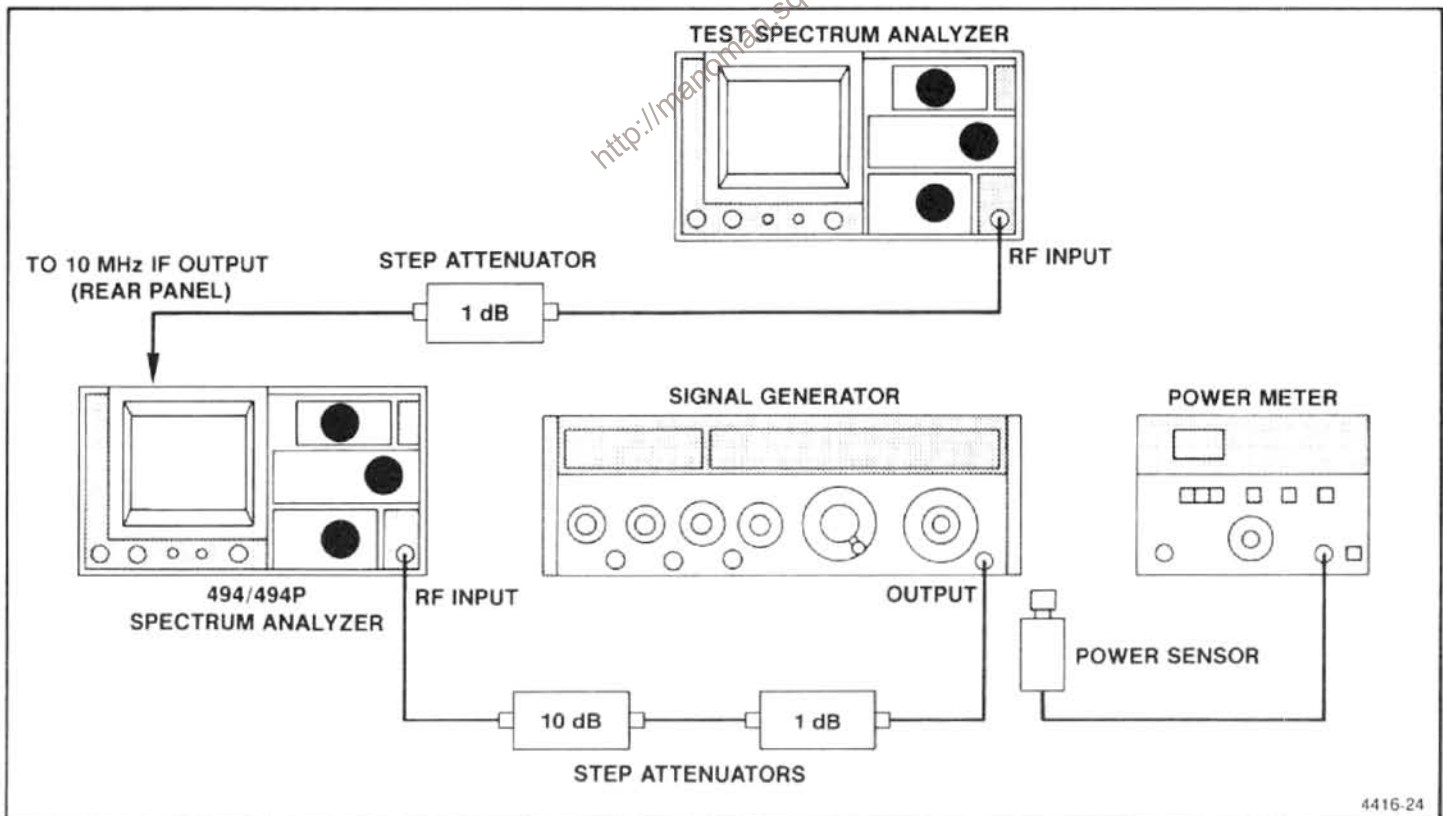


Figure 4-18. Test equipment setup for checking 1 dB input compression point.

Input of a test Spectrum Analyzer. Set the step attenuator for 0 dB attenuation.

e. Set the test Spectrum Analyzer Frequency to 10 MHz, Frequency Span/Div to 100 MHz, Ref Level to -20 dBm, Time/Div to Auto, and activate 2 dB/Div and Auto Resoln.

f. Set the 494/494P FREQUENCY to 1.7 GHz, FREQ SPAN/DIV to 100 kHz, REF LEVEL to -30 dBm, TIME/DIV to AUTO, and activate 10 dB/DIV and AUTO RESOLN.

g. On the 494/494P, activate ZERO SPAN and adjust the CENTER FREQUENCY control to maximize the 10 MHz signal on the test Spectrum Analyzer display.

h. Adjust the test Spectrum Analyzer Ref Level for a four division signal amplitude.

i. Increase the input signal level, to the 494/494P, 1 dB by switching out 1 dB of attenuation between the Signal Generator and the input to the 494/494P. Add 1 dB of attenuation between the 10 MHz output and the test Spectrum Analyzer.

j. Check — the 10 MHz signal amplitude on the test Spectrum Analyzer display should remain the same.

k. Continue to increase the input signal level to the 494/494P by 1 dB increments while increasing the attenuation between the 10 MHz out and the test Spectrum Analyzer until the signal amplitude decreases 1 dB (0.5 division).

l. Check — the 1 dB compression point should be -18 dBm or less (18 dB or less attenuation between the generator and the input of the 494/494P).

m. Check Band 2 (1.7 - 2.0 GHz) compression point as follows:

(1) Deactivate ZERO SPAN, switch the FREQUENCY RANGE to Band 2, and set the FREQUENCY to 1.7 GHz (reference Level -30 dBm).

(2) Set the step attenuators, between the Signal Generator and the RF INPUT, to 30 dB (input to the 494/494P is now -30 dBm).

(3) Peak the signal response with MANUAL PEAK or AUTO PEAK.

(4) Set the attenuator, between the 10 MHz IF out and the test Spectrum Analyzer, to 0 dB.

(5) Activate ZERO SPAN and adjust the test Spectrum Analyzer Reference Level for an on screen display. Maximize the response by tuning the 494/494P CENTER FREQUENCY control.

(6) Set the test Spectrum Analyzer response to some reference level (such as 4 divisions) and repeat the above procedure to check the 1 dB compression point at 1.7 GHz.

(7) Compression should not occur until the input signal level is -28 dBm or more (28 dB external attenuation between the Signal Generator and the 494/494P RF INPUT).

(8) Deactivate ZERO SPAN and set the 494 FREQUENCY to 2.0 GHz.

(9) Return the step attenuators to 30 dB and 0 dB. Set the frequency of the Signal Generator to 2.0 GHz and repeat the above procedure to check 1 dB compression point at 2.0 GHz.

(10) 1 dB compression point should not occur until the input signal level to the RF INPUT is -28 dBm or more.

26 Check External Reference Input Power

$+15$ dBm to -15 dBm; 1,2,5, or 10 MHz.

a. Equipment setup is shown in Figure 4-19. Connect the output of the Signal Generator to a Frequency Counter and set the generator frequency to 10 MHz ± 50 Hz.

b. Disconnect the counter and apply the generator output to the EXTERNAL REFERENCE Input connector (on the rear panel) of the 494/494P. Set the generator output to $+15$ dBm.

c. Check — the crt readout for REF OSC IN USE should read "EXT".

d. Connect the 494/494P CAL OUT to the counter and note that the counter readout is 10 times the external reference source.

e. Decrease the Signal Generator output to -15 dBm and note that the crt readout is still "EXT" and the Frequency Counter still reads 10X the reference signal frequency. If the crt readout changes to: "EXT—UNLK", recheck the external reference source for 10 MHz ± 100 Hz at -15 dBm.

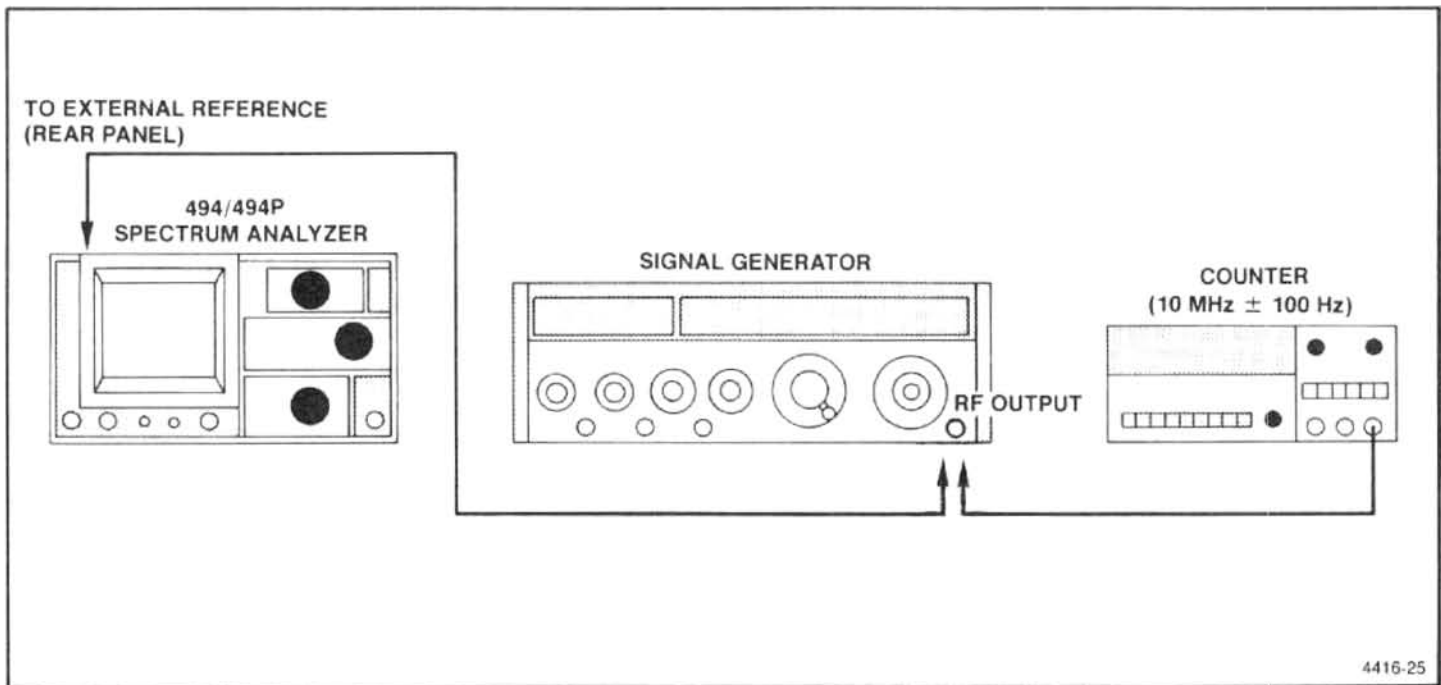


Figure 4-19. Test equipment setup for checking external reference input power.

27. Check Triggering Operation and Sensitivity

Sensitivity, for internal trigger, is 2.0 divisions or more; and 1.0 V peak, 15 Hz to 1 MHz, for external trigger.

a. Equipment setup is shown in Figure 4-20. Apply 100 MHz at -30 dBm from a Signal Generator, that is modulated by the output of a Sine-Wave Generator, to the RF INPUT. Monitor the output of the Sine-Wave Generator with a test Oscilloscope.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 10 kHz, RESOLUTION BANDWIDTH to 1 MHz, TIME/DIV to 20 ms, and REF LEVEL to -30 dBm. Activate LIN Vertical Display.

c. Decrease the output of the Signal Generator so the display is half screen, then modulate the signal with a 1 kHz sine wave.

d. Activate ZERO SPAN and adjust the CENTER FREQUENCY control if necessary for maximum response.

e. Adjust the Sine Wave Generator output for a modulation amplitude of two divisions, then activate INT Triggering.

f. Check the internal trigger operation through the 15 Hz to 1 MHz frequency range.

NOTE

Because of deflection amplifier response, the display amplitude will decrease at the high frequency end.

The triggering signal can also be applied to the MARKER/VIDEO connector on the back panel if a jumper is connected between pins 1 and 5 (Video Select) of the rear-panel ACCESSORIES connector (Figure 4-21).

g. Disconnect the test equipment. Apply a 1 kHz signal from the Sine Wave Generator, through a bnc "T" connector and coaxial cable, to the HORIZ/TRIG connector (on the back panel of the 494/494P (see Figure 4-22) Monitor the input signal amplitude with a test Oscilloscope.

h. Set the output level of the signal to 2 V peak-to-peak (1.0 V peak) as indicated on the test Oscilloscope (see Figure 4-23).

i. Change the TIME/DIV to 0.2 s. Activate EXT Triggering.

j. Check — that the sweep is triggered over the frequency range of 15 Hz to 1 MHz.

k. Return the Triggering to FREE RUN and the input signal level to 0 V.

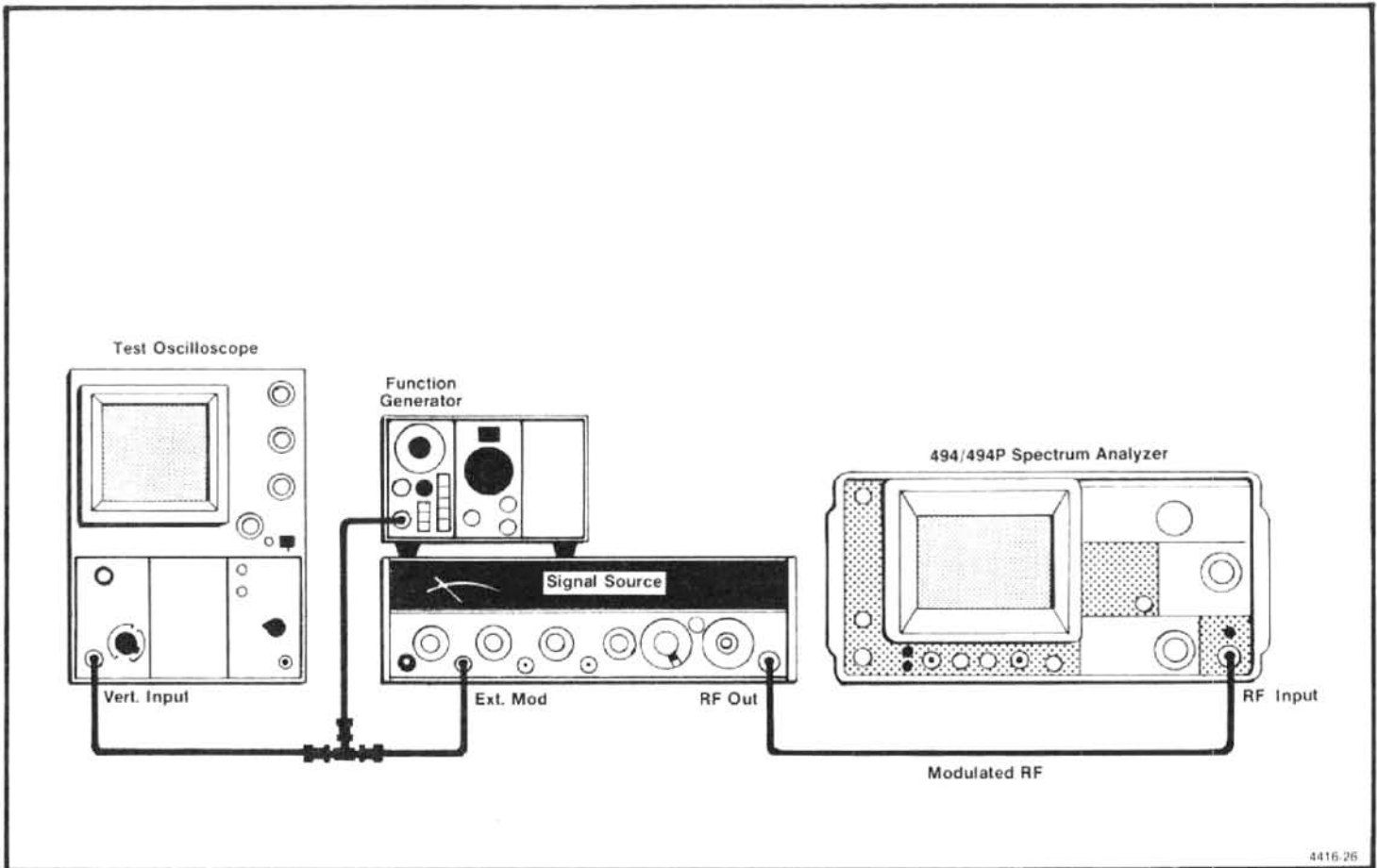


Figure 4-20. Equipment setup for checking internal trigger characteristics.

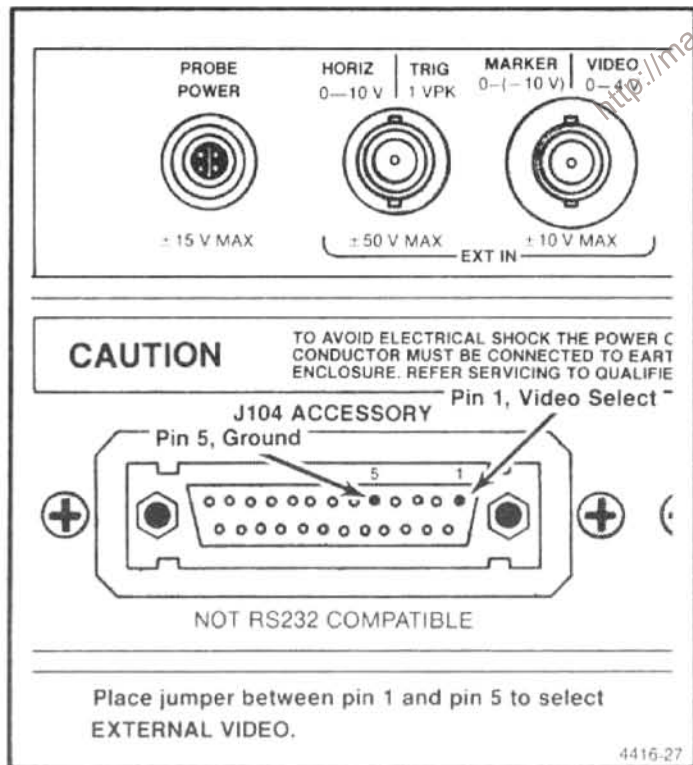


Figure 4-21. External video select pins on ACCESSORIES connector and input to MARKER/VIDEO for signal to check internal triggering.

28. Check External Sweep Operation

0 to 10 V \pm 1 V should provide a full sweep across the 10 division graticule span. This is an operational check, not a performance requirement.

a. With the test equipment connected as directed for the previous step, set the TIME/DIV to EXT, Vertical Display to 2 dB/DIV, and deactivate VIEW A, VIEW B.

b. With an input signal to the HORIZ/TRIG connector of 0 volt, position the crt beam on the left graticule edge, with the POSITION adjustment. This establishes the 0 V reference.

c. Set the generator frequency to 1 kHz and increase its output for a full 10-division sweep.

d. Check — the peak-to-peak voltage out of the Signal Generator should equal 20 V \pm 2 V, peak-to-peak, or 10 V \pm 1 V peak.

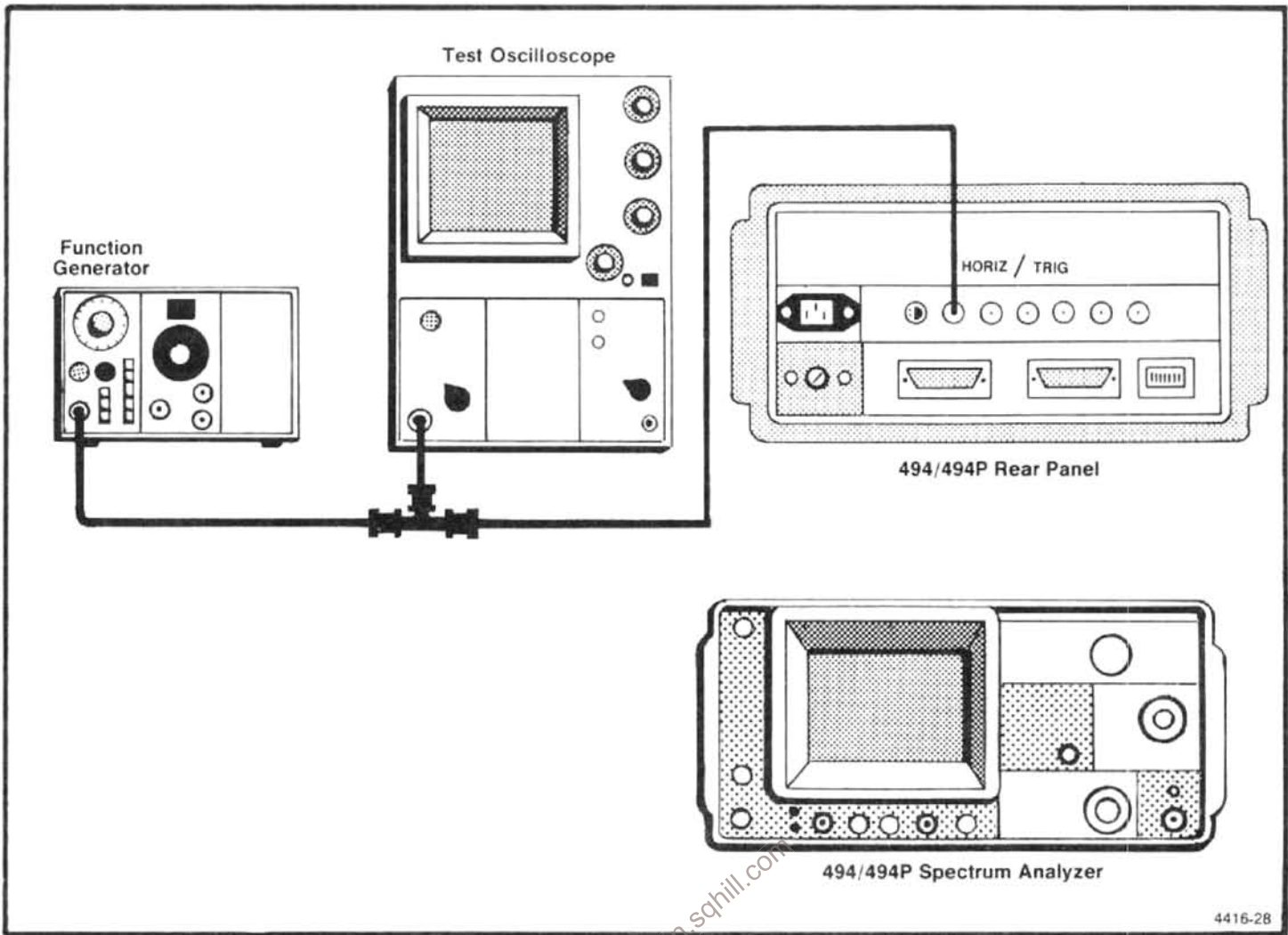


Figure 4-22. Equipment setup for checking external triggering and horizontal input characteristics.

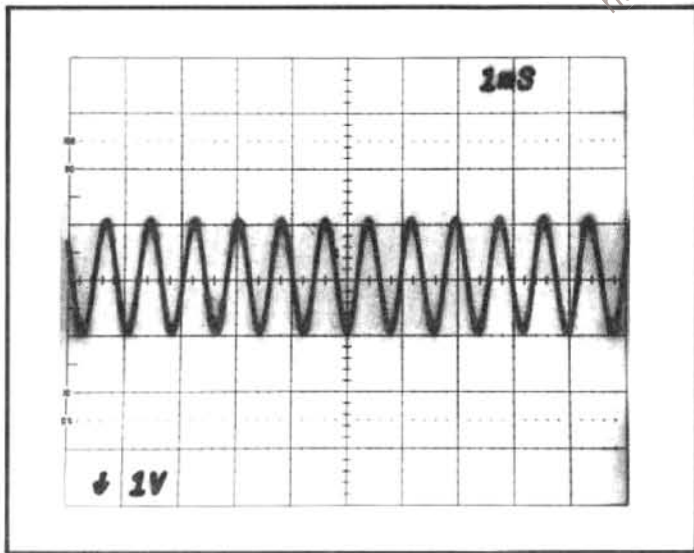


Figure 4-23. Test oscilloscope display of a sinewave input signal to the external TRIG connector (1.0 volt peak at 2.0 V peak-to-peak).

NOTE

A variable voltage source can be used in place of the Sine Wave Generator, to check external sweep operation.

- e. Disconnect and remove the test equipment. Return TIME/DIV to AUTO.

29. Check Vertical Output Signal

Output provides 0.5 V \pm 5% of signal per division of display from the centerline. This is an operational check, not a performance requirement.

- a. Connect the VERT OUTPUT to the input of a dc-coupled test Oscilloscope with a sensitivity of 1 V/div and a sweep rate of 10 ms.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 100 kHz, TIME/DIV to AUTO, REF LEVEL -20 dBm. Activate 2 dB/DIV and AUTO RESOLN, deactivate VIEW A and VIEW B.

c. Apply the CAL OUT signal to the RF INPUT and verify that the signal amplitude is full screen.

d. Check — the amplitude of the output vertical signal on the test Oscilloscope. Output level should equal, plus and minus 2 V for a total of 4 V \pm 0.2 V (see Figure 4-24).

30. Check Horizontal Signal Output Level

Output 0.5 V/division, \pm 5% either side of center screen. This is an operational check, not a performance requirement.

a. Connect a dc-coupled test oscilloscope to the HORIZ OUTPUT connector. Set the TIME/DIV to the MNL position.

b. Adjust MANUAL SCAN control for five division beam deflection from the left to right side of center screen and note the voltage sweep on the test Oscilloscope. The output voltage should vary from -2.5 V to +2.5 V, \pm 10%.

c. Return the TIME/DIV to AUTO; disconnect and remove the test equipment.

31. GPIB Verification Program (494P only)

This verification program can be used with a TEKTRONIX 4050-Series Computer Terminal to check the functional operation of the GPIB interface in the 494P Spectrum Analyzer. All interface lines are verified as well as all interface messages, except those for parallel poll. In addition, the instrument interface is checked for operation on other primary addresses, as well as the talk-only and listen-only modes.

The program is written in Tektronix 4050 BASIC, and is divided into individual tests, each for a specific interface line, message, or function. The tests start on even 1000 line numbers to allow easy modification of the program.

The following describes the function of each test in the program.

Lines 1-5000: Interfaces to user definable keys for recovery from a failed test.

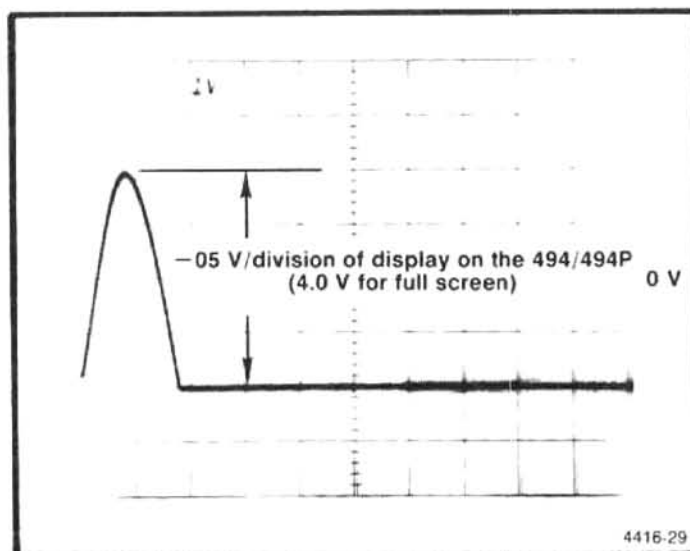


Figure 4-24. Test oscilloscope display of VERTICAL output with a full screen display on the 494.

Lines 5000-6000: Inputs the primary address of the 494P under test (1 should be used).

Lines 6000-7000: ID query response test. The instrument must be able to talk and listen, to send out its ID? response and manipulate all eight of the DIO lines for the test to be successful.

Lines 7000-8000: Local lock-out test. Tests correct operation of the interface message that should disable all programmable front panel controls.

Lines 8000-9000: Go to LOCAL test. Tests correct operation of the interface message that should enable all front panel controls.

Lines 9000-10000: Group Execute Trigger test. Checks that a GET message does cause the 494P to abort the present sweep and re-arm the trigger, causing a sweep to start and end, sending out an End-of-Sweep SRQ. Thus, the SRQ line, as well as the GET message, is verified.

Lines 10000-11000: Selected Device Clear Test. This test verifies that an SDC message does indeed reset the 494P's GPIB output buffer clearing out its ID? response.

Lines 11000-12000: Device clear test. This test is identical to the selected device clear test, except the universal command DCL is used instead.

Lines 12000-13000: Addressed as listener, talker test. This test checks to see that the 494P microprocessor correctly recognized that the GPIA chip has been addressed to listen or talk, and sends the appropriate character to the crt readout (L or T).

Lines 13000-14000: Serial Poll test. This checks correct operation of the serial poll enable (SPE) and serial poll disable (SPD) interface messages. The status byte is read, and if anything other than ordinary operation is indicated, the instrument fails the test.

Lines 14000-15000: GPIB rear panel switch test. All five primary address switches are checked for correct operation. Three subroutines are called in the process of testing one address switch. The first two send a formatted message to the 4050 display, and the third performs the address switch test.

Lines 15000-16000: Line feed or EOI switch test. Checks for correct selection of line feed as a termination when selected by this switch by sending an ID? terminated only by a line feed.

Lines 16000-17000: Talk-only mode test. When selected, this mode should cause the instrument to send a SET? response and (optionally) a CURVE? response whenever the RESET-TO-LOCAL button is pressed. The string received from the instrument is thus examined for existence of a portion of the correct SET? response after the RESET-TO-LOCAL button is pressed.

Lines 17000-18000: Listen-only mode test. When selected, this mode will cause the instrument to respond to any message on the bus, since it is always addressed to listen. The command REF 0 is sent to the bus without addressing the instrument, then the listen-only mode is deselected and the instrument interrogated to see if it did respond to the REF command while in the listen-only mode.

Lines 18000-19000: Interface clean (and Remote Enable) test. This IFC line on the GPIB will unaddress the instrument's interface. This fact is verified by noting that the L is not present in the crt readout, indicating that the IFC line worked; also the REN line will be unasserted when the end statement is executed (except for some early 4052 and 4054's). Thus, a front panel in the local mode is evidence that the REN line was successfully unasserted. (Evidence it was asserted is that the instrument was able to execute commands sent to it by previous tests.)

Lines 19000-end: Utility routines. Rear panel interface switch test text routine puts headers on the interface switch test display. The rear panel test text routine tells the operator what to do after changing the address switches. Test address switch acquires an ID? response from the instrument on its new address during the address switch test. The SRQ handler will handle any 49X SRQ's that occur, although none, except the power-up SRQ, would be expected. (The end of sweep SRQ during the GET test is handled by another SRQ handler.) Delay Generator generates delays for other tests. The Failure Decision Handler allows the program to be restarted with the user definable keys if any test fails.

```

1 GO TO 5000
4 B2=1
5 RETURN
20 B2=5
21 RETURN
5000 REM *** 49XP GPIB VERIFICATION PROGRAM ***
5030 INIT
5040 ON SRQ THEN 19280
5050 DIM V$(400),W$(400)
5060 I7=0
5070 PAGE
5080 PRINT "JJJENTER 49XP'S PRIMARY ADDRESS (DEFAULT = 1) ";
5090 INPUT T$
5100 IF T$<>" " THEN 5130
5110 A1=1
5120 GO TO 5180
5130 A1=VAL(T$)
5140 IF A1>0 AND A1<31 THEN 5180
5150 PRINT "JJJGERROR!! ";A1;" IS NOT A VALID ADDRESS";
5160 PRINT " ONLY 0 THRU 30 ARE VALID ADDRESSESKK"
5170 GO TO 5080
5180 PAGE
5190 REM
5200 REM
5210 REM
5220 REM
5230 REM
6000 REM ***"ID" QUERY RESPONSE ***
6010 PRINT "*** ""ID"" QUERY RESPONSE ***"
6020 PRINT @A1:"INIT;ID?;SIG"
6030 INPUT @A1:T$
6040 V$=SEG(T$,1,9)
6050 IF V$="ID TEK/49" THEN 6080
6060 PRINT "JJJ*** ""ID"" QUERY RESPONSE *** FAIL ***G"
6070 GO TO 19530
6080 WBYTE @32+A1:64,128,-127
6090 PRINT @A1:"WFM ENC:BIN;CUR?"
6100 PRINT @37,0:37,255,255
6110 INPUT %A1:T$
6120 WBYTE @64+A1:
6130 RBYTE R,R,R,T6
6140 WBYTE @95:
6150 IF R=>128 AND T6<128 THEN 7000
6160 PRINT "JJJ*** DI08 TEST *** FAIL ***G"
6170 GO TO 19530
6180 REM
6190 REM
6200 REM
6210 REM
6220 REM
7000 REM *** LOCAL LOCK-OUT.....LLO ***
7010 PRINT "*** LOCAL LOCK-OUT.....LLO ***"
7020 WBYTE @32+A1,17:
7030 PRINT @A1:"SET?"
7040 INPUT @A1:V$

```

```

7050 PRINT "II49XP IN LOCAL LOCK-OUT MODE (LLO )"
7060 PRINT "IIATTEMPT TO USE 49XP CONTROLS"
7070 PRINT "IIPRESS RETURN <CR> WHEN DONE ";
7080 INPUT T$
7090 PRINT @A1: "SET?"
7100 INPUT @A1:W$
7110 IF W$<>V$ THEN 7130
7120 GO TO 8000
7130 PRINT "J*** LOCAL LOCK-OUT.....LLO *** FAIL ***G"
7140 GO TO 19530
7150 REM
7160 REM
7170 REM
7180 REM
7190 REM
8000 REM *** GO TO LOCAL.....GTL ***
8010 PRINT @A1: "INIT;TIM?"
8020 INPUT @A1:R
8030 PRINT @A1: "TIM INC"
8040 PRINT "*** GO TO LOCAL.....GTL ***"
8050 WBYTE @32+A1,1:
8060 PRINT @A1: "TIM?"
8070 INPUT @A1:T6
8080 IF R<>T6 THEN 8100
8090 GO TO 9000
8100 PRINT "J**** GO TO LOCAL.....GTL *** FAIL ***G"
8110 GO TO 19530
8120 REM
8130 REM
8140 REM
8150 REM
8160 REM
9000 REM *** GROUP EXECUTE TRIGGER.....GET ***
9010 PRINT "*** GROUP EXECUTE TRIGGER...GET ***"
9020 ON SRQ THEN 9120
9030 I7=0
9040 PRINT @A1: "INIT;TIM 100M;SIG;EOS ON"
9050 WBYTE @32+A1,8:
9060 T6=3
9070 GOSUB 19390
9080 PRINT @A1: "EOS OFF"
9090 IF I7<>1 THEN 9150
9100 ON SRQ THEN 19280
9110 GO TO 10000
9120 WBYTE @20:
9130 I7=1
9140 RETURN
9150 PRINT "GROUP EXECUTE TRIGGER...GET *** FAIL ***G"
9160 GO TO 19530
9170 REM
9180 REM
9190 REM
9200 REM
9210 REM
10000 REM *** SELECTED DEVICE CLEAR...SDC ***

```



```

10010 PRINT " *** SELECTED DEVICE CLEAR...SDC ***"
10020 PRINT @A1: "ID?"
10030 WBYTE @32+A1,4:
10040 WBYTE @64+A1:
10050 RBYTE R
10060 IF ABS (R )<>255 THEN 10080
10070 GO TO 11000
10080 PRINT " *** SELECTED DEVICE CLEAR.....SDC *** FAIL ***G"
10090 GO TO 19530
10100 REM
10110 REM
10120 REM
10130 REM
10140 REM
11000 REM *** DEVICE CLEAR.....DCL ***
11010 PRINT " *** DEVICE CLEAR.....DCL ***"
11020 PRINT @A1: "ID?"
11030 WBYTE @20:
11040 WBYTE @64+A1:
11050 RBYTE R
11060 IF ABS (R )<>255 THEN 11080
11070 GO TO 12000
11080 PRINT " *** DEVICE CLEAR.....DCL *** FAIL ***G"
11090 GO TO 19530
11100 REM
11110 REM
11120 REM
11130 REM
11140 REM
12000 REM ** ADDRESSED AS LISTENER, TALKER ***
12010 PRINT " *** 49XP ADDRESSED AS LISTENER.. ***"
12020 WBYTE @32+A1:76,79,82,68,79,-63
12030 T6=1
12040 GOSUB 19390
12050 INPUT @A1:V$
12060 T$=SEG (V$,16,1 )
12070 IF T$="L" THEN 12100
12080 PRINT "J *** 49XP ADDRESSED AS LISTENER *** FAIL ***G"
12090 GO TO 19530
12100 PRINT " *** 49XP ADDRESSED AS TALKER.... ***"
12110 PRINT @A1: "INIT;TIM 50M;SIG;SIG;WAI;LORDO?"
12120 INPUT @A1:V$
12130 T$=SEG (V$,16,1 )
12140 IF T$="T" THEN 13000
12150 PRINT " *** 49XP ADDRESSED AS TALKER *** FAIL ***"
12160 GO TO 19530
12170 REM
12180 REM
12190 REM
12200 REM
12210 REM
13000 REM *** SERIAL POLL ***
13010 PRINT " *** SERIAL POLL.....SPD/SPE ***"
13020 WBYTE @95,63,24,64+A1:
13030 RBYTE R

```

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```
13040 WBYTE @95,25:
13050 IF R=0 OR R=16 THEN 13080
13060 PRINT "J*** SERIAL POLL *** FAIL ***G"
13070 GO TO 19530
13080 T6=3
13090 GOSUB 19390
13100 REM
13110 REM
13120 REM
13130 REM
13140 REM
14000 REM *** GPIB INTERFACE REAR PANEL SWITCH TEST ***
14010 PAGE
14020 A1=2
14030 GOSUB 19000
14040 PRINT " O I O I O I O O O 1 O"
14050 GOSUB 19070
14060 GOSUB 19190
14070 PAGE
14080 A1=4
14090 GOSUB 19000
14100 PRINT " O I O I O I O O 1 O O"
14110 GOSUB 19070
14120 GOSUB 19190
14130 PAGE
14140 A1=8
14150 GOSUB 19000
14160 PRINT " O I O I O I O 1 O O O"
14170 GOSUB 19070
14180 GOSUB 19190
14190 PAGE
14200 A1=16
14210 GOSUB 19000
14220 PRINT " O I O I O I 1 O O O O"
14230 GOSUB 19070
14240 GOSUB 19190
14250 REM
14260 REM
14270 REM
14280 REM
14290 REM
15000 REM *** "LF" OR "EOI" SWITCH ***
15010 PAGE
15020 A1=1
15030 GOSUB 19000
15040 PRINT " O I O I 1 I O O O O 1"
15050 GOSUB 19070
15060 PRINT "JJTESTING" "LF" "OR" "EOI" "SWITCH"
15070 GOSUB 19190
15080 WBYTE @32+A1:73,68,63,10
15090 INPUT @A1:T$
15100 T$=SEG(T$,1,9)
15110 IF T$="ID TEK/49" THEN 15140
15120 PRINT "J" "LF" "OR" "EOI" "SWITCH *** FAIL ***G"
15130 GO TO 19530
```

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```

15140 T6=2
15150 GOSUB 19390
15160 REM
15170 REM
15180 REM
15190 REM
15200 REM
16000 REM *** TALK ONLY MODE ***
16010 PAGE
16020 GOSUB 19000
16030 PRINT " O I 1 I O I O O O O 1 "
16040 GOSUB 19070
16050 PRINT "JJJTESTING TALK ONLY"
16060 INPUT @A1:V$
16070 I7=POS (V$, "FINE OFF", 1 )
16080 IF I7<>0 THEN 17000
16090 PRINT "JJJTALK ONLY MODE *** FAIL ***G"
16100 GO TO 19530
16110 REM
16120 REM
16130 REM
16140 REM
16150 REM
17000 REM *** LISTEN ONLY MODE ***
17010 PAGE
17020 GOSUB 19000
17030 PRINT " 1 I O I O I O O O O 1 "
17040 GOSUB 19070
17050 PRINT "JJJTESTING LISTEN ONLY"
17060 PRINT @A1: "INI "
17070 T6=0.5
17080 GOSUB 19390
17090 WBYTE 82,69,70,32,-48
17100 PAGE
17110 GOSUB 19000
17120 PRINT " O I O I O I O O O O 1 "
17130 GOSUB 19070
17140 PRINT @A1: "REF?"
17150 INPUT @A1:V$
17160 IF V$<> "REFLVL +0.0" THEN 17180
17170 GO TO 18000
17180 PRINT "JJJLISTEN ONLY MODE *** FAIL ***G"
17190 GO TO 19530
17200 REM
17210 REM
17220 REM
17230 REM
17240 REM
18000 REM *** INTERFACE CLEAR AND REMOTE ENABLE TEST.....IFC & REN ***
18010 PAGE
18020 PRINT "JJJTESTING IFC (INTERFACE CLEAR), AND REN (REMOTE ENABLE)"
18030 WBYTE @32+A1:
18040 T6=3
18050 GOSUB 19390
18060 PRINT "JJCHECK THE 49XP CRT, FOR AN " "L" "BETWEEN THE VERTICAL "

```

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```

18070 PRINT "DISPLAY AND THE MIN RF ATTEN READOUTS."
18080 PRINT "JPRESS RETURN TO CONTINUE.";
18090 INPUT P$
18100 INIT
18110 PRINT "JIF AN "L" "IS STILL PRESENT, THE IFC LINE IS FAULTY,"
18120 PRINT "IF THE "L" "VANISHED, IFC TESTED OK."
18130 PRINT "JJCHECK ALSO THE 49XP FRONT PANEL FOR PROPER LOCAL CONTROL"
18140 PRI "IF THE FRONT PANEL IS LOCKED OUT, THE REN LINE IS FAULTY, IF"
18150 PRINT "NOT, REN TESTED OK"
18160 PRINT "JJGPIB VERIFICATION COMPLETEG"
18170 END
18180 REM
18190 REM
18200 REM
19000 REM *** REAR PANEL INTERFACE SWITCH TEST TEXT ROUTINE ***
19010 PRINT "SET GPIB ADDRESS SWITCHES TO:"
19020 PRINT "JJLISTENITALKILF ORI ADDRESS"
19030 PRINT " ONLYIONLYIEOII16 8 4 2 1"
19040 PRINT "-----I-----I-----I-----"
19050 RETURN
19060 REM
19070 REM *** REAR PANEL TEST TEXT ROUTINE ***
19080 PRINT "JJAFTER CHANGING THE SWITCHES, ";
19090 PRINT "PRESS THE REMOTE/LOCAL BUTTON ONCEJJ"
19100 PRINT "I (NOTE: IF YOU GET A GPIB INTERFACE ERROR MESSAGE,"
19110 PRINT "I IT MEANS THAT THE SWITCH (ES ) WEREN" T "
19120 PRINT "I READ CORRECTLY. TO RE-TEST, TYPE"
19130 PRINT "I "RUN" FOLLOWED BY THE LINE NUMBER IN THE"
19140 PRINT "I ERROR MESSAGE ) "
19150 PRINT "JJIPRESS RETURN <CR> WHEN DONE ";
19160 INPUT T$
19170 RETURN
19180 REM
19190 REM *** TEST ADDRESS SWITCH ***
19200 PRINT @A1: "ID?"
19210 INPUT @A1:T$
19220 T$=SEG (T$,1,9 )
19230 IF T$="ID TEK/49" THEN 19260
19240 PRINT "ADDRESS SWITCH TEST FAIL"
19250 GO TO 19530
19260 RETURN
19270 REM
19280 REM *** SRQ HANDLER ***
19290 T6=3
19300 GOSUB 19390
19310 POLL Z1,Z1;A1
19320 PRINT @A1: "ERR?"
19330 INPUT @A1:S$
19340 PRINT "GGAN INTERRUPT OCCURRED ON THE BUS, THE 49XP RETURNS ";S$
19350 PRINT "JPRESS RETURN <CR> TO CONTINUE ";
19360 INPUT T$
19370 RETURN
19380 REM
19390 REM *** DELAY GENERATOR ***
19410 REM *** T6 GIVEN IN SEC (GLOBAL ) *** I9 SCRATCH ***

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```
19420 IF T6<0 THEN 19510
19430 IF RND (0 )>0.5 THEN 19490
19440 REM *** 4051 ***
19450 T6=T6*220
19460 FOR I9=1 TO T6
19470 NEXT I9
19480 GO TO 19510
19490 REM *** 4052
19500 CALL "WAIT",T6
19510 T6=0
19520 RETURN
19530 REM **** FAILURE DECISION HANDLER ****
19540 PRINT "JJISELECT A UDK:"
19550 PRINT "I_ (1) RE-START"
19560 PRINT "I_ (5) END"
19570 SET KEY
19580 B2=0
19590 IF B2<>1 AND B2<>5 THEN 19590
19600 IF B2=5 THEN 19630
19610 PAGE
19620 GO TO 6000
19630 END
```

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ADJUSTMENT PROCEDURE

Introduction

If the instrument performance is not within specified requirements for a particular characteristic, determine the cause, repair if necessary, then use the appropriate adjustment procedure to return the instrument operation to performance specification. After any adjustment, verify performance by repeating that part of the Performance Check.

Allow the instrument to warm up for at least one hour, in ambient air of +20°C to +30°C before making any adjustments. Waveform illustrations in these instructions may be idealized and should not be referenced as representative of specification tolerances.

Adjustment steps that interact are noted and reference is made, within the procedure, to the affected circuit or steps.



STATIC DISCHARGE CAN DAMAGE MANY SEMICONDUCTOR COMPONENTS USED IN THIS INSTRUMENT.

Many semiconductor components, especially MOS types, can be damaged by static discharge. Damage may not be catastrophic, therefore, not immediately apparent. It usually appears as a 'weakening' of the semiconductor characteristics. Devices that are par-

ticularly susceptible are: MOS, CMOS, JFETs, and high impedance operational amplifiers. Damage can be significantly reduced by observing the following precautions.

1. Handle static-sensitive components or circuit assemblies at or on a static-free surface. Work station areas should contain a static-free bench cover or work plane such as conductive polyethylene sheeting and a grounding wrist strap. The work plane should be connected to earth ground.
2. All test equipment, accessories, and soldering tools should be connected to earth ground.
3. Minimize handling by keeping the components in their original containers until ready for use. Minimize the removal and installation of semiconductors from their circuit boards.
4. Hold the IC devices by their body rather than the terminals.
5. Use containers made of conductive material or filled with conductive material for storage and transportation. Avoid using ordinary plastic containers. Any static sensitive part or assembly (circuit board) that is to be returned to Tektronix, Inc., should be packaged in its original container or one with anti-static packaging material.

ADJUSTMENT STEPS

Step		Page
1.	Check and adjust low voltage power supply	5-2
2.	Crt display	5-4
3.	Deflection Amplifier (gain and frequency response)	5-6
4.	Adjust sweep timing	5-8
5.	Frequency control system calibration	5-9
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12.	IF gain calibration	5-21
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15.	Preselector Driver calibration	5-24
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19.	Phase lock calibration	5-32

Preparation

To prepare the rackmount or benchtop version for adjustment, refer to the Rackmount/Benchtop Versions part of the Options section of this manual (Section 8).

Remove the cabinet of the 494/494P as follows.

1. Set the 494/494P on its face or front panel.
2. Loosen the four screws through the back rubber feet.
3. Pull the cover up and off of the 494/494P.
4. Place the instrument on the bench and reconnect the power cord.

Some circuit boards or assemblies must be removed and placed on extenders to gain access to some test points or adjustments. When this is done, turn the power off before removing the assembly.

1. Check and Adjust Low Voltage Power Supply

This high-efficiency power supply uses an internal oscillator with a frequency of 66 kHz. The frequency adjustment is normally required only after replacing oscillator components; therefore, Part 1 is the normal adjustment and check procedure, Part 2 of this step should only be required after repair of the assembly.

WARNING

The 494/494P uses a high efficiency power supply, with the primary ground potential different from chassis or earth ground. An isolation transformer, with a turns ratio of 1:1 and a 500 VA minimum rating, should be used between the power source and the 494/494P power input receptacle. The transformer must have a three-wire input and output connector with ground through the input and output. Stancor GIS21000 is an example of a suitable transformer. A jumper should also be connected between the primary ground side to chassis ground (emitter of Q2061 and the ground terminal of the input filter FL301.

If the power supply is separated from the instrument and operated on the bench, hazardous potentials exist within the supply for several seconds after power is disconnected. This is due to the slow discharge of capacitors C6101 and C6111. A relaxation oscillator lights DS5112 (next to C6111) when the potential exceeds 80 V.

PART 1

Check and Adjust Low Voltages

(1) Connect a Variac (line voltage regulator) in line with the 494/494P power input and set the Variac for 117 Vac. Remove the metal cover over the Z-Axis and Sweep boards.

(2) Connect a digital voltmeter (DVM) to +15 V test point (Figure 5-1B) on the Z-Axis board to monitor the +15 V supply.

(3) Remove the Power Supply cover screw, located below the 10 MHz IF Output jack on the rear panel (see Figure 5-1A). This will provide access to adjustment R6028.

(4) Insert a narrow-bit screwdriver through the screw hole to engage adjustment R6028 and adjust it for +15 V on the DVM.

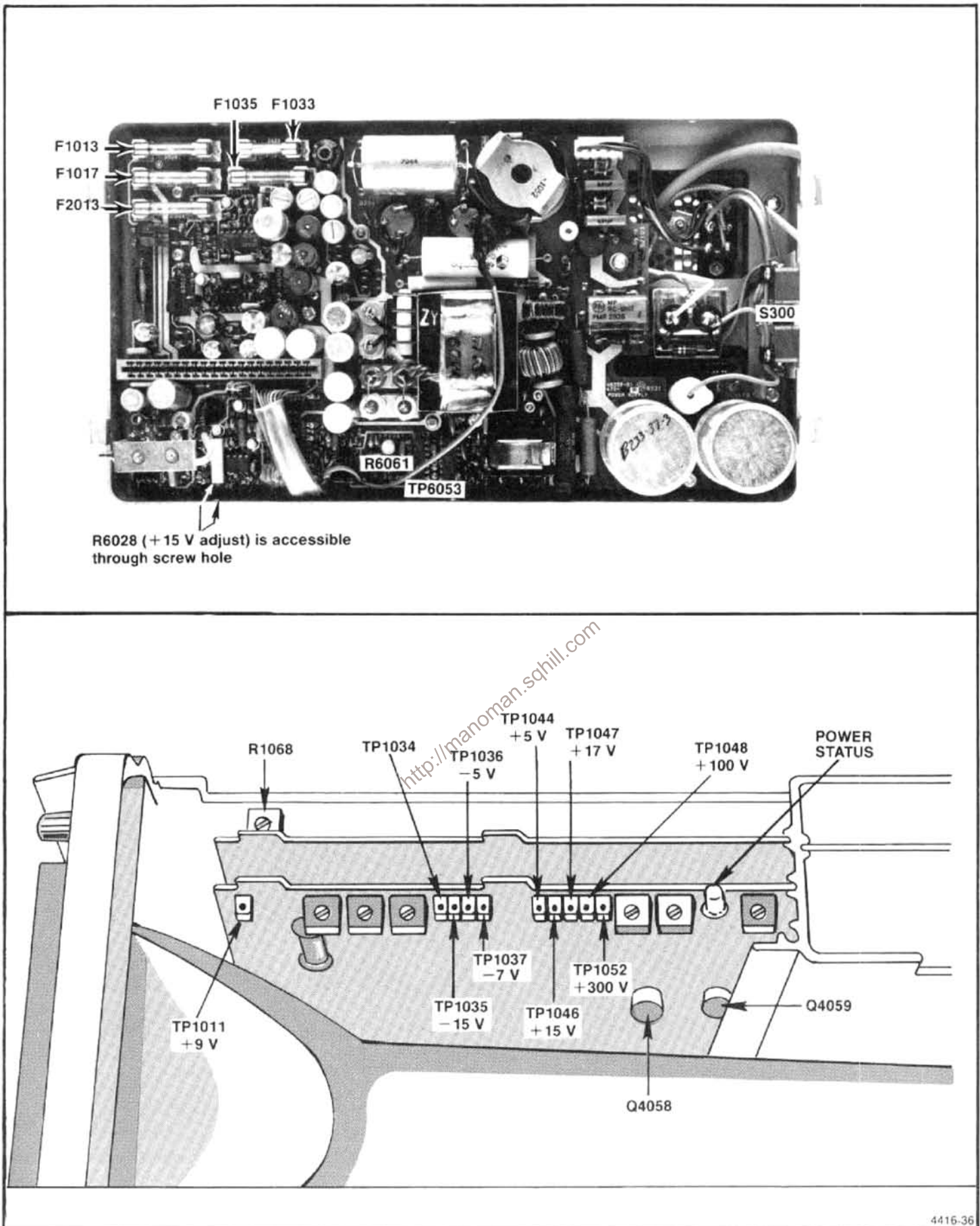


Figure 5-1. Low voltage power supply adjustments and test point locations.

(5) Vary the input voltage from 90 to 132 Vac and note that the +15 V supply remains regulated.

(6) Check the other supply voltages at the test points indicated in Figure 5-1B, against tolerances listed in Table 5-1.

(7) Remove the line voltage regulator (Variac) and re-connect the 494/494P directly to the power source.

**Table 5-1
POWER SUPPLY VOLTAGE TOLERANCES**

Supply	Tolerance
+9 V	+8.5 V to +10.5 V
-5 V	-4.8 V to -5.2 V
-7 V	-7 V to -8.5 V
-15 V	-14.85 V to -15.15 V
+5 V	+4.8 V to +5.2 V
+17 V	+16.8 V to +18.6 V
+100 V	+95 V to +105 V
+300 V	+280 V to +310 V

PART 2

Adjusting the Power Supply Oscillator Frequency

(1) Remove the Power Supply module, as described in the Maintenance section, then remove the Power Supply module cover and disconnect P3045.

(2) Plug the power cord into the power input receptacle and connect it to a suitable power source (115 Vac or 230 Vac, depending on the position of S302).

(3) Use a plastic or insulated tuning tool or equivalent, to insert between the two on/off power switches (S300) to close these switches (Figure 5-1).

(4) Connect a test oscilloscope probe, with a deflection sensitivity of 5 V/div and sweep rate of 10 μ s/div to TP6053 (Figure 5-1). Note the amplitude of the output waveform, of the oscillator U6059, is approximately 10 V.

(5) Adjust R6061 (Oscillator Freq Adj) for a waveform period of 15 μ s (66 kHz).

(6) Reconnect P3045 and replace the Power Supply module cover, then re-install the module on the 494/494P.

2. Crt Display (Z-Axis and High Voltage Circuits)

a. Switch POWER off and preset the INTENSITY control fully counterclockwise, MANUAL SCAN to midrange, and TIME/DIV to MNL position. Remove the cover over the Z-Axis and Sweep board. Set the Intensity Limit R1027, on the Z-Axis board (Figure 5-2) fully counterclockwise and Crt Bias R2040, on the High Voltage board (Figure 5-3) fully clockwise.

b. Switch POWER on and after the power-up state has stabilized, change the Vertical Display mode to 2 dB/DIV. Deactivate READOUT and VIEW A, VIEW B for no digital storage.

c. Adjust Crt Bias as follows:

(1) Using a voltmeter in the 20 volt range, measure and record the collector voltage of Q4058 or Q4059 (Figure 5-1A) on the Z-Axis board.

(2) Turn the INTENSITY clockwise until a crt beam dot appears on screen.

(3) Focus by adjusting R3033 on the High Voltage board (Figure 5-3) for the smallest round dot.

(4) Set the INTENSITY for a collector voltage 5.5 V higher than the voltage noted in part 1.

(5) Use the non-metallic screwdriver to adjust Crt Bias, R2040, counterclockwise until the crt beam is visible, then clockwise until the beam dot just extinguishes, with the screen shaded. (If no dot appears, with the adjustment fully counterclockwise, this will be the bias setting.)

(6) Turn the INTENSITY clockwise until a dot is visible then defocus the dot with the Focus adjustment R3033. Adjust Astigmatism R1058 (Figure 5-2) for a round dot then refocus with R3033 for the smallest sharpest dot.

(7) Turn the INTENSITY counterclockwise until the dot just disappears and again measure the collector voltage of Q4058 or Q4059. Voltage should equal or exceed the voltage noted in part 4. If the voltage is less, repeat the procedure for setting crt bias.

d. Adjust the crt cathode current as follows:

(1) Switch POWER off then remove P4036 (Figure 5-3) on the High Voltage board. Turn INTENSITY fully clockwise, MANUAL SCAN fully counterclockwise, and ensure that the TIME/DIV is in the MNL position. Set the Intensity Limit R1027, on the Z-Axis board, (Figure 5-2) fully clockwise.

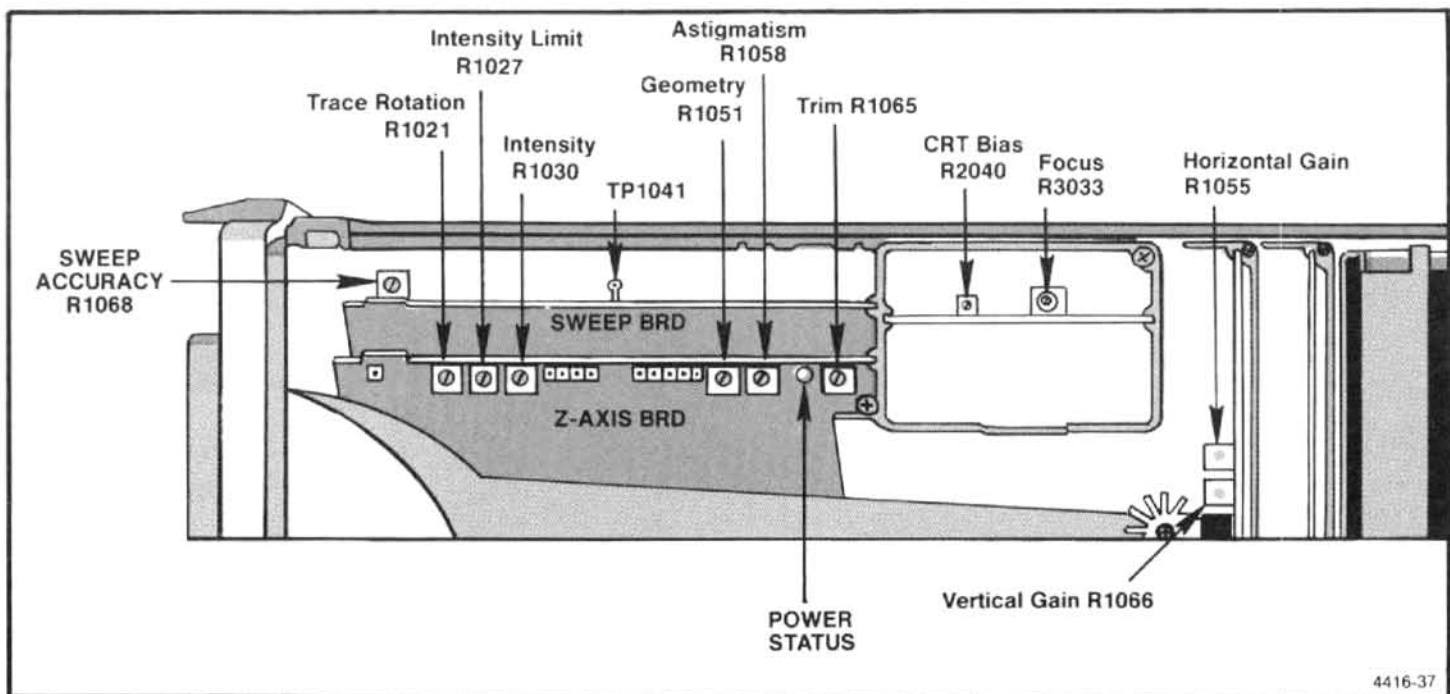


Figure 5-2. Location of adjustments and test points on the Deflection Amplifier board, High Voltage module, Z-Axis board, and Sweep board.

(2) Connect the voltmeter between TP4028 (Figure 5-3) and the ground lug on the crt shield.

(3) Switch POWER on. After the instrument initializes, activate 2 dB/DIV and switch Digital Storage off.

(4) Adjust Intensity Limit R1027 (Figure 5-2) for a voltage reading of 0.9 volts at TP4028.

(5) Switch POWER off and re-install the jumper P4036 on the High Voltage board. Turn POWER on and adjust the INTENSITY for normal viewing.

e. Apply the CAL OUT signal to the RF INPUT and set FREQUENCY to 100 MHz, FREQ SPAN/DIV to 10 MHz, TIME/DIV to AUTO, and REF LEVEL to -20 dBm. Activate 2 dB/DIV, AUTO RESOLN, NARROW Video Filter, and switch VIEW A and VIEW B off.

f. Activate ZERO SPAN and adjust REFERENCE LEVEL until the trace is approximately mid-screen; then adjust Trace Rotation R1021 (Figure 5-2) so the trace is aligned with the graticule lines.

g. Activate VIEW A and VIEW B then use the PEAK/AVERAGE cursor, positioned at the top then bottom of the screen, as a reference line to adjust Geometry R1051 (Figure 5-2) for the straightest trace at top and bottom of the screen.

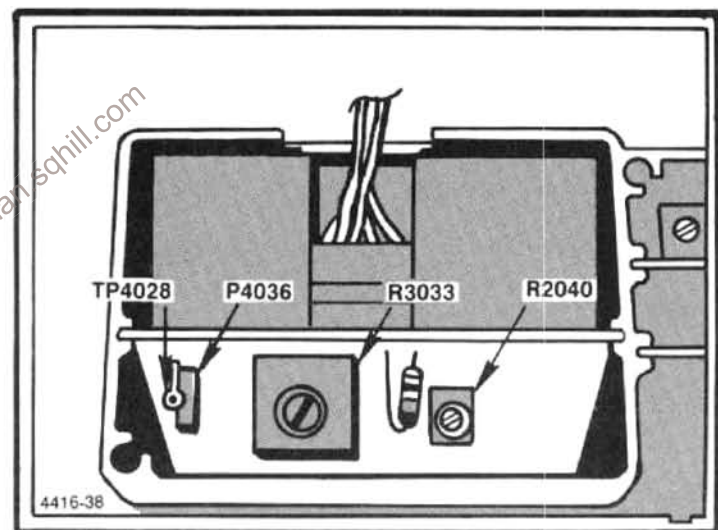


Figure 5-3. Location of test points and adjustments on the High Voltage module.

h. Change the REF LEVEL to position the trace within the graticule area with Vertical Display mode of 2 dB/DIV. Adjust INTENSITY so the trace is just visible.

i. Adjust Δ Intensity R1030 (Figure 5-2) so the brightness of the readout characters is slightly higher than the trace. Readout characters should be just visible after the trace has disappeared. This ratio provides the best setting for photograph purposes. Disconnect CAL OUT signal from the RF INPUT.

3. Deflection Amplifier (gain and frequency response)

a. Test equipment setup is shown in Figure 5-4. Set the TIME/DIV to 1 ms. Position the trace on the bottom graticule line.

b. Apply a 500 kHz signal, with an amplitude of 0 to +4 V, from the sine-wave generator, to the Ext MARKER/VIDEO input. Connect a jumper between pin 1 (Ext Video Select) and pin 5 (ground) of the ACCESSORIES jack (Figure 5-4). Deactivate VIEW A and VIEW B and set Triggering to INT.

c. Adjust Vert Gain R1066 (Figure 5-2) for a full screen display.

d. Disconnect the 500 kHz signal from the MARKER/VIDEO input. Remove the jumper between pins 1 and 5 of the ACCESSORIES connector if you are not going to adjust sweep timing (step 4). Set Triggering to FREE RUN.

e. Set TIME/DIV to MNL, connect a digital voltmeter (DVM) to TP1041, on the Sweep board (Figure 5-2) and adjust MANUAL SCAN for 0.0 V at TP1041. Adjust Horizontal Position control to center the Crt beam.

f. Adjust MANUAL SCAN for a reading of +5 V at TP1041. Now adjust Horiz Gain R1055 (Figure 5-2) to position the crt beam to the right graticule edge (10th graticule line).

g. Adjust MANUAL SCAN so crt beam moves to the left edge of the graticule and check that the voltage at TP1041 is now approximately -5.0 V.

h. Disconnect the DVM, set TIME/DIV to AUTO, change the test oscilloscope to Ext Trigger and apply the Readout Off signal, at TP1038 on the Crt Readout board (Figure 5-5), to the test oscilloscope Ext Trigger input. Set test oscilloscope Time/Div to 2 μ s.

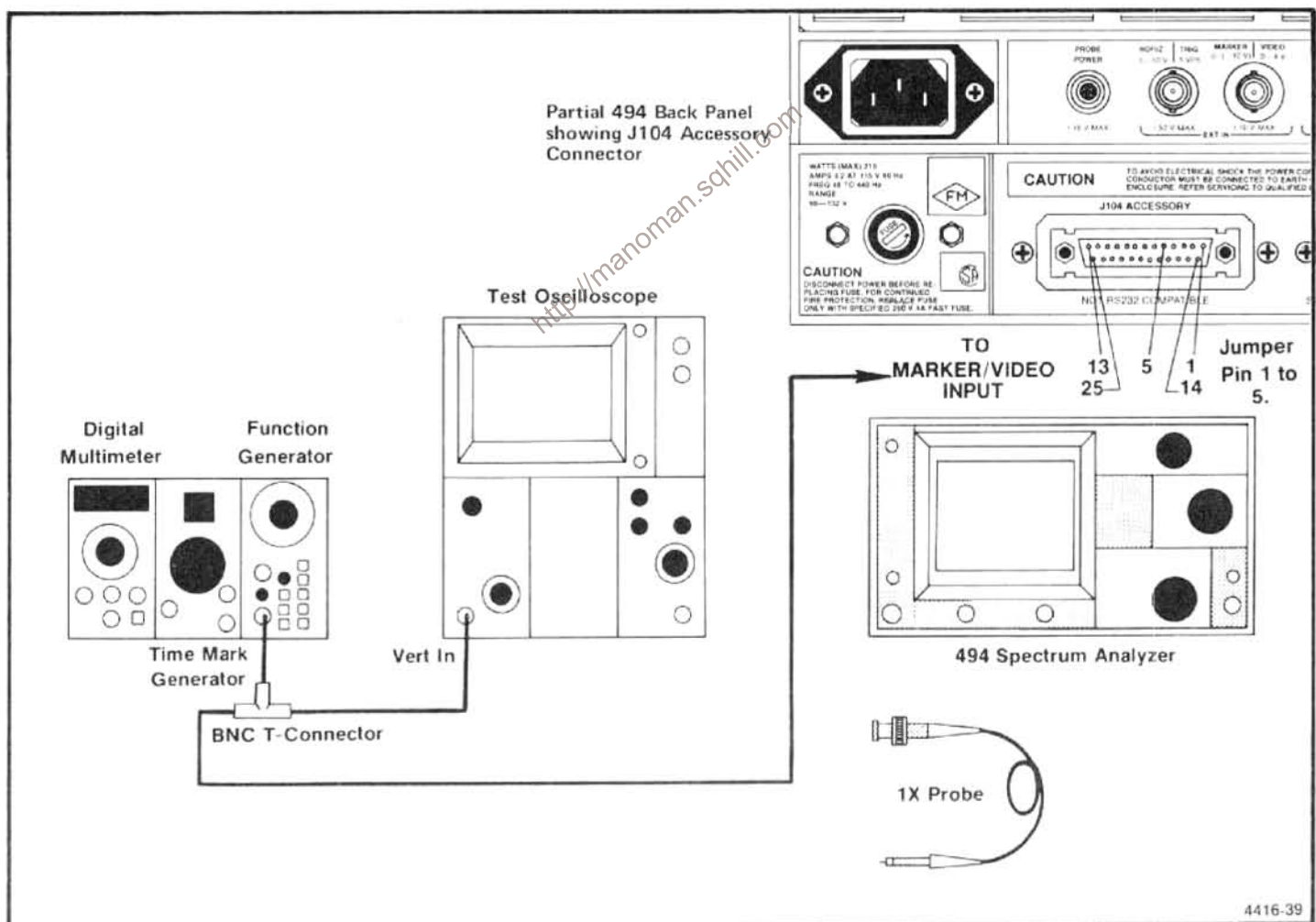


Figure 5-4. Test equipment setup for calibrating the Deflection Amplifier.

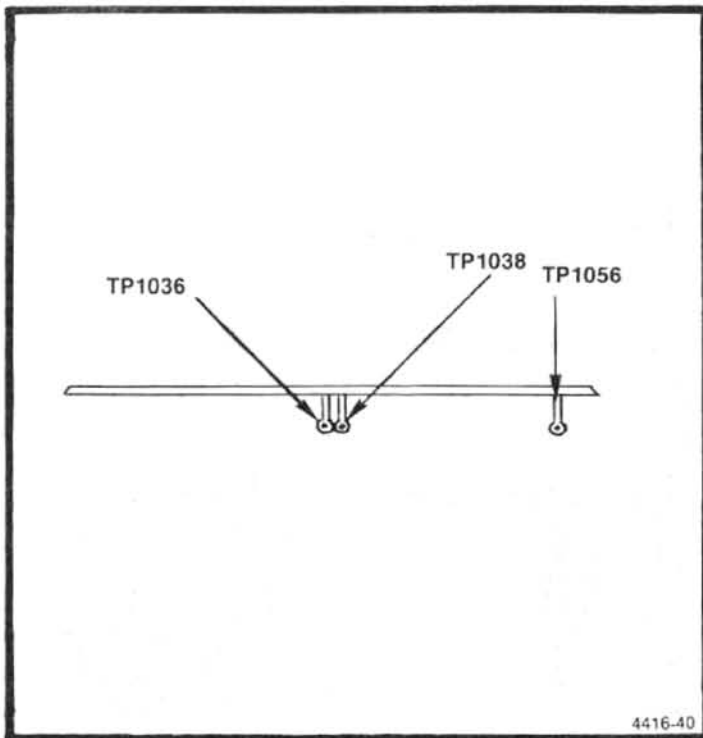


Figure 5-5. Test points on the Crt Readout board.

i. Adjust the controls for a triggered sweep then switch the 494/494P sweep off by activating SINGLE SWEEP, and ensure READOUT is on.

j. Connect the test oscilloscope probe to the collectors of Q1031 and Q1024, on the Deflection Amplifier board (see Figure 5-6). Adjust C5021 for the best frequency response (no overshoot or rolloff).

k. Connect the probe to the collectors of Q1043 and Q1049, on the Deflection Amplifier board and adjust C4057 (Figure 5-6) for the best response.

l. Connect the probe to the collectors of Q1072, Q2078 (Figure 5-6) and adjust C4061 for the best response.

m. Connect the probe to the collectors of Q1095, Q2096 (Figure 5-6) and adjust C5104 for best response.

n. Disconnect the connection to TP1038 and the test oscilloscope probe. Check the appearance of "Z" in GHz of the frequency readout. If necessary, adjust C5104 and C4061 (vertical output) for the straightest top on the Z.

o. Set the Vertical Display to LIN and adjust REF LEVEL for 100 μ V. Set TIME/DIV to MNL and adjust MANUAL SCAN fully clockwise.

p. Adjust C5021 and C4057 for best REF LEVEL readout (straightest letters and numerals).

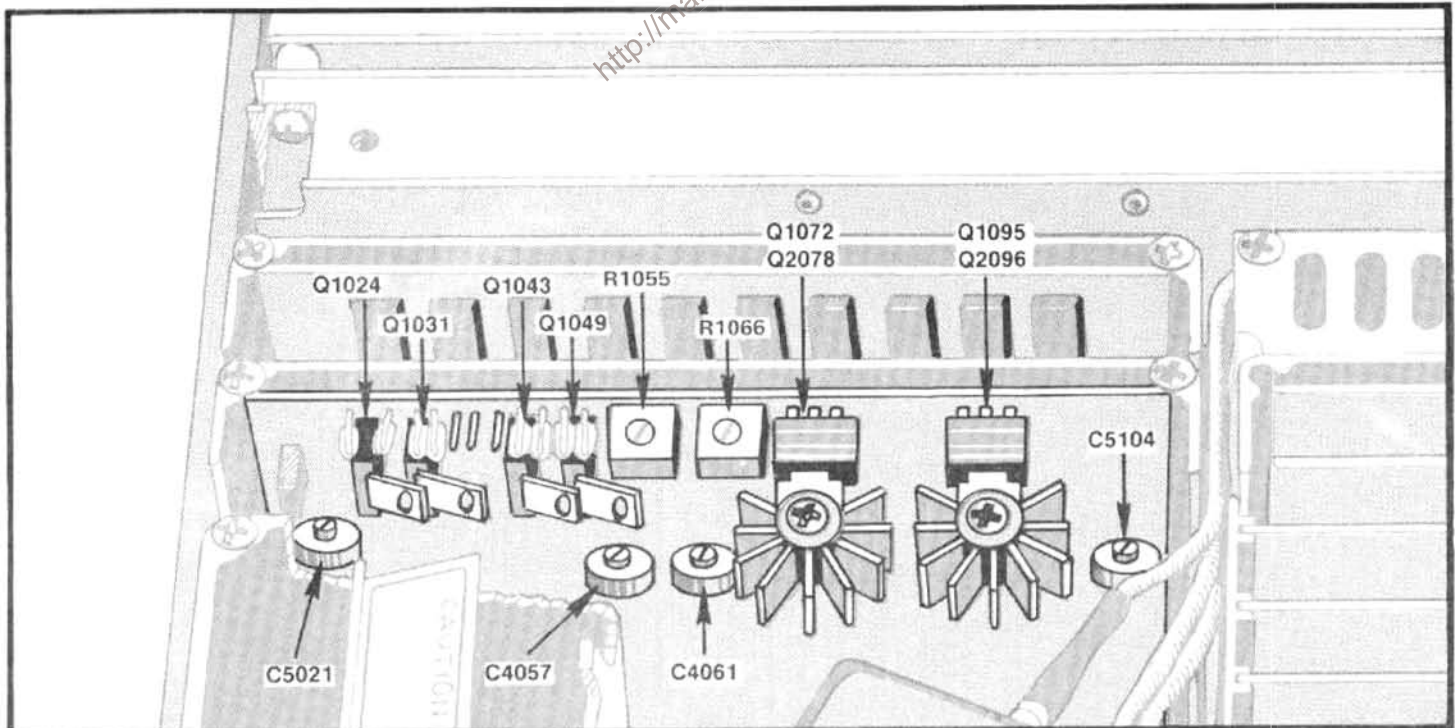


Figure 5-6. Test points and adjustments on the Deflection Amplifier for gain and frequency response.

4. Adjust Sweep Timing

a. Test equipment setup is shown in Figure 5-7. Select EXT Triggering, TIME/DIV of 10 ms, and a FREQ SPAN/DIV of 10 MHz or less. Digital Storage (VIEW A and VIEW B) must be off.

b. Apply 10 ms time marks from the time-mark generator to the EXT MARKER/VIDEO connector and connect a jumper between pins 1 and 5 of the ACCESSORIES connector. Apply the Trigger Output of the time-mark generator to the TRIG/HORIZ input, on the back panel of the 494/494P. This should provide a display of 10 ms markers.

c. Adjust Sweep Timing R1068 (see Figure 5-8) for 1 marker/division. (Use Horizontal Position adjustment to align markers with graticule lines.)

d. Check the accuracy of the remaining TIME/DIV selections. Error over the center eight divisions must not exceed $\pm 5\%$.

e. Set the TIME/DIV to AUTO, FREQ SPAN/DIV to MAX, and activate AUTO RESOLN.

f. Check the Time/Div versus Resolution Bandwidth as per Table 5-2, for all FREQ SPAN/DIV settings.

g. Return Triggering to FREE RUN. Disconnect the time-mark generator markers and trigger signal to the 494/494P. Remove the jumper between pins 1 and 5 of the ACCESSORIES connector. Reposition the trace if moved in part c.

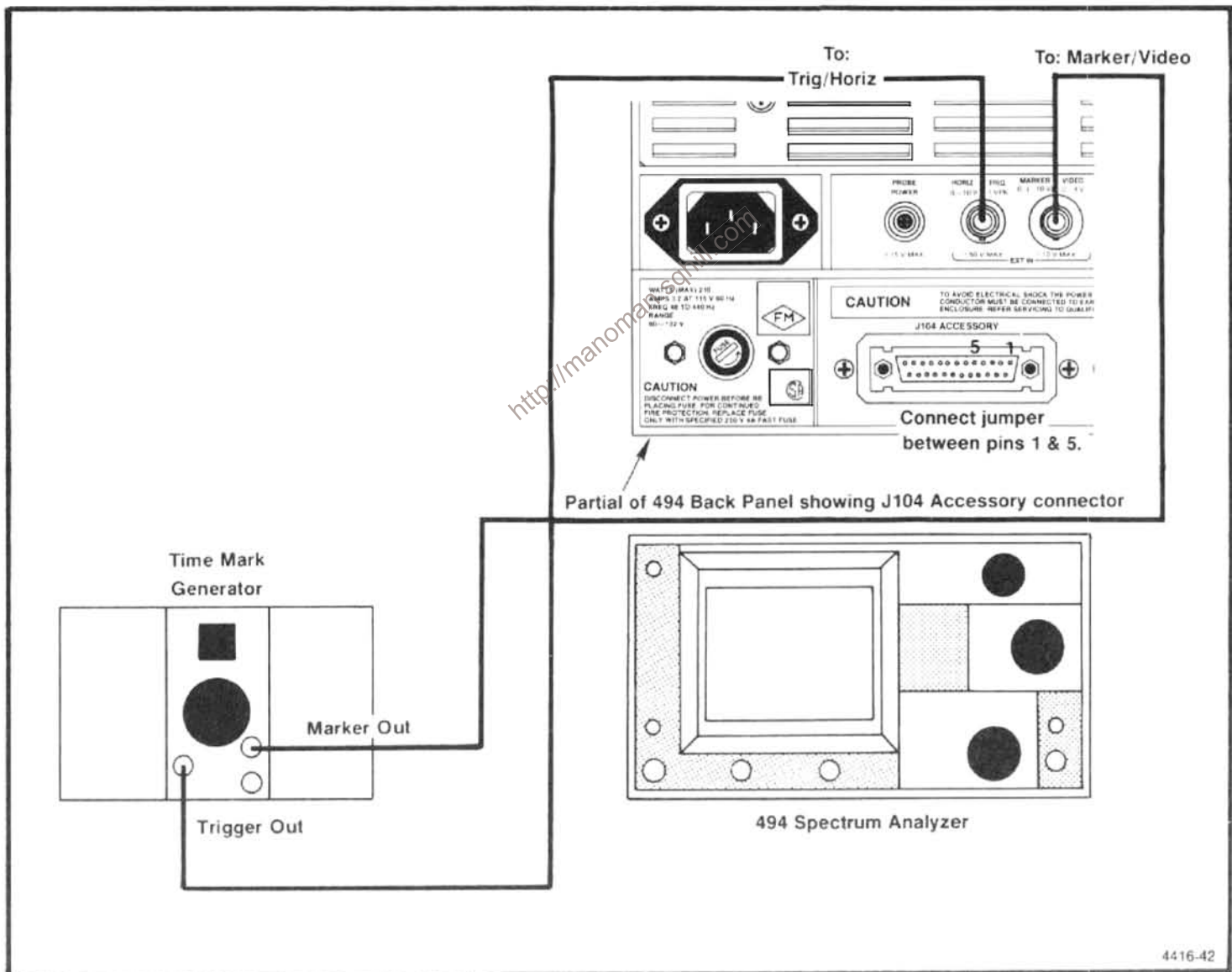


Figure 5-7. Test equipment setup for calibrating sweep timing.

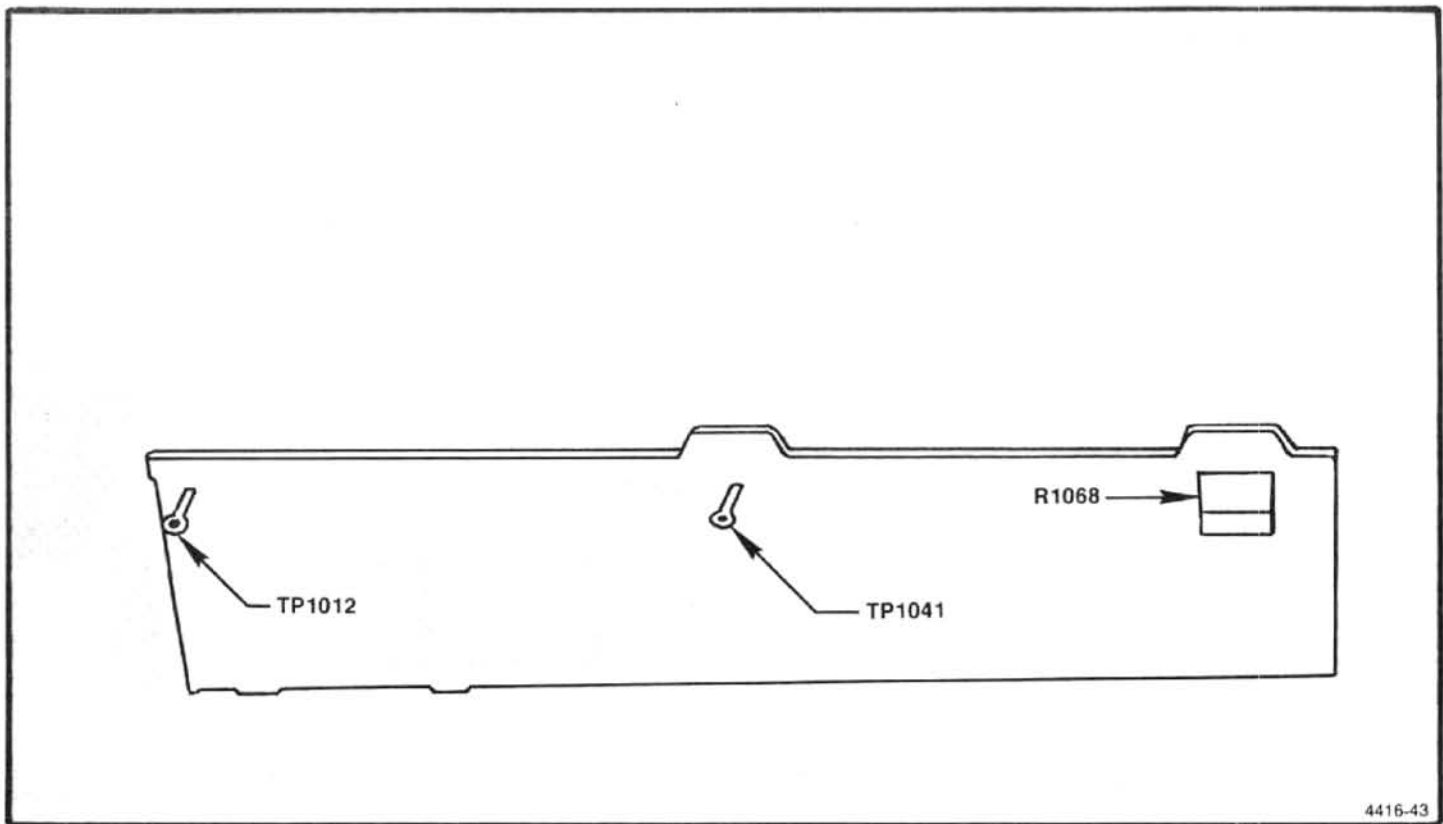


Figure 5-8. Timing adjustments and test points on the Sweep board.

Table 5-2
SWEEP RATE AS A FUNCTION OF SPAN
IN THE AUTO MODE

FREQ SPAN/DIV	TIME/DIV	RESOLUTION BANDWIDTH
MAX	50 ms	1 MHz
200 MHz	20 ms	1 MHz
100 MHz	10 ms	1 MHz
50 MHz	10 ms	1 MHz
20 MHz	10 ms	1 MHz
10 MHz	10 ms	1 MHz
5 MHz	10 ms	1 MHz
2 MHz	10 ms	100 kHz
1 MHz	10 ms	100 kHz
500 kHz	10 ms	100 kHz
200 kHz	50 ms	10 kHz
100 kHz	20 ms	10 kHz
50 kHz	10 ms	10 kHz
20 kHz	10 ms	10 kHz
10 kHz	100 ms	1 kHz
5 kHz	50 ms	1 kHz
2 kHz	20 ms	1 kHz
1 kHz	1 s	100 Hz
500 Hz	.5 s	100 Hz
200 Hz	.2 s	100 Hz
100 Hz	.5 s	30 Hz
50 Hz	.5 s	30 Hz

5. Frequency Control System Calibration

The 494/494P has a procedure in firmware for calibrating the frequency control system. However, it is possible that some adjustments may be misadjusted enough to cause the microcomputer to display an error message. If this occurs bypass the step then return to the calibration routine.

The adjustment tool for this step should be a long (6 inches), small diameter (1/8 inch), non-metallic screwdriver so adjustments mounted on the lower portion of the boards can be accessed, otherwise the CF Control board must be removed and mounted on an extender.

a. Test equipment is shown in Figure 5-9. Set the FREQUENCY to 0.0 MHz, FREQ SPAN/DIV to 5 MHz, and Triggering to FREE RUN.

b. Connect a shorting strap from TP1035, on the Span Attenuator board, to chassis ground (Figure 5-10). Connect the DVM between TP1073 and ground.

c. Adjust Sweep Offset R1063 (Figure 5-10) for 0.00 V.

d. Remove the shorting strap and set switch #3 of S1038 on the Memory board, (Figure 5-11) to the open (1) position. Set FREQ SPAN/DIV to 5 MHz. (This enables the calibration mode and diagnostic functions that are in the internal firmware.) Press <SHIFT> PULSE STRETCHER and select "0" (Overall System calibration) from the menu. Perform the calibration steps in the directory to the Phase Lock Synthesizer portion ("Connect a DVM to pin B on the Controlled Oscillator board and ground"), then press <SHIFT> to abort.

(1) If a "Calibration Step Cannot Be Completed" message is displayed, bypass the step, perform the other adjustments then return to the adjustment and try to bring the adjustment in range. If this doesn't take care of the problem, refer to; Troubleshooting the Frequency Control System procedure, in the Maintenance section.

(2) Disable the diagnostic mode by setting switch #3 of S1038 on the Memory board to the close (0) position.

e. Adjust 1st LO Sweep as follows:

(1) Apply the CAL OUT signal to the RF INPUT, set the FREQUENCY to 600 MHz, FREQ SPAN/DIV to 100 MHz and adjust REF LEVEL to display the markers.

(2) Adjust Tune Coil Swp R1065, on the Span Attenuator board (Figure 5-10) for one marker per division over

the center eight divisions of the graticule. Adjust the CENTER FREQUENCY as necessary to align the markers.

(3) Remove the Calibrator signal and apply 0.2 μ s time marks from the time mark generator to the RF INPUT.

(4) Set the FREQ SPAN/DIV to 5 MHz, REF LEVEL to +10 dBm, and FREQUENCY to about 10 MHz.

(5) Adjust the 1st LO FM Coil Swp, R1071 (Figure 5-10), for 1 marker/division over the center eight divisions of the display.

f. Max Span Dot (Offset to align dot with display).

(1) Disconnect the CAL OUT signal from 492 RF INPUT. Set FREQUENCY to 0.00 GHz, FREQ SPAN/DIV to MAX, and activate AUTO RESOLN. Switch VIEW A and VIEW B Off.

(2) Select a value for R1028, on the 1st LO Driver board (Figure 5-12), to set the frequency dot marker directly on the start spurious response.

NOTE

Increasing the value of R1028 will move the Dot to the right. Changing the resistance 1k will move the dot approximately 1 minor division.

(3) Apply the CAL OUT signal to the RF INPUT. Press <SHIFT> FREQ and enter 1.8 GHz, set FREQ SPAN/DIV to MAX, REF LEVEL to -30 dBm and check that the dot marker is over the 1.8 GHz marker ± 0.5 minor division.

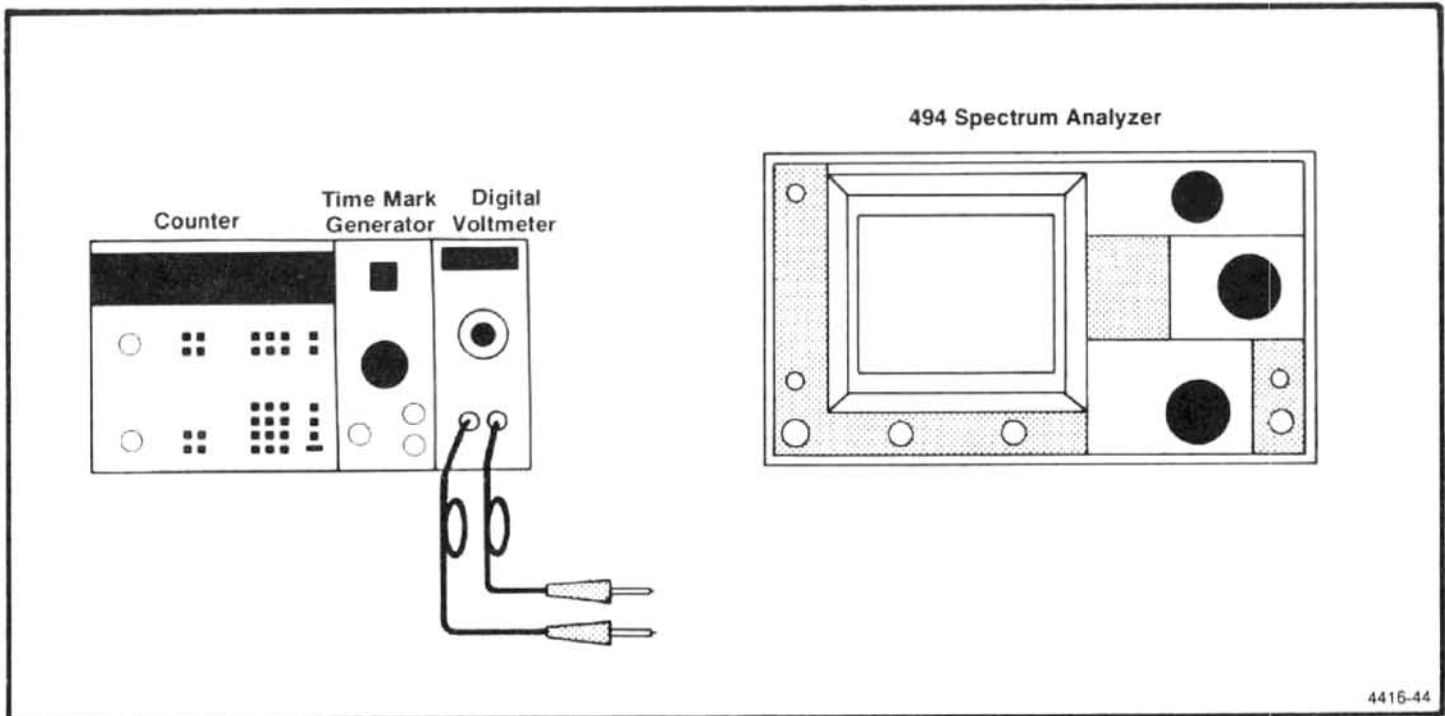


Figure 5-9. Test equipment setup for calibrating the frequency control system.

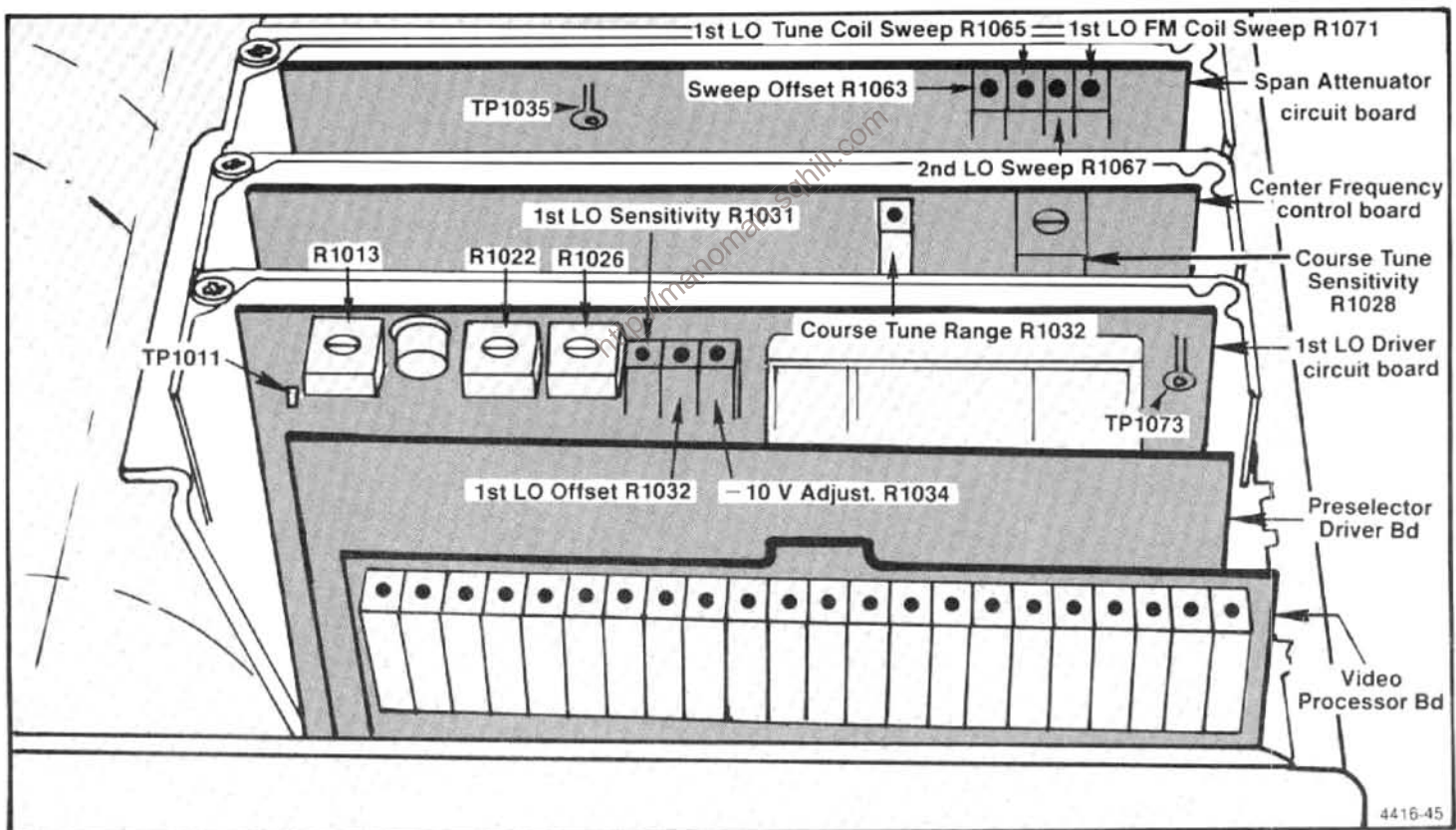


Figure 5-10. Adjustment and test point locations for calibrating the frequency control system.

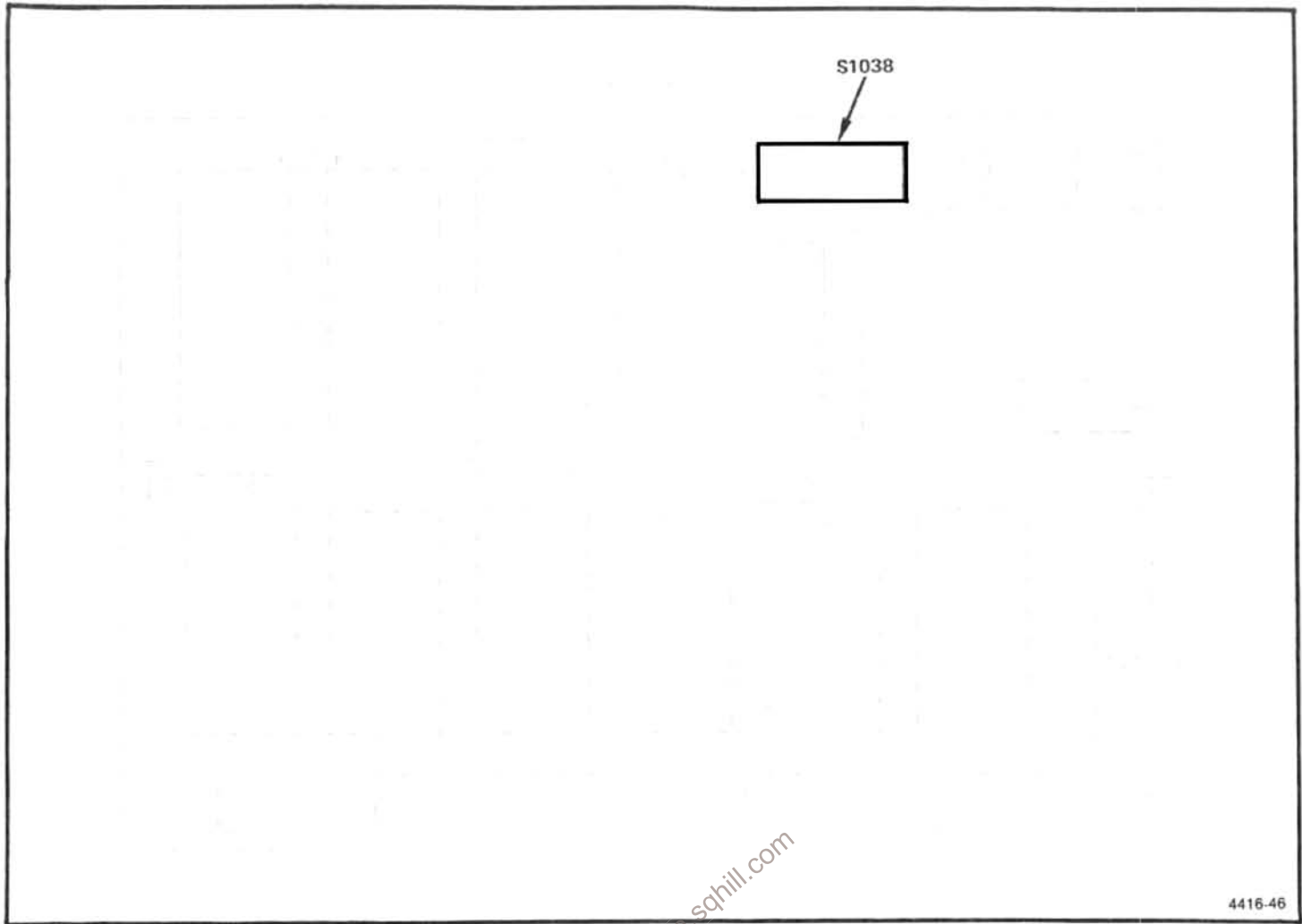


Figure 5-11. Location of Option switch S1038 on the Memory board.

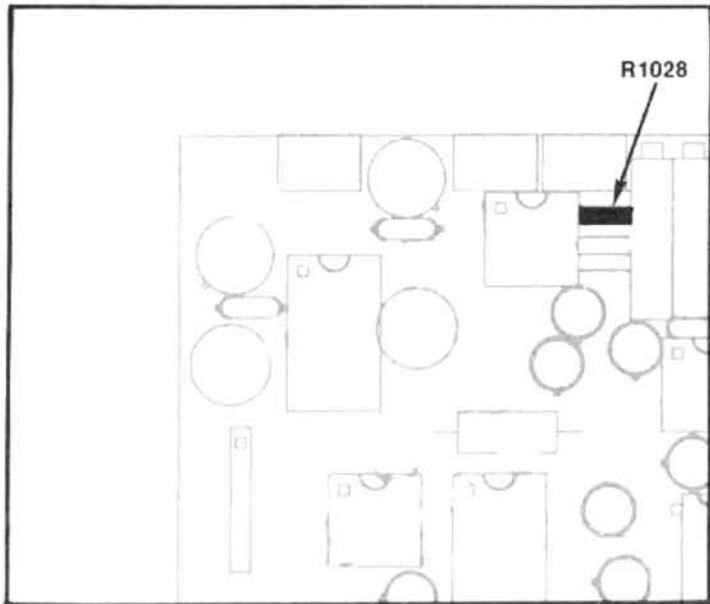


Figure 5-12. Location of select resistor R1028 on the 1st LO Driver.

6. Adjust Start (0 Hz) Response Amplitude and Mixer Bias

This adjustment should only be done if frequency response problems are encountered.

- a. Set the FREQUENCY to 2.0 MHz, FREQ SPAN/DIV to 200 kHz, RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to -30 dBm, and activate WIDE Video Filter.
- b. Connect a DVM between TP1011, on the 1st LO Driver board (Figure 5-13) and ground (crt shield). Adjust R1013 (Figure 5-13) for -1.0 V.
- c. Apply a calibrated -13 dBm 2 MHz signal to the RF INPUT (input to 1st mixer is now -13 dBm).
- d. Activate SAVE A to save the 2 MHz, -13 dBm signal as a reference.

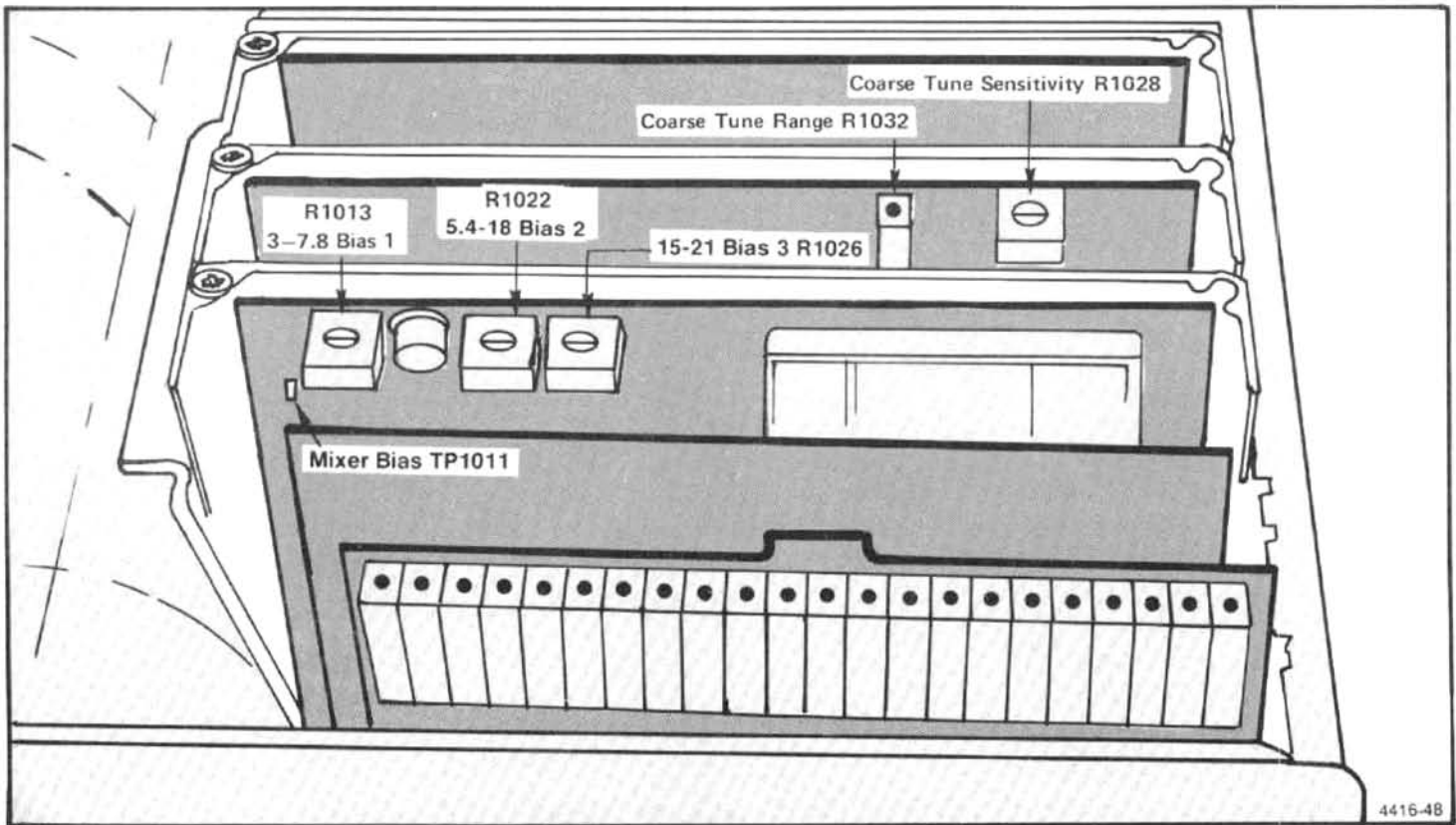


Figure 5-13. Adjustment and test points on the 1st LO Driver board.

e. Change the FREQUENCY to 0.0 MHz to bring the start (0 Hz) response to center screen.

f. Adjust R1013 for a null in the amplitude of the 0 Hz response. (DO NOT exceed 0.1 V positive when adjusting for a null because this will degrade flatness.) Use a thin screw driver to adjust the tuning screw on the 1st Mixer Diode assembly A12A1. (The tuning screw is towards the rear of the instrument, see Figure 5-14.) Alternately adjust R1013 and the tuning screw for minimum amplitude.

CAUTION

Care should be taken to not force the tuning screw past the point where it bottoms out. The null should occur about a full turn from the bottom.

g. The start (0 Hz) response should now be narrower than the 2 MHz reference signal. Turn the diode mixer tuning screw counterclockwise until the start spur response width equals the 2 MHz, -13 dBm reference. The amplitude level is now -13 dBm. This will provide the best overall flatness. Remove the 2 MHz signal from the RF INPUT and deactivate SAVE A and WIDE Video Filter.

7. Adjust 1st Converter Bias

NOTE

These adjustments should only be necessary if frequency response or flatness problems on Bands 4 and 5, are encountered. Bias 1 for the fundamental bands is adjusted in the previous step.

- a. Connect the DVM between TP1011, on the 1st LO Driver board, and ground. Increase the FREQUENCY RANGE to Band 4 (5.4-18 GHz).
- b. Adjust R1022 (Bias 2) for -0.25 V at TP1011.
- c. Change the FREQUENCY RANGE control to Band 5 (15-21 GHz).
- d. Adjust R1026 (Bias 3) for -0.25 V at TP1011.
- e. Perform the frequency response check in the Performance Check section. If the instrument fails to meet specifications, adjust the respective bias slightly from these initial settings and recheck frequency response.

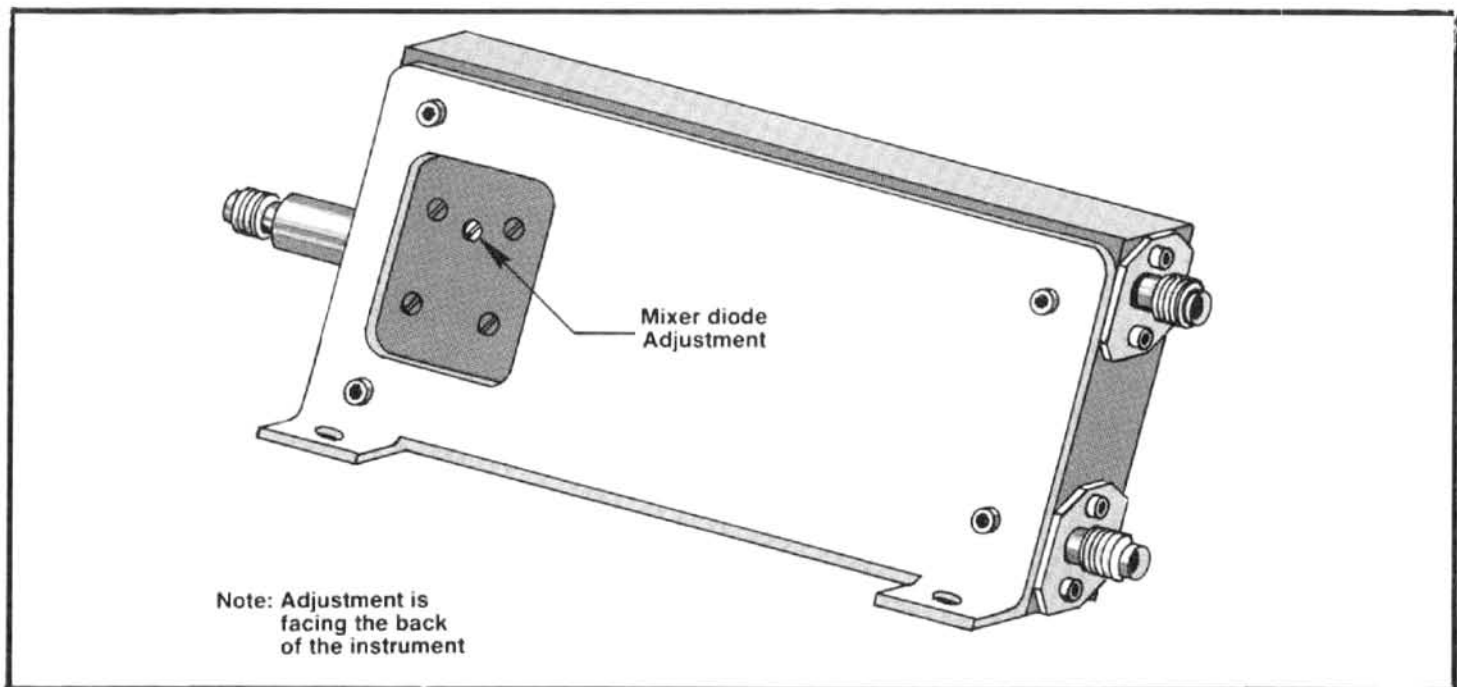


Figure 5-14. Location of the 1st Mixer tuning adjustment.

8. Log Amplifier Calibration



Use only an insulated screwdriver or tuning tool, such as Tektronix Part No. 003-0675-00, to make these adjustments.

a. Before calibrating the Log Amplifier, set the correction factors to zero. Press <SHIFT> 10 dB/DIV and select "SET CORRECTION FACTORS TO ZERO". Remove Leveler Disable plug P3035 on the Video Processor board (Figure 5-15).

b. Switch POWER off. Remove the Log Amplifier and Detector board assembly from the instrument then remove the shield so adjustments are accessible. Replace the assembly in the instrument and switch POWER on.

c. Test equipment setup is shown in Figure 5-16. Set the REF LEVEL to -60 dBm, FREQUENCY to 2 MHz, FREQ SPAN/DIV to 2 MHz, and the TIME/DIV to 10 ms. Activate AUTO RESOLN and 10 dB/DIV.

d. Center the two front panel LOG and AMPL CAL adjustments. Remove P621 and apply a 10 MHz, $+6$ dBm,

signal from the signal generator through 10 dB and 1 dB step attenuators, to the input of the Log Amplifier at J621 (Figure 5-17). Set the step attenuators for 50 dB of attenuation.

e. Position the display at a graticule reference line with the Variable Output Control of the signal generator; then switch the REF LEVEL from -60 dBm to -110 dBm and adjust the front panel LOG CAL so each 10 dB step equals one division.

f. Set the REF LEVEL to -20 dBm and the step attenuators for 0 dB.

g. Increase the attenuation through the step attenuators in 10 dB steps to 50 dB and adjust the Log Gain R4020 (Figure 5-17) so each 10 dB of change produces a division of change on the display.

h. Return the step attenuator to 0 dB. Display should be full screen ($+6$ dBm); if not, readjust the signal generator output for $+6$ dBm.

i. Alternately switch the Vertical Display between 10 dB/DIV and 2 dB/DIV while adjusting Input Ref Lvl R4071 (Figure 5-17) for minimum amplitude change between the two displays.

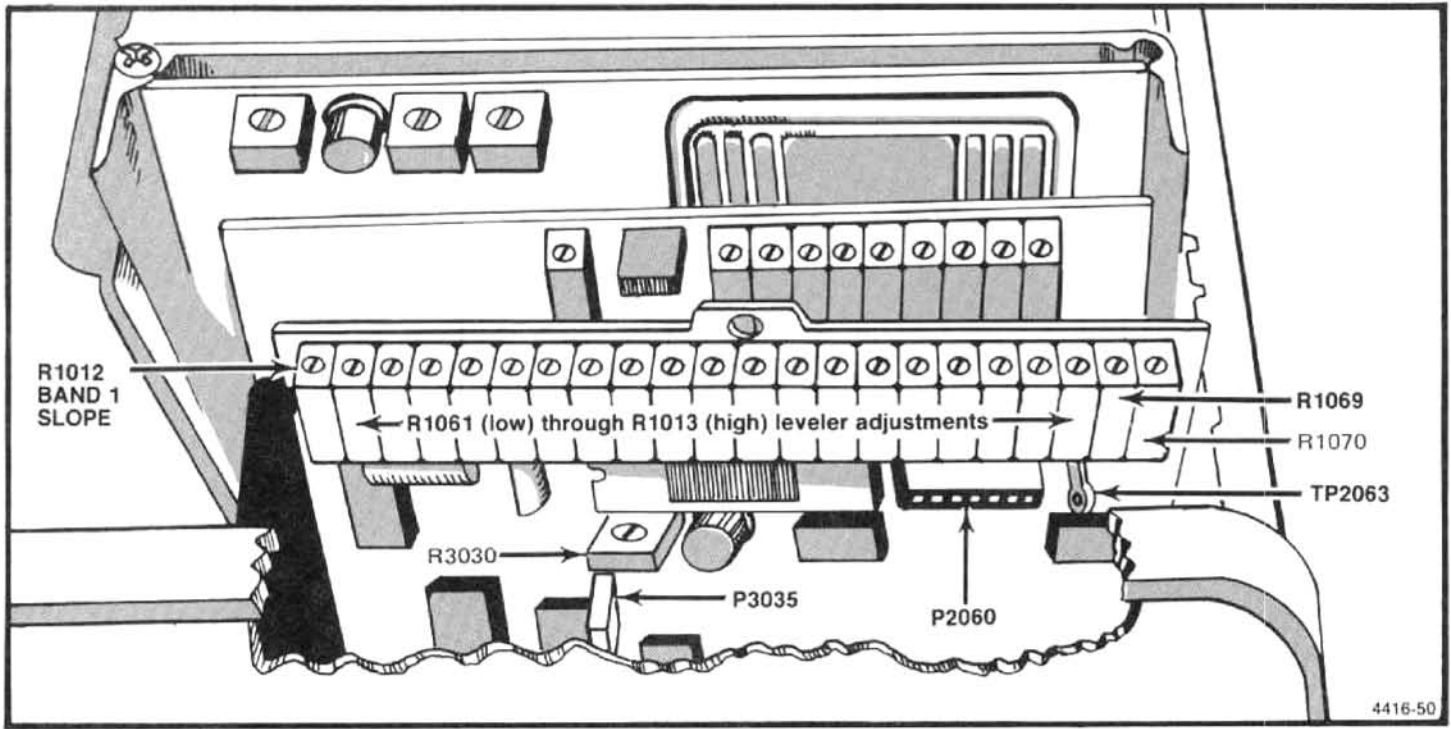


Figure 5-15. Location of P3035 on the Video Processor board.

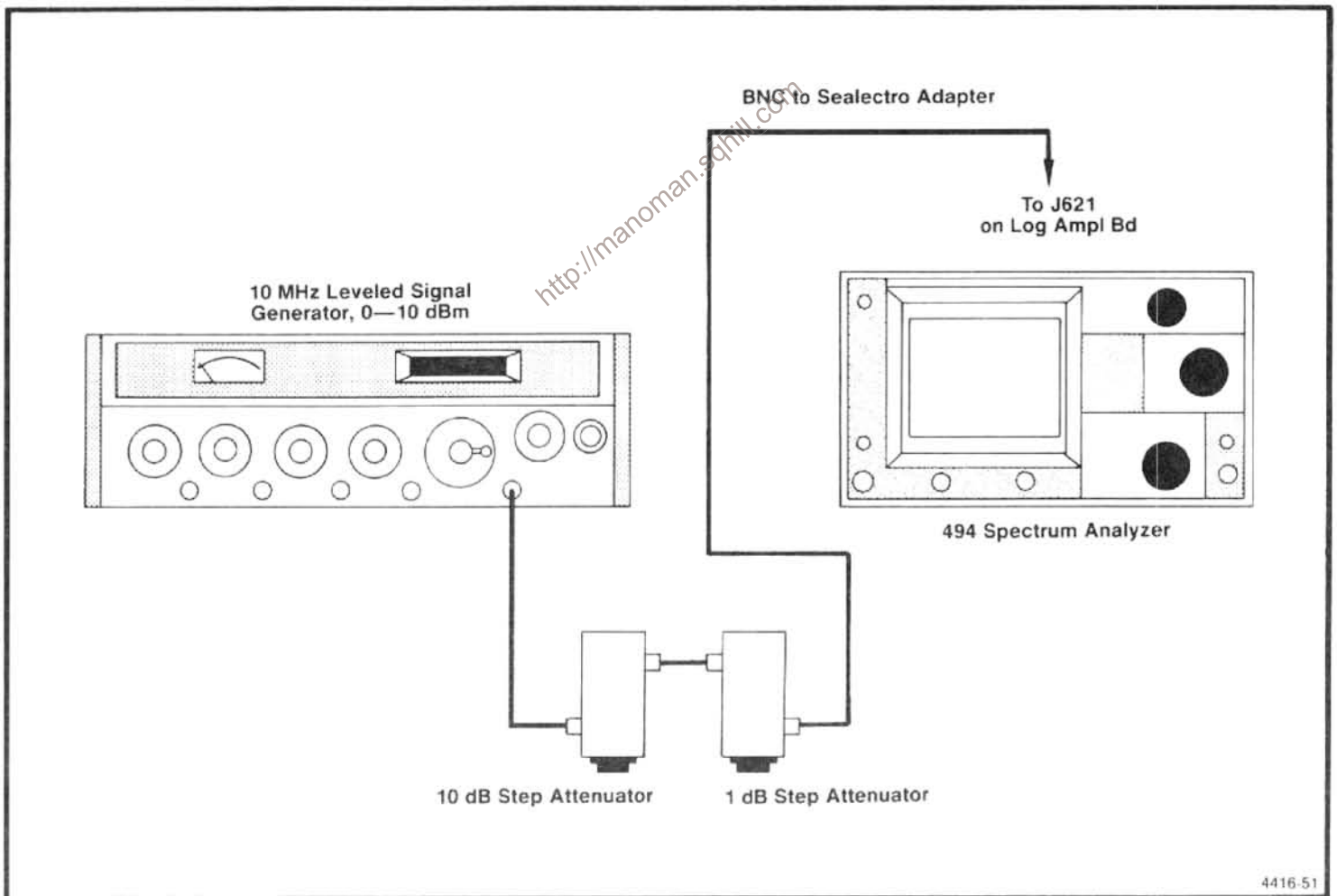


Figure 5-16. Test equipment setup for calibrating the Log Amplifier.

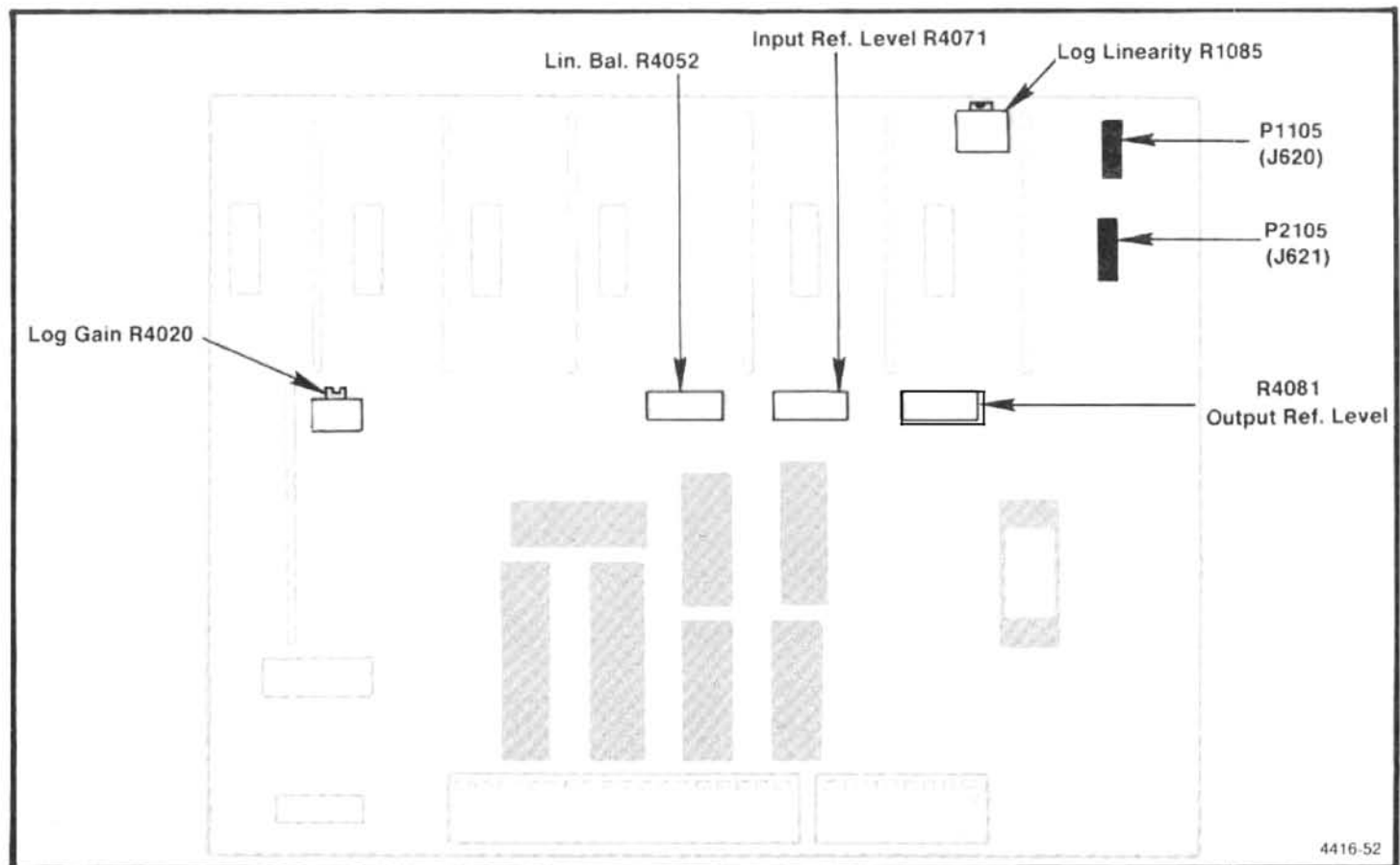


Figure 5-17. Location of test points and adjustments for calibrating the Log and Video Amplifier.

j. Activate 2 dB/DIV and add 10 dB of attenuation. If the 10 dB step (5 division) is short, adjust the gain slightly with R4020 in the same direction; then remove the 10 dB of external attenuation and adjust R1071 for a full screen display. Repeat this check until the 10 dB step is within 0.2 dB of 10 dB. Activate 10 dB/DIV and recheck 10 dB logging.

k. Activate 2 dB/DIV and momentarily remove the input signal to the Log Amplifier. Position the baseline on the bottom graticule line then reapply the signal to the Log Amplifier.

l. Adjust Output Ref Lvl R4081 (Figure 5-17) for a full screen (eight divisions) display.

m. Switch to the 10 dB/DIV mode and set the step attenuators for 40 dB of attenuation. Adjust Log Linearity R1085 (Figure 5-17) so the display is mid-screen.

n. If a large change in the setting of R1085 was required in part m, repeat the adjustments of R4071 and R4081 because of interaction.

o. Check the accuracy of 10 dB/DIV and 2 dB/DIV display modes by adding attenuation in 10 dB steps for 10 dB/DIV mode and 1 dB steps for the 2 dB/DIV mode and observe that the display steps 1 major division, ± 0.25 minor division, for each 10 dB step, and 1 division, ± 1.0 minor division, for the 2 dB mode. (Readjust the signal generator output to establish a new reference level after each step.) After the accuracy of the individual steps is verified, reset the signal level for full screen. Now add appropriate step attenuation to step the display down screen and measure the worst case error over the dynamic range. Error must not exceed ± 1.5 dB over the first 80 dB of range, or ± 1.0 dB over the 16 dB range.

p. If the 10 dB log step in the 2 dB/DIV mode is long, adjust gain with R4020 for less gain and rebalance R4071.

q. Set the step attenuators to 10 dB and activate 2 dB/DIV.

r. Set the Ref Level to -15 dBm and adjust the signal generator output for a full screen display in the 2 dB/DIV mode.

s. Press LIN and adjust Lin Bal R4052 (Figure 5-17) for a full screen display. Amplitude of LIN, 2 dB/DIV, and 10 dB/DIV display should now be the same.

t. Check LIN display linearity by adding 6 dB, 12 dB, and 18 dB of attenuation and note the display step down from full screen to, 4 ± 0.4 , 6 ± 0.4 , and 7 ± 0.4 divisions.

u. Remove the signal generator signal connection to the Log Amplifier input jack and replace P621. Switch POWER off, remove Log Amplifier board and replace the shield. Replace P3035 on the Video Processor board. Re-install the assembly and switch POWER on.

9. Calibrating the Resolution Bandwidth and Shape Factor

NOTE

The filters in each section are aligned separately, then a signal is applied through both the VR#1 and VR#2 sections. The final adjustments trim filter shape and bandwidth. Because of interaction, it is easy to offset one filter to compensate for another misadjusted filter; therefore, only adjust each filter in small increments.

The 3 dB down bandwidth of each filter section should be as wide or slightly wider than the 6 dB down point of the combined two filter sections. Gain levels are given in the Theory of Operation section and on the diagrams in Volume 2.

Before calibrating the VR Bandwidth and Gain, the correction factors must be set to zero. Refer to Log Amplifier Calibration (previous step) for the procedure.

a. Equipment setup is shown in Figure 5-18.

(1) Remove and install the VR module on an extender. Connect the output 10 MHz IF signal, from the 3rd Converter, to the input of the VR#2 section. Use a Sealectro male-to-male adapter and coaxial cable to connect between P693 and J683.

(2) Connect the output of VR#2 to the input of the Log Amplifier assembly by connecting a cable from J682 to J621 (see Figures 5-18 and 5-17).

(3) Apply the CAL OUT signal to the RF INPUT. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 50 kHz, RESOLUTION BANDWIDTH to 10 kHz, REF LEVEL to -20 dBm, and activate 2 dB/DIV.

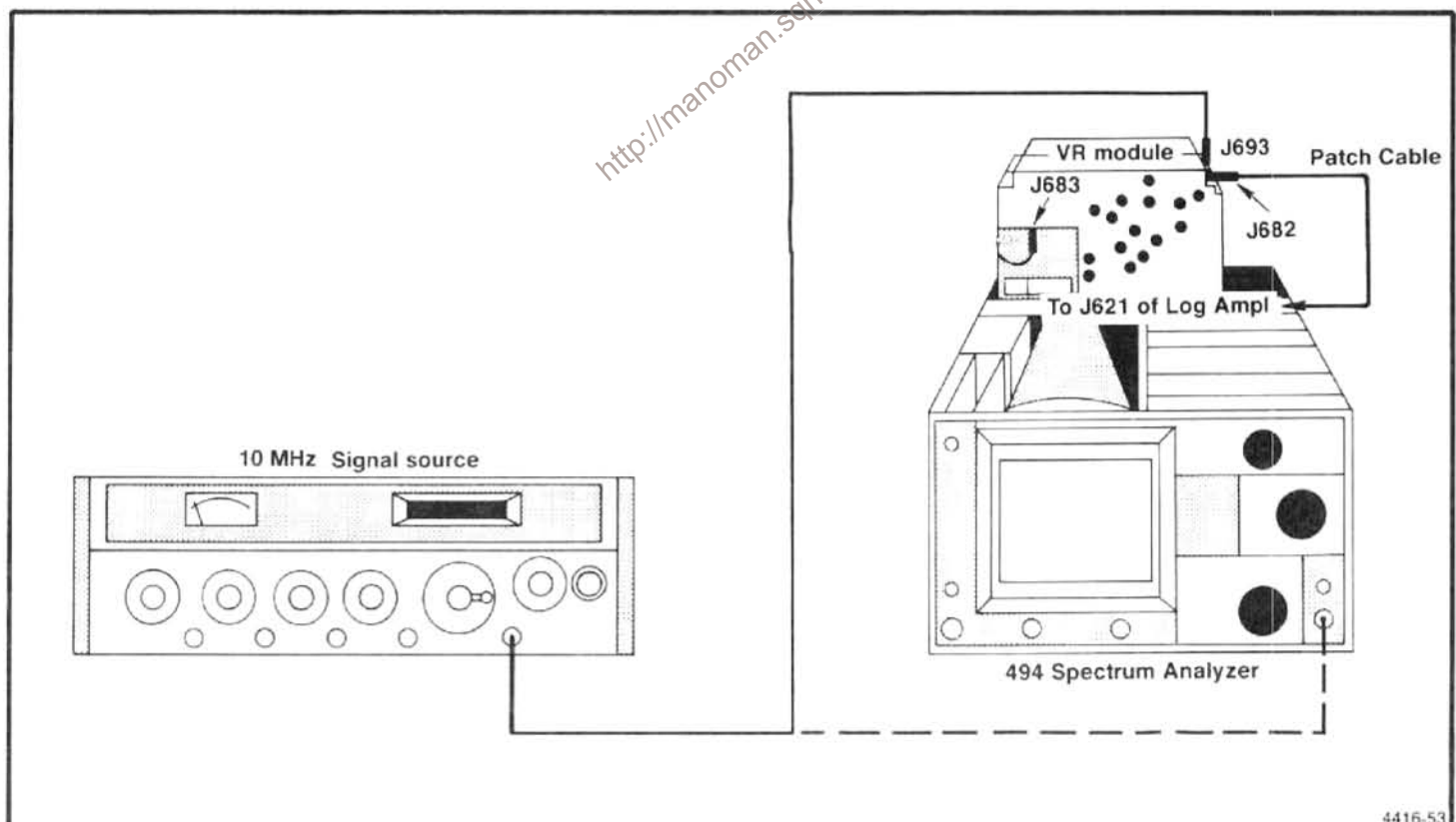


Figure 5-18. Equipment setup for calibrating the VR system.

b. Adjust the REF LEVEL for a seven division signal. Tune the display to center screen and activate SAVE A.

c. Change the RESOLUTION BANDWIDTH to 100 kHz and adjust REF LEVEL to bring the signal amplitude to about the same level as the 10 kHz response.

d. Adjust C2050 and C5055 on the 2nd Filter Select in VR#2 (Figure 5-19) for the best 100 kHz filter response (100 kHz bandwidth, 3 dB down, that is centered about the 10 kHz reference). Refer to Figure 5-20.

e. Return the RESOLUTION BANDWIDTH to 10 kHz, deactivate and reactivate SAVE A to re-establish the 10 kHz reference.

f. Switch the FREQ SPAN/DIV to 500 kHz and the RESOLUTION BANDWIDTH to 1 MHz. Adjust REF LEVEL to set the 1 MHz response amplitude to that of the 10 kHz reference, then adjust C2026 and C1022 (Figure 5-20) for the best 1 MHz response centered about the 10 kHz filter response.

g. Switch the RESOLUTION BANDWIDTH to 30 Hz and FREQ SPAN/DIV to 500 Hz. Adjust REF LEVEL so the response is near the amplitude of the reference.

h. Adjust the frequency of the temperature compensated crystal filter with R4025 (Figure 5-19) for maximum signal amplitude. Deactivate SAVE A.

i. Disconnect the 10 MHz third converter IF signal from the input to VR#2 input and reconnect it to J693 (the input of VR#1, see Figure 5-21). Connect the output of VR#1 (P683) through a Sealectro male-to-male adapter and coaxial cable to the input of the Log Amplifier at J621 (Figures 5-17 and 5-18).

j. Set the FREQ SPAN/DIV to 1 kHz, RESOLUTION BANDWIDTH to 1 kHz and adjust REF LEVEL for a 7 division display. Activate SAVE A.

k. Set the FREQ SPAN/DIV to 10 kHz, RESOLUTION BANDWIDTH to 10 kHz and adjust REF LEVEL for a 7 division display.

l. Adjust the 10 kHz filter with C2037 (Figure 5-21) for best filter response shape around the 1 kHz reference.

m. Deactivate SAVE A and then reactivate to save the 10 kHz display.

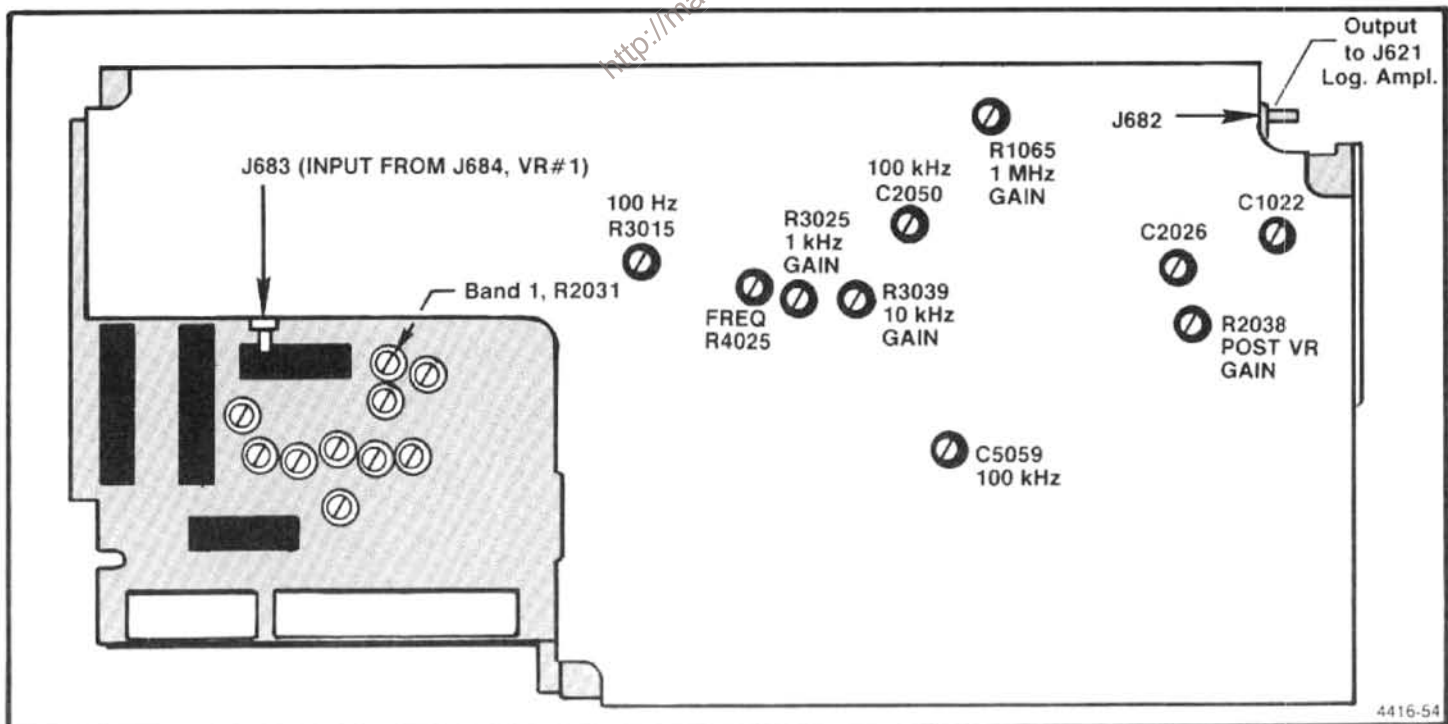


Figure 5-19. Adjustments on the VR#2 module.

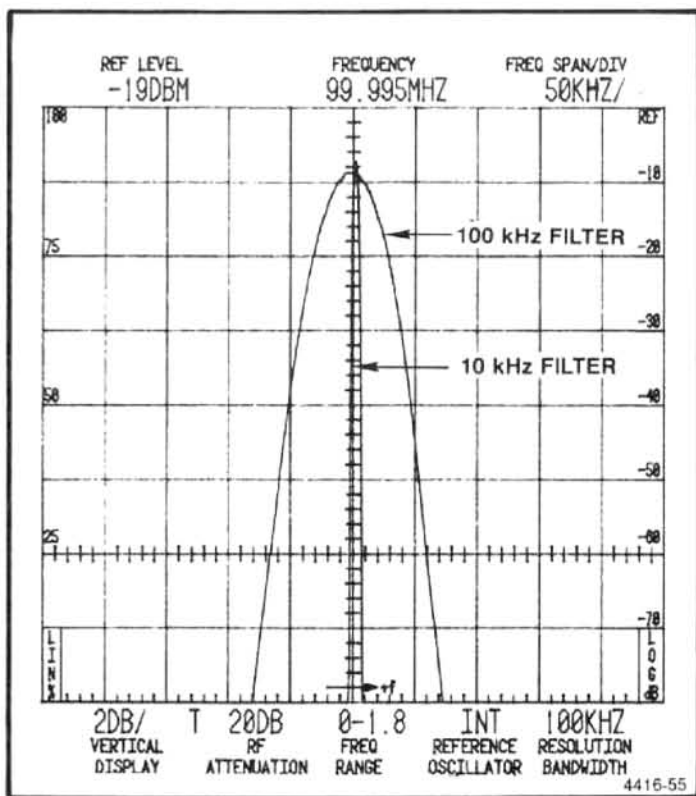


Figure 5-20. Response of the 100 kHz filter over the response of the 10 kHz filter.

n. Now, set the FREQ SPAN/DIV to 50 kHz, RESOLUTION BANDWIDTH to 100 kHz, and adjust the 100 kHz filter with C3023 and C3035 (Figure 5-21) for filter shape and centering about the 10 kHz filter reference.

o. Set the RESOLUTION BANDWIDTH to 1 MHz, FREQ SPAN/DIV to 500 kHz, and adjust the 1 MHz filter response and centering with C1033 and C1026 in the VR Input board (Figure 5-21). Deactivate SAVE A.

p. Set the RESOLUTION BANDWIDTH to 30 Hz and the FREQ SPAN/DIV to 50 Hz. Readjust R4025 for maximum response.

q. Disconnect the cable between P683 and the Log Amplifier input (J621). Reconnect P683 to J683 and connect the output from the VR#2 to the Log Amplifier input (J621). The signal should now pass through both VR#1 and VR#2 to the input of the Log Amplifier.

r. Check the waveshape, bandwidth, and centering of all filters. If necessary, make only fine or minor adjustments. Figure 5-22 shows typical response shapes.

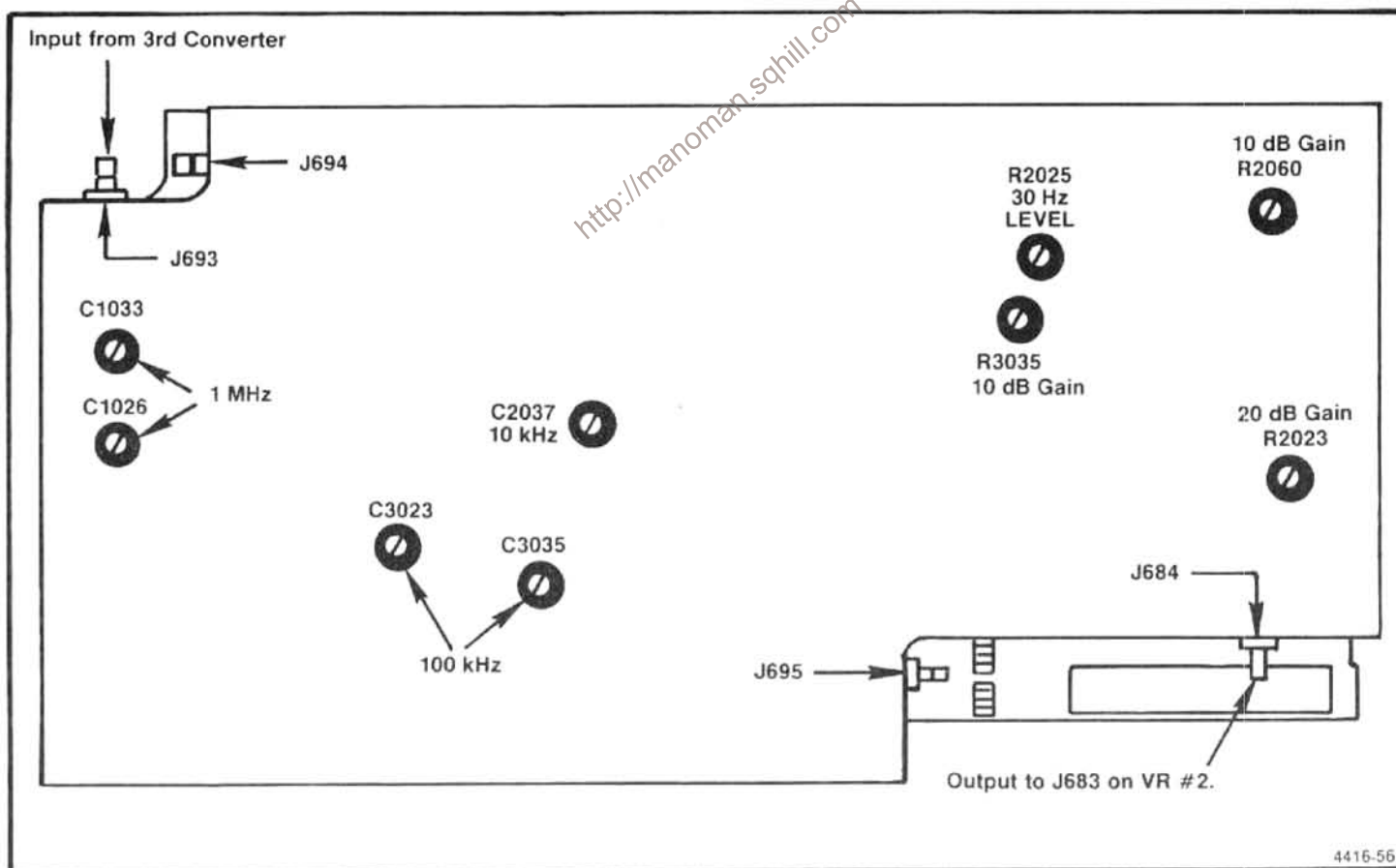


Figure 5-21. Adjustments on the VR#1 module.

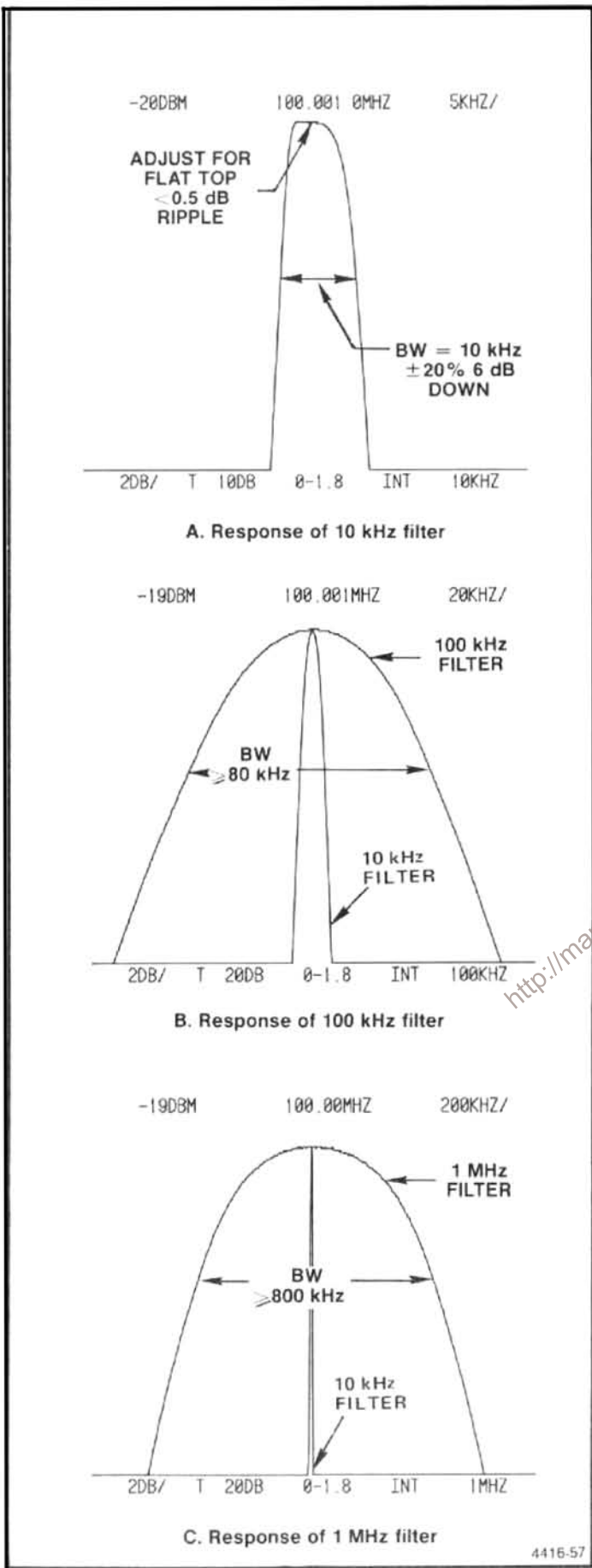


Figure 5-22. Typical response of the 10 kHz, 100 kHz, and 1 MHz bandwidth filters.

s. Level the gain of the filters as follows:

(1) Set the FREQ SPAN/DIV to 500 kHz, RESOLUTION BANDWIDTH to 100 kHz, and REF LEVEL to -20 dBm.

(2) Adjust all filters to the 100 kHz level as follows: (Change FREQ SPAN/DIV as necessary to maintain a suitable display)

Filter	Adjust	Location
1 MHz	R1065	VR#2
10 kHz	R3035	VR#2
1 kHz	R3025	VR#2
100 Hz	R3015	VR#2
30 Hz	R2025	VR#1

Locations of the adjustments are shown in Figure 5-20 and 5-21. If any change is made in the 100 Hz response the 30 Hz Gain should be readjusted.

10. Presetting the Variable Resolution Gain and Band Leveling

NOTE

The Log Amplifier must be calibrated before adjusting any VR gain settings. Log Amplifier calibration can be verified by applying a +6 dBm, 10 MHz signal to the input (J621), of the Log Amplifier, and checking for full screen display with the REF LEVEL at -20 dBm.

a. Before adjusting the VR gain and band leveling, set the correction factors to zero. Refer to Log Amplifier Calibration (step 8) for the procedure.

b. Test equipment setup is shown in Figure 5-18. Set the FREQ SPAN/DIV to 1 MHz, RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL at -20 dBm, and activate 2 dB/DIV.

c. The gain of the Post VR Amplifier should be 20 dB for best signal-to-noise ratio through the VR stages. If any maintenance has been performed on this stage, perform the following steps.

(1) Remove the cover for the VR#2 module. Disconnect the jumper connector to the input of the Post VR Amplifier (pin JJ).

(2) Apply a 10 MHz, -14 dBm signal, from a 50 Ω signal source, to pin JJ of the amplifier.

(3) Adjust Gain R2038 for a full screen display.

(4) Remove the signal from the input to the Post VR Amplifier and replace the jumper connector to pins JJ at the input to the Post VR Amplifier. Replace the cover for the VR#2 module.

d. Adjust the front panel AMPL CAL to its fully counterclockwise position and set the Band 1 Gain R2031 on VR#2 (Figure 5-19) fully counterclockwise.

e. Disconnect P693 from the input to VR#1 module (Figure 5-21) and activate MIN NOISE. Apply a 10 MHz, -25 dBm signal, from the signal generator, through a bnc-to-Seaelectro adapter to J693. Adjust the generator frequency to peak the signal amplitude. (Signal amplitude should be between 3.5 and 6.5 divisions. If signal amplitude is not within these limits it indicates a gain problem in the VR.)

f. If the signal amplitude is over 5 divisions, adjust Post VR Gain R2038 on VR#2, (Figure 5-19) for a 5 division signal amplitude. If the signal amplitude is less than 5 divisions proceed to part "g" of this step.

g. Adjust the front panel AMPL CAL for a 7 division signal.

h. Switch MIN NOISE off, decrease the generator output to -35 dBm, leave the REF LEVEL at -20 dBm, and adjust the 10 dB Gain, R3035, on the 10 dB Gain board of VR#1 (Figure 5-21) so the signal amplitude is 7 divisions.

i. Change the generator output to -45 dBm, the REF LEVEL to -40 dBm, and adjust 20 dB Gain R2023 on the 20 dB Gain Step board (Figure 5-21) for a 7 division signal amplitude.

j. Change the generator output to -65 dBm, the REF LEVEL to -60 dBm, and adjust the 10 dB Gain, R2060, on the 20 dB Gain Step board (Figure 5-21) for a 7 division signal amplitude.

k. Set the REF LEVEL to -30 dBm and the generator output to -35 dBm. Check for a 7 division signal amplitude. Repeat this check for -45 , -55 , and -65 dBm input levels. Note that each maintains the 7 division signal to verify that the gain of the VR gain stages are correct. Readjust gain if necessary.

l. Remove the 10 MHz signal to J680 and reconnect P680. The final band level adjustments are described after

calibrating the Preselector Tracking and checking flatness. The mean level for each band is set to the level of band 1.

m. Press <SHIFT> CAL to rerun a calibration routine and re-establish processor correction factors.

11. Calibrator Output Level

The calibrator output level is calibrated to a known reference. The procedure for checking the level is described in the Performance Check section. Output level is adjusted with Cal Level R1041, in the 3rd converter (#2 in Figure 5-23).

12. IF Gain Calibration

a. Test equipment setup is shown in Figure 5-23. Set the RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to -20 dBm, and apply a -21.5 dBm, 110 MHz signal, through step attenuators, to the input (J365) of the 110 MHz filter.

b. Set the step attenuators for 0 dB. (With -21.5 dBm input, the signal level should be 7 divisions or more.) Adjust the generator output for a 7 division signal reference level.

c. Remove the 110 MHz signal to the 110 MHz filter and reconnect P365.

d. Set the step attenuators for 21 dB attenuation and apply the 110 MHz signal to the input (J321) of the 110 MHz IF amplifier (Figure 5-23).

e. Adjust the gain of the IF Amplifier, with R1015, for a display amplitude that equals the seven division reference set in part b.

f. Remove the 110 MHz signal and reconnect P321. Apply the CAL OUT signal to the RF INPUT. Set the REF LEVEL to -20 dBm, FREQUENCY to 100 MHz, FREQ SPAN/DIV to 100 kHz, and RESOLUTION BANDWIDTH of 100 kHz.

g. Set the front panel AMPL CAL fully counterclockwise and adjust 110 MHz IF Gain R1015 for 5 division of signal. (If this cannot be achieved, it indicates excessive loss through the front end.)

h. Adjust the AMPL CAL for a full screen signal. AMPL CAL adjustment should now have 6 dB down range and 6 dB or more up range.

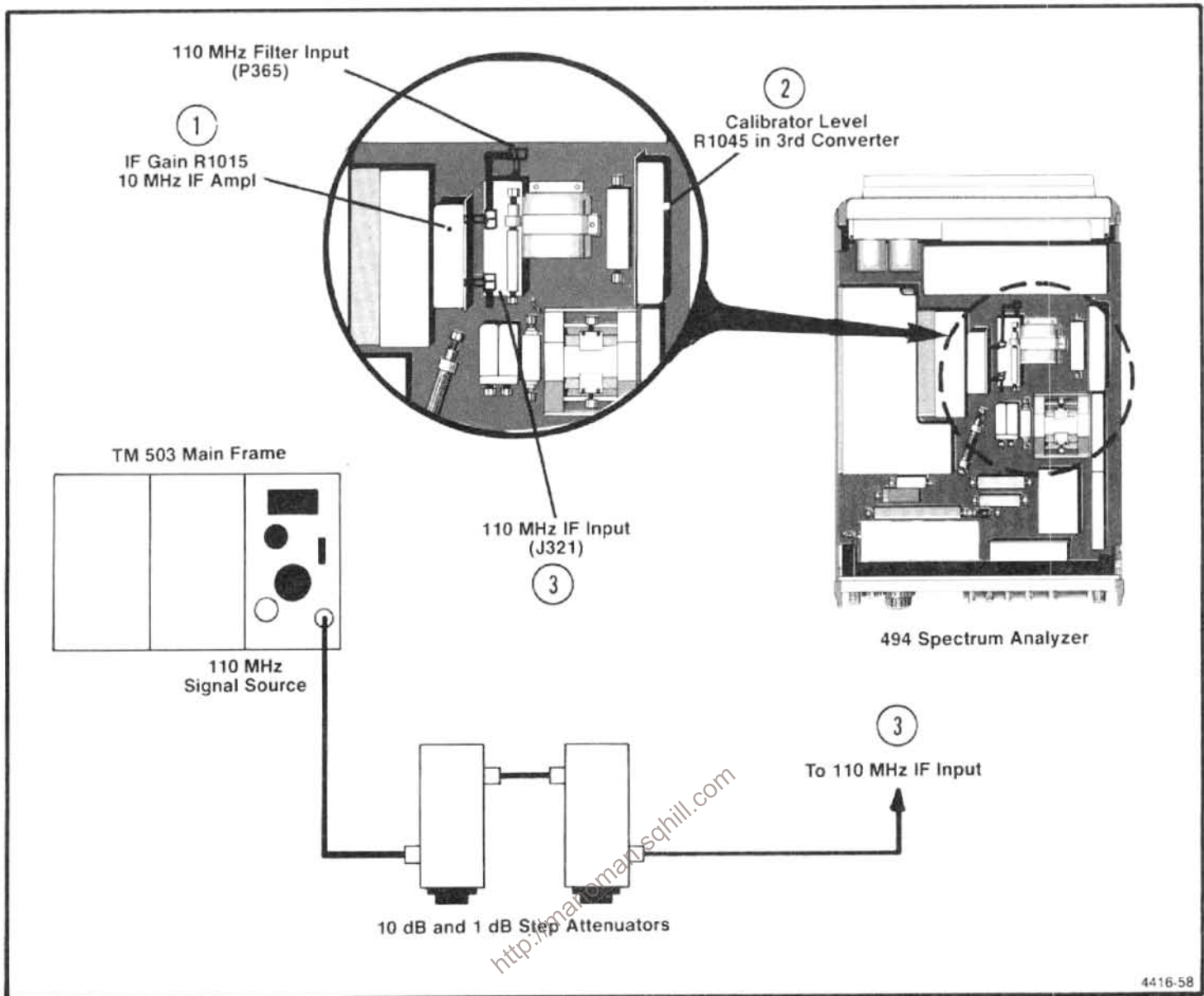


Figure 5-23. Test equipment setup for adjusting the IF gain and the location of adjustments and connectors.

NOTE

Two variable capacitors, C325 and C2047 on the 110 MHz IF board, do not require adjustment during calibration. This adjustment requires return loss measurement which is a maintenance and repair function.

13. Digital Storage Calibration

NOTE

This is a two-part procedure; the first calibrates the 494, the second is a program to be used with TEKTRONIX 4050-Series Computer terminal and a 494P instrument.

PART 1, 494 PROCEDURE

- a. Set the FREQUENCY to 200 MHz, FREQ SPAN/DIV to 20 MHz, REF LEVEL to -20 dBm, and activate AUTO RESOLN, 10 dB/DIV, and VIEW A.
- b. Apply the CAL OUT signal to the RF INPUT and adjust the PEAK/AVERAGE cursor so it is about one division above the bottom of the screen.
- c. On the Horizontal Digital Storage board:
 - (1) adjust Output Offset, R1039 (Figure 5-24) so the left edge of the cursor is at the left edge of the crt (about 0.25 division over-span from the left graticule line);

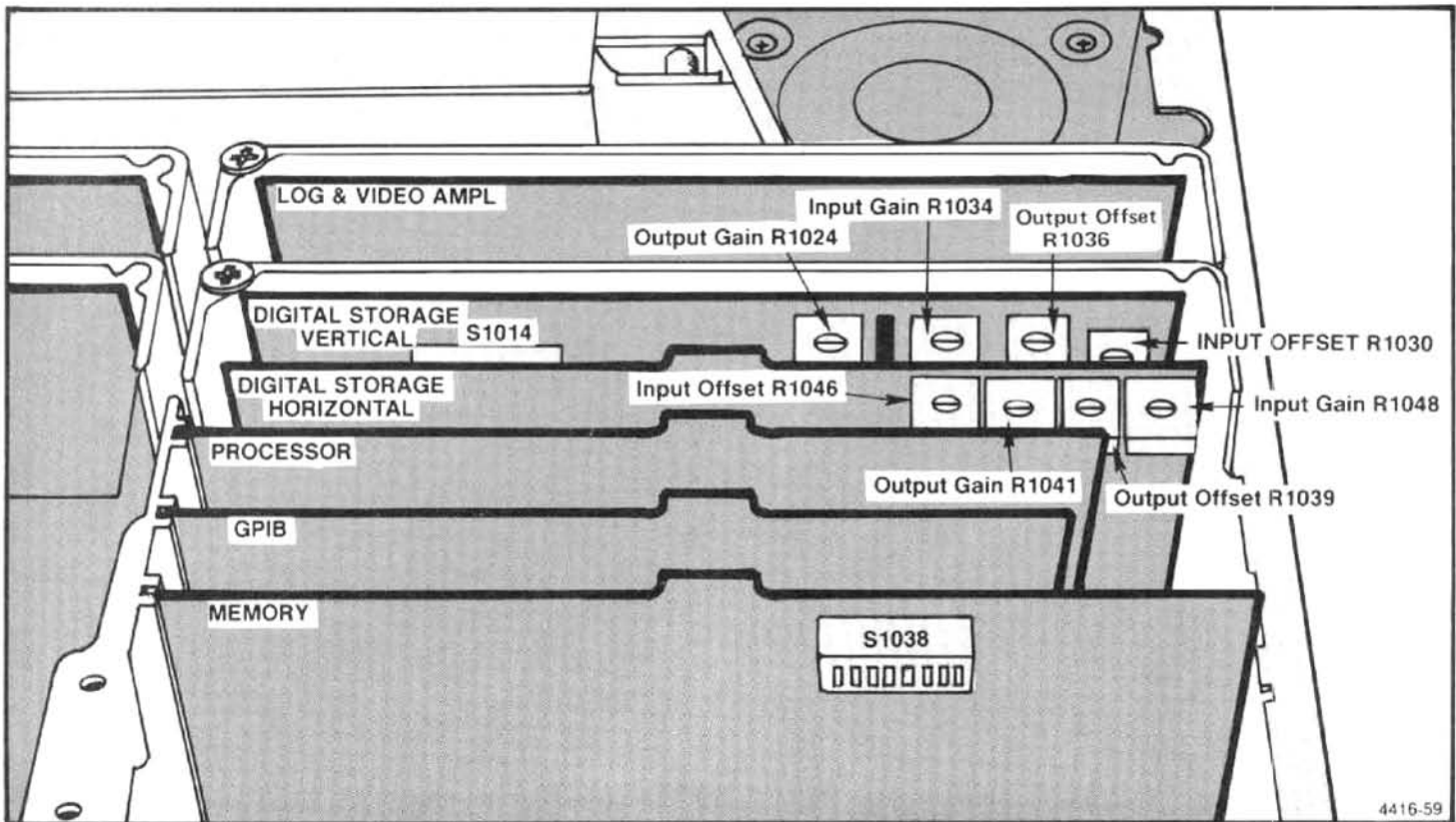


Figure 5-24. Digital storage calibration adjustments.

(2) adjust Output Gain, R1041 (Figure 5-24) so the right edge of the cursor is at the right edge of the crt;

(3) alternately switch VIEW A on and off while adjusting Input Gain, R1048 (Figure 5-24) so the storage signal at the right edge tracks with the non-store signal.

(4) alternately switch VIEW A on and off while adjusting Input Offset R1046, so the stored display at the left edge tracks with the non-store display.

(4) change the REF LEVEL to raise the amplitude of the signal to full screen;

(5) adjust Input Gain R1034, so the stored display, of the high amplitude signal, is the same as the non-store display;

(6) repeat the low level and high level adjustments to compensate for interaction.

d. On the Vertical Digital Storage board:

(1) Output Gain R1024 and Output Offset R1036 (Figure 5-24) are adjusted at the factory. In the 494P only, an alternate procedure follows. These adjustments should not be changed; however, if they are disturbed, center the adjustments and Input Gain R1034 before proceeding;

(2) activate 2 dB/DIV display mode and turn PEAK/AVERAGE control clockwise;

(3) using a signal near the bottom of the display, adjust Vertical Offset R1030 (Figure 5-24) so the stored display is the same amplitude as the non-store signal;

PART 2, 494P PROCEDURE

a. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 10 MHz, RESOLUTION BANDWIDTH to 1 MHz, REF LEVEL to -10 dBm, PEAK/AVERAGE control fully counter-clockwise, and activate 2 dB/DIV, VIEW A and VIEW B, and NARROW Video Filter.

b. Connect CAL OUT to the RF INPUT and interconnect the 494P with the 4050-Series Controller, via a GPIB cable (both should already be turned on). Set the 494P GPIB ADDRESS switches on the rear panel for address 1 (switch 1 up, all others down).

c. Enter and run the following program:

```

100 DIM C (1000 )
110 K=125
120 I1=0
130 FOR I=1 TO 10
140 FOR J=1 TO 100
150 C (I1+J )=K
160 NEXT J
170 K=K-25
180 I1=I1+100
190 IF K >=25 THEN 210
200 K=225
210 NEXT I
220 PRINT @1 : "SIGSWP"
230 WBYTE @33:64,C,-255
    
```

d. Adjust the POSITION controls to center the frequency dot and place the baseline on the bottom graticule line.

e. Adjust the following to match the step waveform to the graticule: (Figure 5-24)

Assembly	Adjustment
Horizontal Digital Storage	Output Offset, R1039
Horizontal Digital Storage	Output Gain, R1041
Vertical Digital Storage	Output Offset, R1036
Vertical Digital Storage	Output Gain, R1024

Be sure that the left and right edges of the step waveform coincide with the left and right edges of the graticule. This matches the horizontal display width of a 1000-point waveform to the graticule.

f. Press REMOTE TO LOCAL and activate FREE RUN Triggering. Reduce the FREQ SPAN/DIV to 200 kHz.

g. Adjust REF LEVEL so the signal peak is about one division above the bottom of the graticule.

h. Deactivate VIEW A. Press VIEW B repeatedly, and adjust Vertical Offset R1030, on the Vertical Digital Storage board, to minimize the amplitude difference between the stored and non-store waveforms.

i. Adjust the REF LEVEL to bring the signal peak close to the top of the graticule.

j. Again, while pressing VIEW B repeatedly, adjust Input Gain R1034 on the Vertical Digital Storage board (Figure 5-24) to minimize the amplitude difference between the stored and non-store waveforms.

k. Because the offset and gain adjustments interact, repeat parts h through k as necessary.

l. Deactivate NARROW Video Filter, increase FREQ SPAN/DIV to 10 MHz and tune the signal to within one division of the right edge of the graticule.

m. Press VIEW B repeatedly and adjust Input Gain R1048 on the Horizontal Digital Storage board (Figure 5-24) so the horizontal position of the stored signal matches that of the non-stored signal.

n. Tune the signal to within 1 division to the left edge of the graticule. Alternately switch VIEW B on and off while adjusting the Input Offset R1046 so the horizontal position of the stored display is the same as the non-store display.

14. Setting B—SAVE A Reference Level

When B—SAVE A is selected, the expression implemented is $(B - \text{SAVE A}) + k$, where k is a constant set by the input data for an 8-to-4 line encoder, U1015. Each bit will move the reference level about 0.2 minor division. Normally, the reference level is set at the center graticule line; however, it can be set anywhere within the graticule area by the setting of an 8-bit binary switch, S1014 (Figure 5-24). The MSB (switch #8) shifts the display about five divisions, switch #7 half this amount, etc. The following procedure sets the reference level.

Estimate the amount and direction the reference level is to be shifted, then close or open the switches on S1014 to obtain the desired B—SAVE A reference level.

15. Preselector Driver Calibration

a. Test equipment setup is shown in Figure 5-25.

b. Set the offset for driver U2054 as follows: (Offset should only require adjusting if U2054 is changed.) Switch POWER off, pull the Preselector Driver board and install on extender board (Figure 5-26) then switch POWER on.

(1) Set the FREQUENCY RANGE to band 1 (0-1.8 GHz);

(2) Pull P3055 and connect a DVM between TP4054 and analog ground (Figure 5-26). Set the voltmeter range to 30 Ω V or less;

(3) Starting from a fully counterclockwise position, adjust Driver Offset R2066 (Figure 5-26) for 0 V at TP4054;

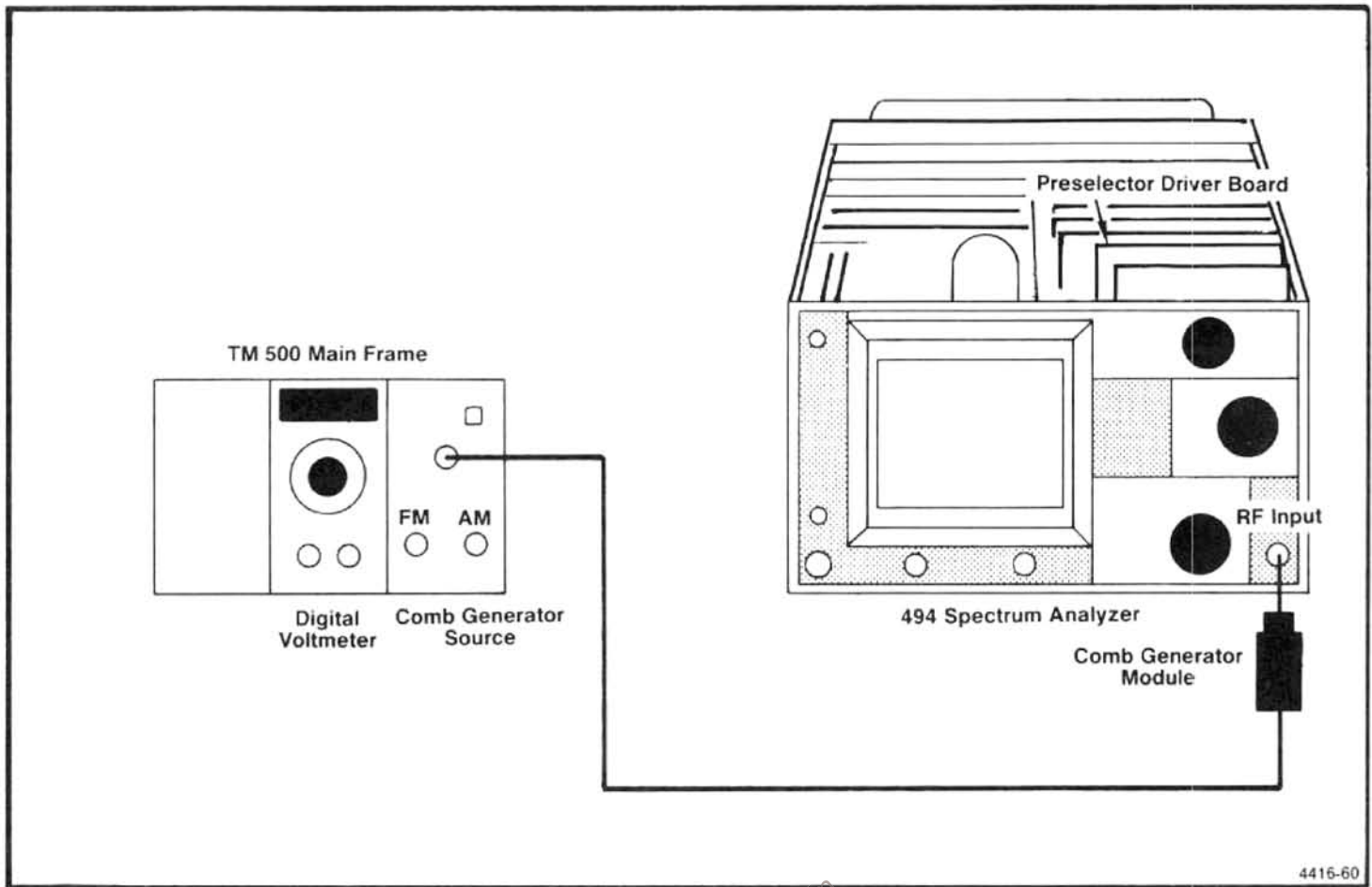


Figure 5-25. Test equipment setup for Preselector Driver adjustments.

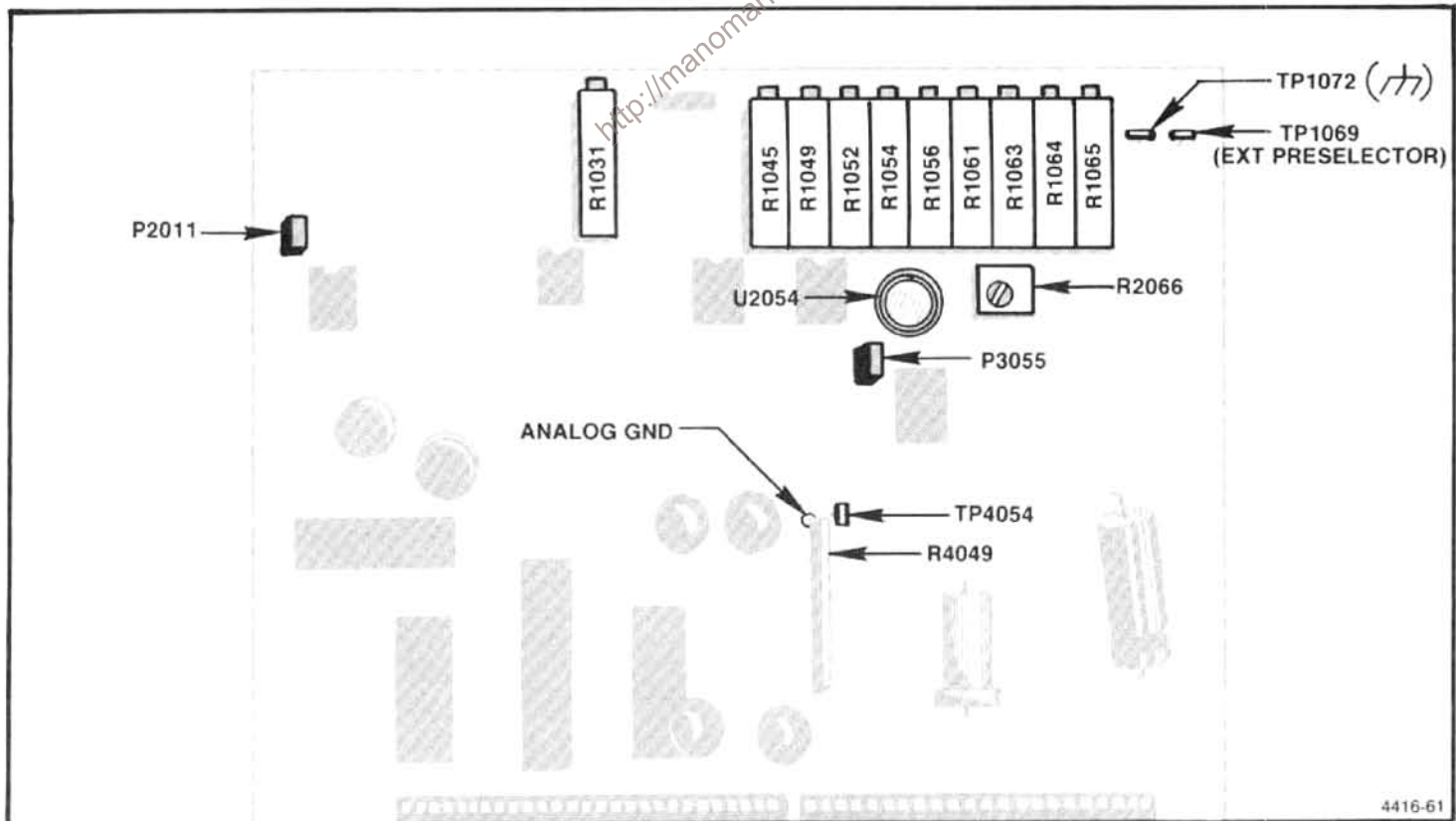


Figure 5-26. Preselector Driver adjustment and test points.

Adjustment Procedure—494/494P Service Vol. 1

- (4) Disconnect the DVM, replace P3055, then switch POWER off and reinstall the Preselector Driver board. Switch POWER on.
- c. Connect DVM between the center tap of the MANUAL PEAK potentiometer and ground. Adjust the control for 0 V indication. If index on the knob is not aligned with the mark on the front panel, loosen knob and position the mark so it is aligned.
- d. Apply the CAL OUT signal to the RF INPUT. Set the REF LEVEL to -30 dBm, FREQ SPAN/DIV to 20 MHz and activate AUTO RESOLN. Select the 1.7-5.5 GHz FREQUENCY RANGE and adjust the CENTER FREQUENCY to center the 2.1 GHz marker. Center the Input Offset adjustment R1031 (Figure 5-26) then center the 2.1 GHz marker with the CENTER FREQUENCY control.
- e. Ground TP1069 with a jumper strap and adjust the Preselector Offset R1064 for maximum response of the 2.1 GHz signal. Remove the grounding strap.
- f. Peak the 2.1 GHz signal with the -829 MHz IF Offset R1049 (Figure 5-26)
- g. Remove the Calibrator signal to the RF INPUT and connect the output of the Microwave Comb Generator to the RF INPUT. Change the REF LEVEL to 0 dBm, set FREQUENCY to 5.5 GHz, and center the 5.5 GHz comb marker on screen.
- h. Peak the 5.5 GHz signal with the Preselector Sense, R1065, adjustment.
- i. Repeat parts f through h to ensure that the 2.1 and 5.5 Hz frequency points track the input tuning.
- j. Change the FREQUENCY RANGE to 5.4-18.0 GHz (band 4). Adjust REF LEVEL and RESOLUTION BANDWIDTH to observe the 6 GHz marker. Adjust MANUAL PEAK to peak the 6 GHz signal.
- k. Set FREQUENCY to 9 GHz and observe the 9 GHz marker on screen. Peak this response with the X3 Gain R1052 adjustment.
- l. Repeat parts j and k to ensure tracking over this range.
- m. Increase FREQUENCY to the 12 GHz marker, then peak the 12 GHz point with Shaper #1 R1054 adjustment (Figure 5-26).
- n. Adjust FREQUENCY to center the 17 GHz marker, then peak the signal with Shaper #2, R1056 adjustment.
- o. Recheck the 6, 9, 12, and 17 GHz points to verify that they all peak at the same position of the front-panel MANUAL PEAKING control. If they do not, repeat parts g through n.
- p. Change the FREQUENCY RANGE to 1.7-5.5 GHz (band 2). Center a comb marker between 5.4 and 5.5 GHz, then peak the signal with the front-panel MANUAL PEAK control.
- q. Change FREQUENCY RANGE to the 5.4-18.0 GHz (band 4). Center the same signal used in part p with the CENTER FREQUENCY control. Adjust Input Offset R1031, to peak the signal.
- r. Repeat parts p through q until the signal amplitude peaks, on both bands, occur at the same position of the MANUAL PEAK control.
- s. Set MANUAL PEAK control so the index mark aligns with the front panel mark. Change FREQUENCY RANGE to 1.7-5.5 GHz, and adjust CENTER FREQUENCY to center the 3.5 GHz comb marker.
- t. Adjust -829 MHz IF Offset R1049 (Figure 5-26) to peak the 3.5 GHz response.
- u. Change FREQUENCY RANGE to 3.0-7.1 GHz, set the FREQUENCY to 5.0 GHz to observe the marker, then peak the 5.0 GHz signal with $+829$ MHz IF Offset R1045 adjustment.
- v. Change FREQUENCY RANGE to 15-21 GHz. Set the FREQUENCY to 15 GHz, then peak the 15 GHz signal with R1064.
- w. Tune the 19 GHz marker to center screen then peak the 19 GHz signal with Shaper #3 R1061 adjustment (Figure 5-26).
- x. Tune to the 21 GHz marker then peak the signal with Shaper #4, R1063, adjustment.

y. Recheck the 15, 19, and 21 GHz points to verify that they all peak at the same position of the MANUAL PEAK control.

z. Change FREQUENCY RANGE to 3.0-7.1 GHz, center a 5.0 GHz signal on screen, then peak the signal with +829 MHz IF, R1045, adjustment.

aa. Change to the 1.7-5.5 GHz band, center a 3.5 GHz marker on screen, then peak the 3.5 GHz signal with -829 MHz IF, R1049, adjustment.

ab. All bands should now track or the signal peak for all bands should occur with the MANUAL PEAK knob index marker near the front-panel mark.

16. Baseline Leveling (Video Processor)

This procedure sets response slope for band 1 and adjusts the baseline so response perturbations for band 4 are offset to level the display.

a. Test equipment setup is shown in Figure 5-27. The output of the sweep generator is applied through a 3 dB attenuator and high performance coaxial cable to a power divider. Connect one output of the power divider directly to the RF INPUT of the 494/494P and the other to the sensor for the power meter. Set the RF plug-in ALC switch to MTR position and connect a coaxial cable between Recorder Output of the power meter and the Ext ALC Input of the plug-in unit on the sweeper. Set the Power Level to approximately -10 dBm then adjust the Gain on the unit for stable operation (output stops oscillating).

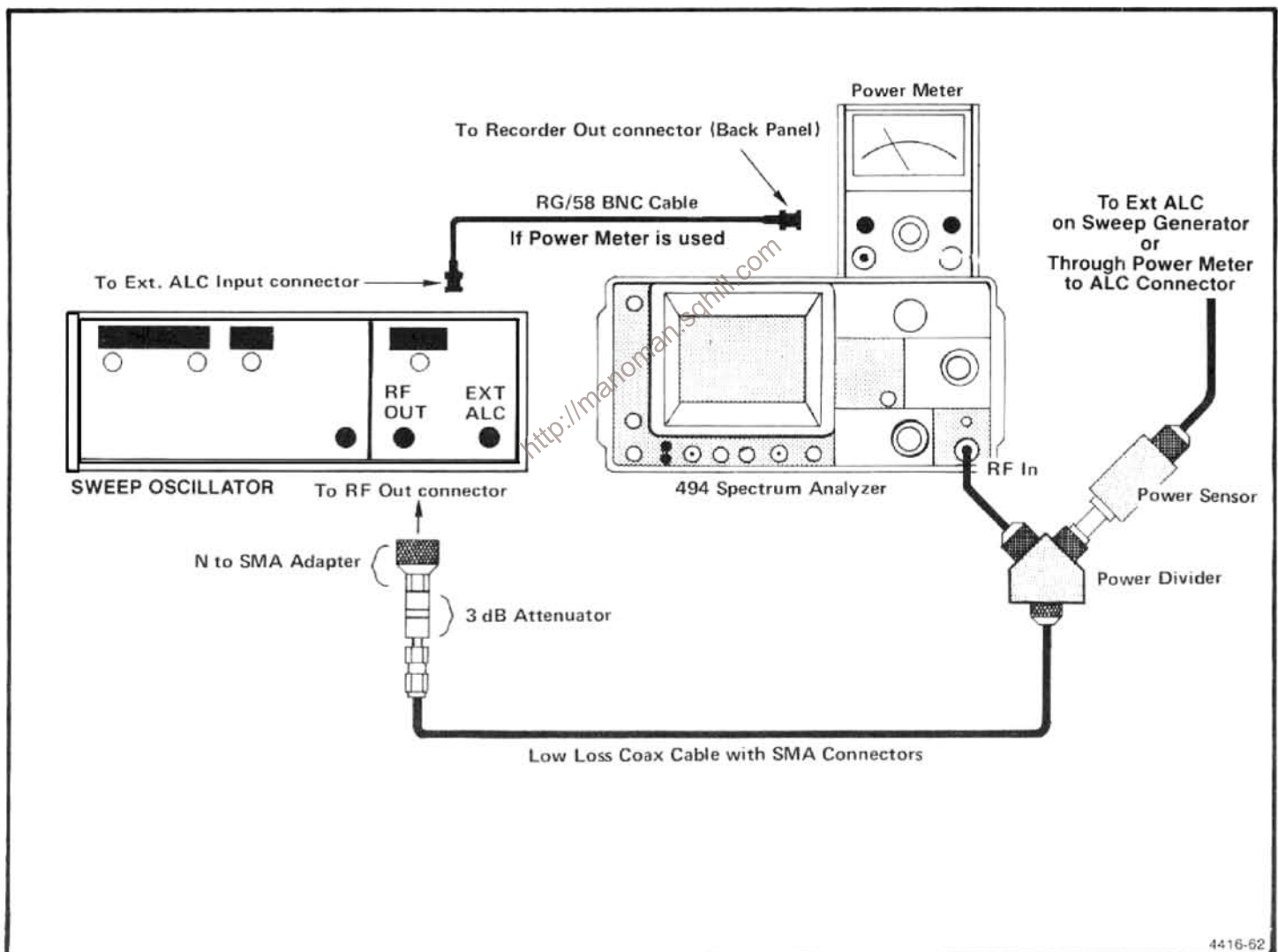


Figure 5-27. Test equipment setup for adjusting baseline leveling.

b. Set the FREQUENCY to 0.00 GHz. FREQ SPAN/DIV to MAX, REF LEVEL to -20 dBm, TIME/DIV to AUTO, and activate AUTO RESOLN and 2 dB/DIV. Set PEAK/AVERAGE control fully counterclockwise.

c. Apply the output of the sweep oscillator to the RF INPUT, as shown in Figure 5-27. Set the sweep oscillator to the Automatic Internal Sweep (Marker Sweep), sweep time to 100 s, and set it so the oscillator sweeps from 10 MHz to 1.8 GHz.

d. Activate MAX HOLD, VIEW A, and VIEW B and select a TIME/DIV so there are no breaks in the digitized stored display (Figure 5-28A).

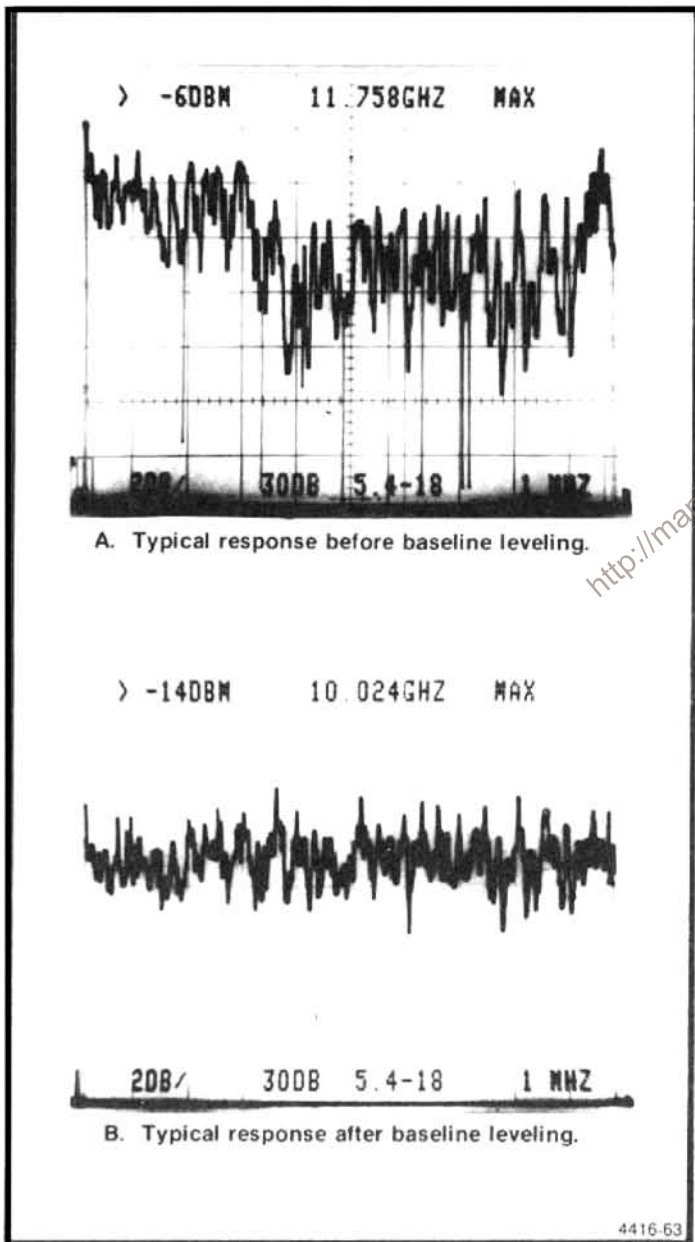


Figure 5-28. Typical response when adjusting baseline leveling.

e. Reactivate MAX HOLD and SAVE A. Trace and record the response of band 1. Note the number of divisions from the baseline to the lowest point in the first 5 divisions of the display.

f. Adjust the CENTER FREQUENCY to place the dot marker directly over the lowest point within the last 3 divisions of the display.

g. Set the sweep oscillator CW Marker control On and adjust it so a signal is at center screen on the 494/494P.

h. Adjust band 1 Slope R1012, on the Video Processor board (Figure 5-29), to set the top of the signal to the same amplitude level noted above, in part e.

i. Repeat until the frequency response is within 1.5 dB of the mid-point between the two extremes.

j. On the Video Processor board pull the Leveler Disable plug P3035 (Figure 5-29).

k. Set the FREQUENCY to 10 GHz, FREQUENCY RANGE to 5.4-18.0 GHz (band 4) FREQ SPAN/DIV to MAX, REF LEVEL to -10 dBm, and TIME/DIV to 10 ms. Activate 10 dB/DIV, and AUTO RESOLN. (UNCAL indicator will light.)

l. On the sweep oscillator select a 5.5 GHz cw marker and adjust the output for -10 dBm reading on the power meter.

m. Activate 2 dB/DIV and adjust the REF LEVEL so the signal amplitude is half screen. Adjust MANUAL PEAK for maximum response or activate AUTO PEAK.

n. On the sweep oscillator change to the automatic internal sweep (Marker Sweep) and set the sweep time for 100 s/sweep (its slowest sweep).

o. Activate VIEW A and VIEW B then select a sweep time, on the 494/494P so the stored display is solid (no breaks in the digitized display, (Figure 5-28).

p. Activate MAX HOLD and SAVE A. Trace and record the response of band 4.

q. Deactivate VIEW A and MAX HOLD (SAVE A and VIEW B still active).

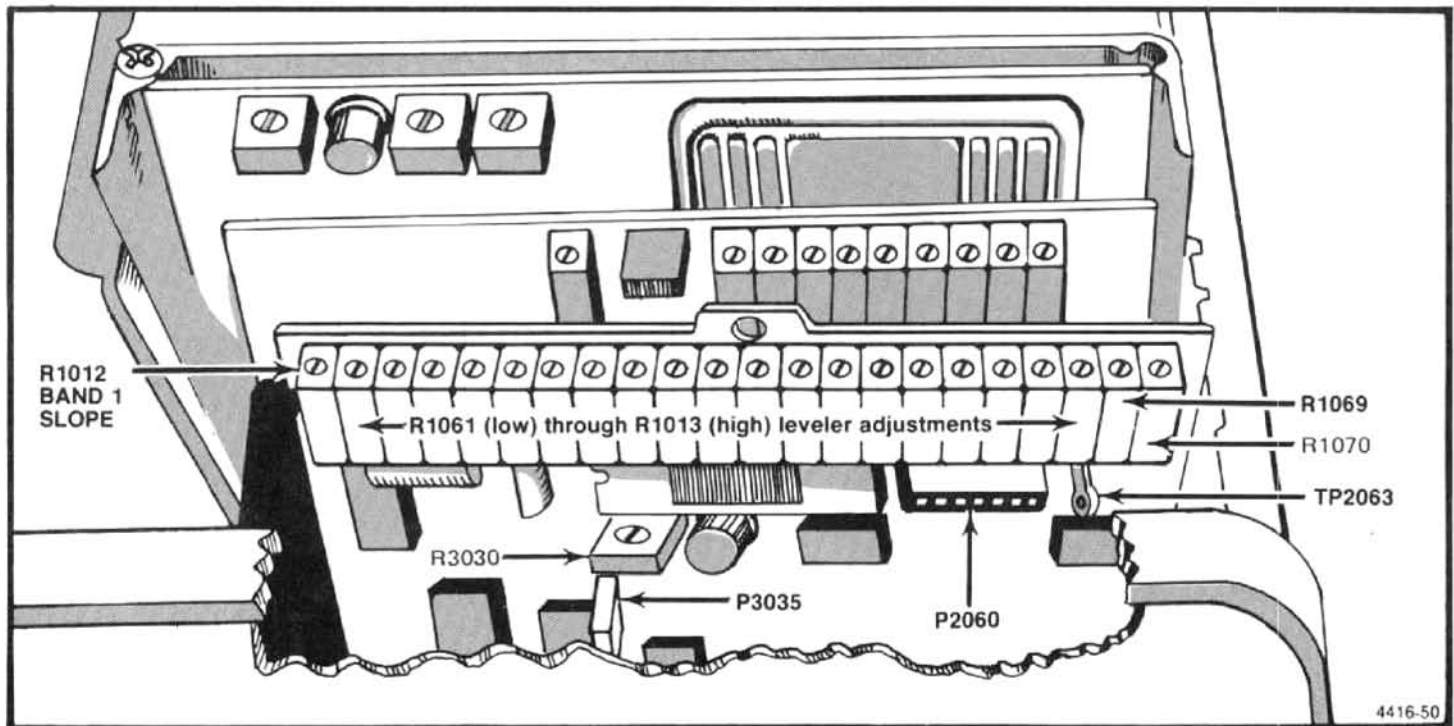


Figure 5-29. Adjustments and test points on the Video Processor.

r. Activate 10 dB/DIV and note the baseline. Activate NARROW Video Filter and adjust the REF LEVEL so the baseline moves to the top of the screen.

s. Press 2 dB/DIV and VIEW A, then adjust the REF LEVEL so SAVE A display and the baseline are at center screen.

t. Unplug P2060 (Figure 5-29) and move it from Normal to Invert mode position (one pin to the left). Replace Leveler Disable plug P3035.

u. Start with R1061 and adjust the leveling potentiometers sequentially, from R1061 through R1013, so the contour of the baseline is an average of the SAVE A display. In the process use Horiz adjust R1069 (Figure 5-29) to shift the baseline to the right or left so the baseline aligns with the average contour of SAVE A display.

v. Replace P2060 to the Normal mode position (one pin to the right). The baseline will now be 180° or the inverse of its previous position.

w. Deactivate and then activate VIEW A, VIEW B, SAVE A, and MAX HOLD. Retrace and check new response. Response should appear flat (Figure 5-28B).

x. Disconnect and remove the signal to the RF INPUT from the test equipment.

y. Compensation adjustment R3030 is set at the factory and usually does not require adjustment. Pull Leveler Disable plug P3035 then replace it. If the baseline remains straight or breaks up after the plug is replaced, compensation is required. Adjustment procedure is as follows:

(1) With the front-panel controls set as directed in part b, activate NARROW Video Filter and change TIME/DIV to 50 ms. Alternately turn the 19 level adjustments clockwise and counterclockwise so every other potentiometer is fully clockwise and the adjacent potentiometer is fully counterclockwise. Display should now appear as a periodic triangular waveform.

(2) Adjust the REF LEVEL so the baseline is near full screen then switch to the 2 dB/DIV mode and adjust so the display is mid-screen (Figure 5-30A).

(3) Turn Compensation adjustment R3030 counterclockwise until the display breaks up (Figure 5-30B).

(4) Now turn R3030 clockwise 1.5 to 2 turns past the point the display again becomes a periodic triangular waveform.

(5) Turn Horiz Adjust R1069 to center the display.

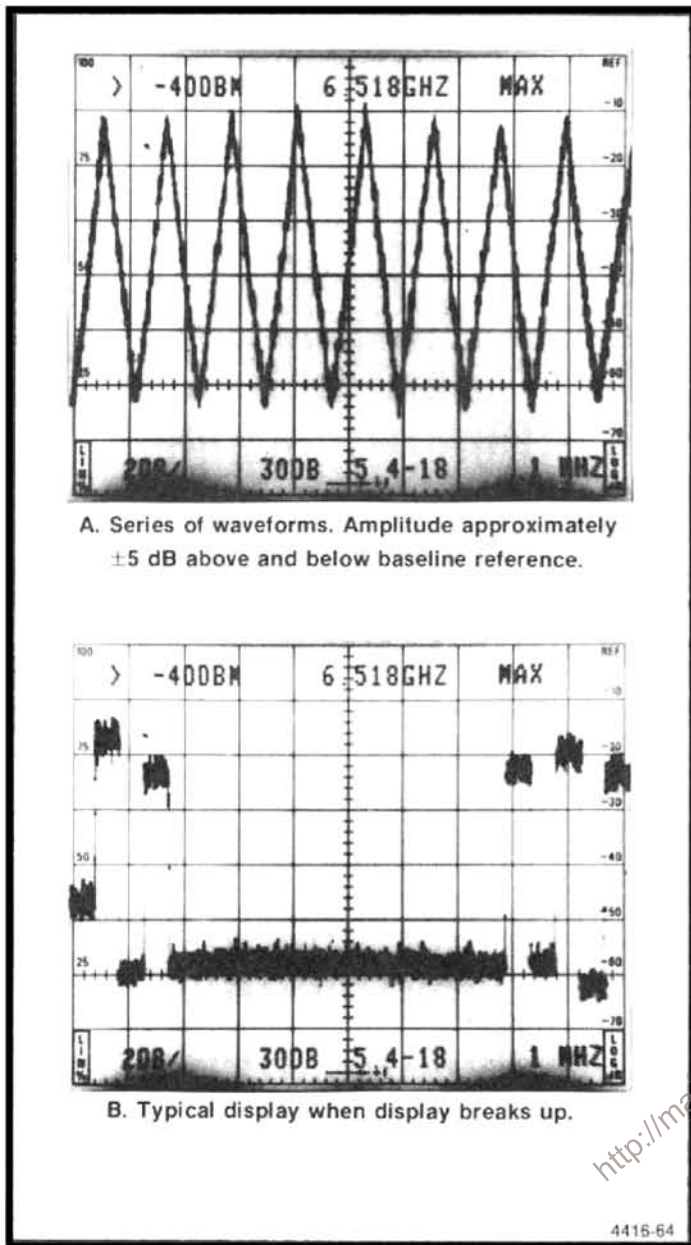


Figure 5-30. Typical response when adjusting compensation of the baseline leveling circuits.

(6) Return the baseline leveler adjustments to their midrange position for a straight line display and proceed with the baseline leveling alignment as previously described (parts a through x).

z. Adjust the slope of band 5 as follows:

(1) Readjust the Sweep Oscillator so it sweeps from 15 GHz to 21 GHz (Marker Sweep) and adjust the output so the power meter reads approximately -10 dBm.

(2) Adjust R1070 (Band 5 Slope) on the Video Processor board, fully counterclockwise.

(3) Set the CENTER FREQUENCY to 15 GHz, FREQUENCY RANGE to 15-21 GHz (band 5), FREQ SPAN/

DIV to MAX, REF LEVEL to -10 dBm and the TIME/DIV to 50 ms. Activate 10 dB/DIV and AUTO RESOLIN (UNCAL indicator will light).

(4) Select a 15 GHz marker on the Sweep Oscillator and adjust the output for -10 dBm as indicated on the power meter.

(5) Activate 2 dB/DIV and adjust the REF LEVEL so the signal amplitude is approximately 6 divisions. Adjust MANUAL PEAK for maximum response or activate AUTO PEAK.

(6) Change the Sweep Oscillator to Automatic Internal Sweep and set the Sweep Time for 100 s or its slowest sweep.

(7) Activate View A, View B, and MAX HOLD. Note the response as the oscillator sweeps.

(8) Activate SAVE A and deactivate MAX HOLD, then select CW Marker on the Sweep Oscillator and move the signal to the upper end of band 5 (19-21 GHz).

(9) Visualize an imaginary line through the midpoint of the saved display and select a point on the saved display (between 19 and 20 GHz) that intersects the imagined line.

(10) Switch VIEW A on and off as required while moving the CW Marker to the selected point.

(11) Switch VIEW A off and adjust R1070 until the CW Marker is at the 6 division level or maximum, whichever occurs first.

(12) Deactivate SAVE A and repeat steps (6 through 10) until the best overall flatness is achieved.

17. Band Leveling for Coaxial Bands (bands 1-5)

NOTE

The mean value of the frequency response for each band is set to a -20 dBm reference at 100 MHz. If the range of any band gain adjustments is insufficient, add a diode between the emitter of Q3036 and pins DD, on the VR#2 Mother board, as shown on the schematic diagram for Variable Resolution #2.

a. Perform Frequency Response Check of bands 1 through 5 as described in the Performance Check section and note the frequency at the mean level (average level between two extremes) for each band.

b. Perform "Presetting the Variable Resolution Gain and Band Leveling" adjustment step prior to proceeding with this step.

c. Test equipment setup is shown in Figure 5-31. Set the FREQUENCY RANGE to 1.7-5.5 (band 2), FREQ SPAN/DIV to 10 MHz, REF LEVEL to -20 dBm, and activate AUTO RESOLN, 2 dB/DIV, VIEW A and VIEW B.

d. Apply a calibrated -20 dBm signal, whose frequency is the same as that noted for the mean level in part a, to the RF INPUT. Set the FREQUENCY to the input signal and reduce the FREQ SPAN/DIV to 500 kHz.

NOTE

If a power meter is used to monitor signal level, connect the power meter sensor in line with the signal to the RF INPUT.

e. Adjust band 2 Gain R3034 on the VR#2 Mother board (Figure 5-32) for a full screen (-20 dBm) display.

f. Change the FREQUENCY RANGE to 3.0-7.1 GHz (band 3) and apply a calibrated -20 dBm signal with the same frequency as noted for the mean level in Band 3 for part a of this step.

g. Set the FREQUENCY to the incoming signal, FREQ SPAN/DIV to 500 kHz/Div and adjust band 3 Gain, R3030, (Figure 5-32) for a full screen display.

h. Repeat the above procedure for each coaxial band (1-5) and set the gain of each with the appropriate adjustment. If the range of any adjustment is insufficient, add or remove the appropriate diode (see schematics and component locator, in Volume 2) to obtain the required range. Adding the diode increases gain.

18. Band Leveling for Waveguide Bands (bands 6-11)

a. Test equipment setup is shown in Figure 5-31. Apply 2072 MHz at -30 dBm, through a dc-blocking capacitor to the EXT MIXER input. Monitor the input with a power meter to set the power level then add a known 30 dB attenuator so the input level to the EXTERNAL MIXER port is -60 dBm. Set the FREQUENCY RANGE to 18-26 GHz (band 6), FREQ SPAN/DIV to 200 MHz, REF LEVEL to -30 dBm, and activate AUTO RESOLN.

NOTE

The baseline of the display will rise when 2072 MHz signal is applied to the EXTERNAL MIXER input port connector.

b. With -60 dBm input level applied, adjust Band 6 Gain Leveling, R3024, (Figure 5-32) for full screen display.

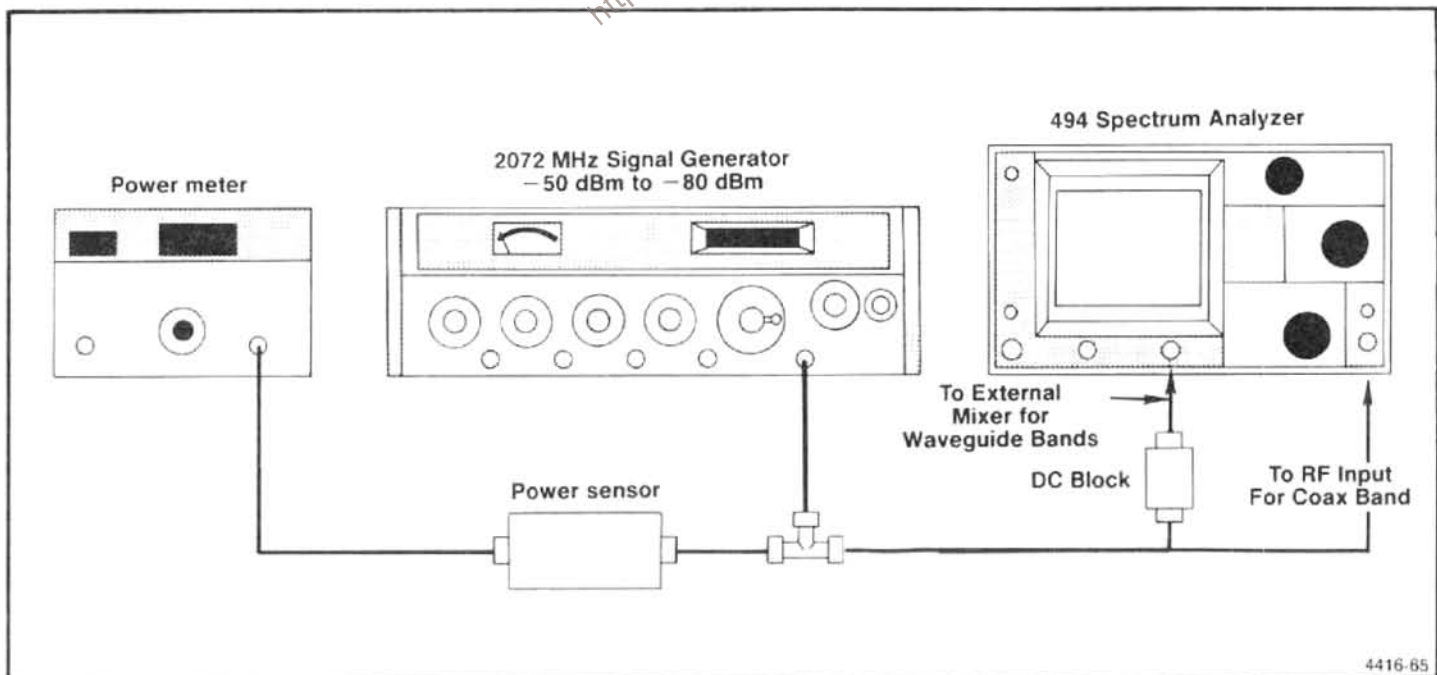


Figure 5-31. Test equipment setup for adjusting band leveling for the coaxial and waveguide bands.

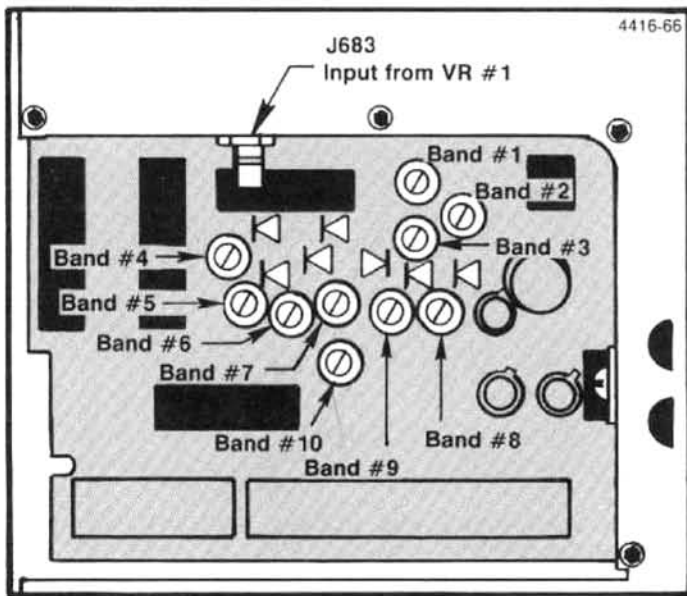


Figure 5-32. Band leveling adjustments and gain diodes on the VR#2 Mother board.

c. Change the FREQUENCY RANGE and input signal frequency and level as listed in Table 5-3, and adjust the appropriate Band Gain adjustments for a full screen display. Gain adjustment for the waveguide bands need to be adjusted only if these bands will be used.

Table 5-3
EXT MIXER BAND LEVELING ADJUSTMENTS

Band	Input Level	Gain Adjustment
6 (18-26 GHz)	-60 dBm	R3024
7 (26-40 GHz)	-60 dBm	R3026
8 (40-60 GHz)	-60 dBm	R3032
9 (50-90 GHz)	-60 dBm	R3029
10 (75-140 GHz)	-60 dBm	R3028
11 (110-220 GHz)	-60 dBm	R3028
12 (170-325 GHz)	-60 dBm	R3028

d. Switch POWER off; replace VR module, then switch POWER back on.

19. Phase Lock Calibration

The Phase Lock assembly normally requires calibration only after some part of the assembly has been repaired or replaced. Phase noise, produced by the phase lock loop, is specified for -70 dBc or better, 3 kHz out from the response. This should be checked before calibrating the assembly.

a. Test equipment setup is shown in Figure 5-33. Remove the Phase Lock module and the two cover plates so all circuit test points and adjustments are accessible. Plug the assembly on extender boards and into the instrument. Use extender cables and adapters to reconnect signal cables to their respective connector (cable with yellow band to J501, and the cable with black band to J502).

If desired, the direct reading counter can be connected to the Vertical Output of the test oscilloscope. This will enable the user to observe the display of a test point and get a count, if appropriate, throughout this procedure. The ground side of the test oscilloscope probe will serve as the common ground return for both instruments.

b. Press <SHIFT> CAL and do the directed calibration routine through adjusting the LOG CAL. Press <SHIFT> to return the instrument to normal operation and set REF LEVEL to -30 dBm. Check that the AUTO RESOLN is active (button lit).

c. Check Offset Mixer—This part of the procedure is only required after repair or replacement of the Mixer board.

(1) Connect the Direct Input of the Frequency Counter to pin N (Figure 5-34) and adjust the counter controls for a count. Note the frequency.

(2) Connect the counter to pin K and note the frequency.

(3) Connect the counter to the collector of Q1040 and note the frequency. Frequency should equal the difference between pins N and K (e.g., 25.080 - 25.000 = 80 kHz). Disconnect the counter probe from the collector of Q1040.

(4) Connect the probe of a test oscilloscope to the collector of Q1040 and check for a 50% duty cycle of the approximately 80 kHz signal and an amplitude that is approximately 5 V peak-to-peak.

d. Check Synthesizer

(1) With the FREQ SPAN/DIV at 200 kHz, phase lock should occur.

(2) Change FREQ SPAN/DIV to 500 kHz and connect the counter to J500 on the Synthesizer board. Check for a reading of 50.00 MHz.

(3) Connect the counter to TP2040 (Figure 5-34A) and check for a reading that is near 25.0 MHz.

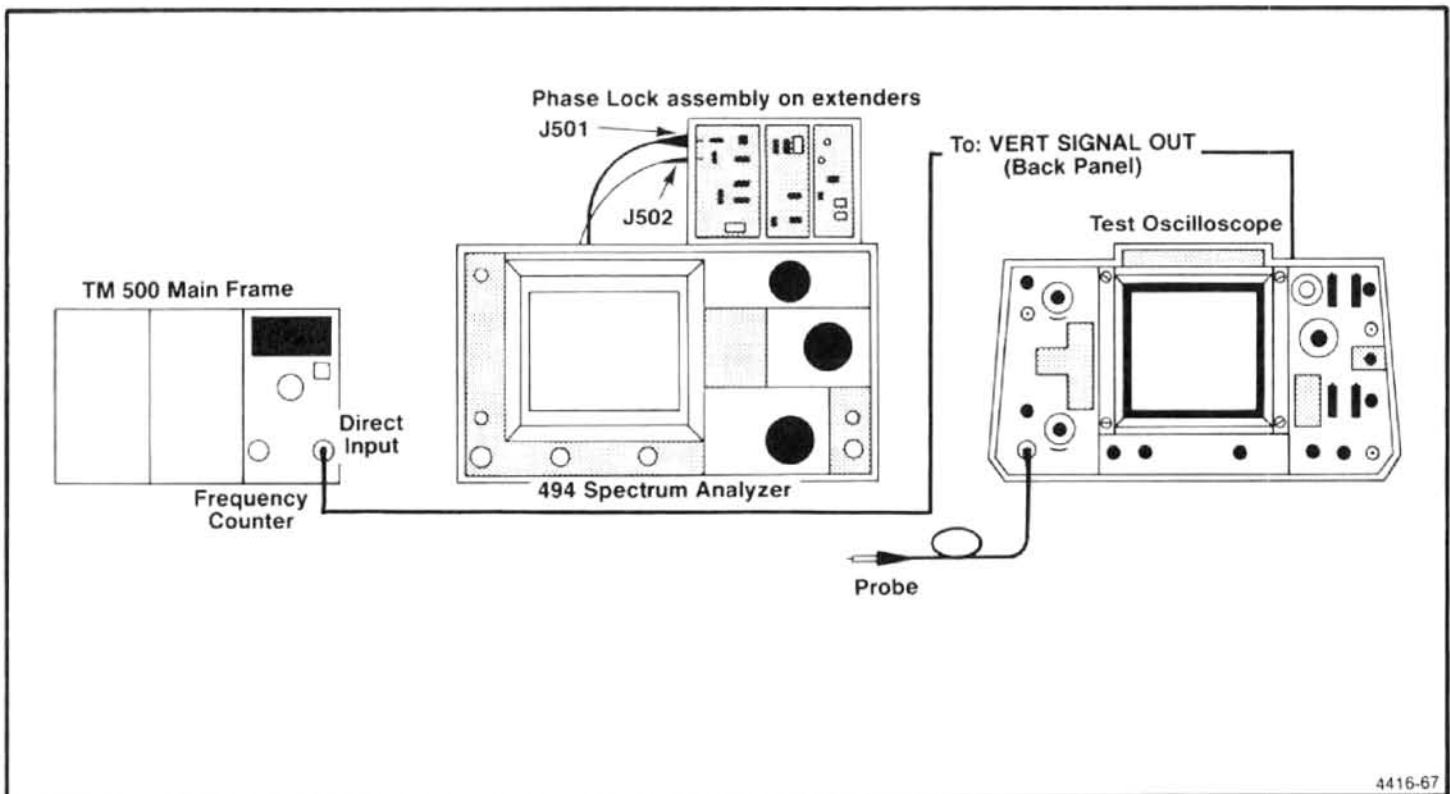


Figure 5-33. Test equipment setup for calibrating the Phase Lock assembly.

(4) Connect the test oscilloscope to TP1040 (Figure 5-34A) and check for positive pulses with an amplitude of approximately 4 V peak-to-peak.

(5) Change the FREQ SPAN/DIV to 200 kHz and observe that the signal on TP1040, in part (4), is still there.

e. Controlled Oscillator—This part of the check is only required after repair or replacement of the Controlled Oscillator board.

(1) Press <SHIFT> PULSE STRETCHER and select "Phase Lock Synthesizer" (#5) from the displayed menu.

(2) Follow the instructions until the message, "VERIFY LAST STEP". Due to the interaction of C1013 and C2011 adjustments, the two steps will have to be repeated until the voltages are correct. Alternately press AUTO RESOLN and IDENT and adjust until the two voltage readings are correct.

(3) Connect the counter to TP2011 on the Controlled Oscillator board (Figure 5-34A) and alternately press AUTO RESOLN and IDENT and check for a count reading of either 25.0943 MHz or 25.0328 MHz.

f. Check Operation of Strobe Driver

The "Phase Lock Synthesizer" test is still used for this test. If aborted, press <SHIFT> PULSE STRETCHER to return to the Synthesizer routine. Any step in the routine will work.

(1) Connect the test oscilloscope to TP2015 on the Strobe Driver board (Figure 5-34B) and check for a square wave response with a Time/Div setting of .05 μ s. Amplitude should be approximately 5 V peak-to-peak.

(2) Connect the test oscilloscope to TP2087 and check for a sinusoidal waveform of approximately 5 V peak-to-peak.

(3) Connect the counter to TP2087 and check for a count of either 5.018868 or 5.006477 MHz.

(4) Connect the test oscilloscope to P502 or P504 and check for 5 V logic level signals respectively.

(5) Press <SHIFT> to abort the test.

g. Error Amplifier—This procedure sets loop gain which is required when either the Phase Lock assembly, 1st LO, Phase Detector, or Error Amplifier is replaced.

(1) Set FREQ SPAN/DIV to 200 kHz then press <SHIFT> EXT Triggering. The "Diagnostic Aids" menu will now be displayed. Select "1st LO Phase Lock" (0) and press HELP, phase lock should be disabled.

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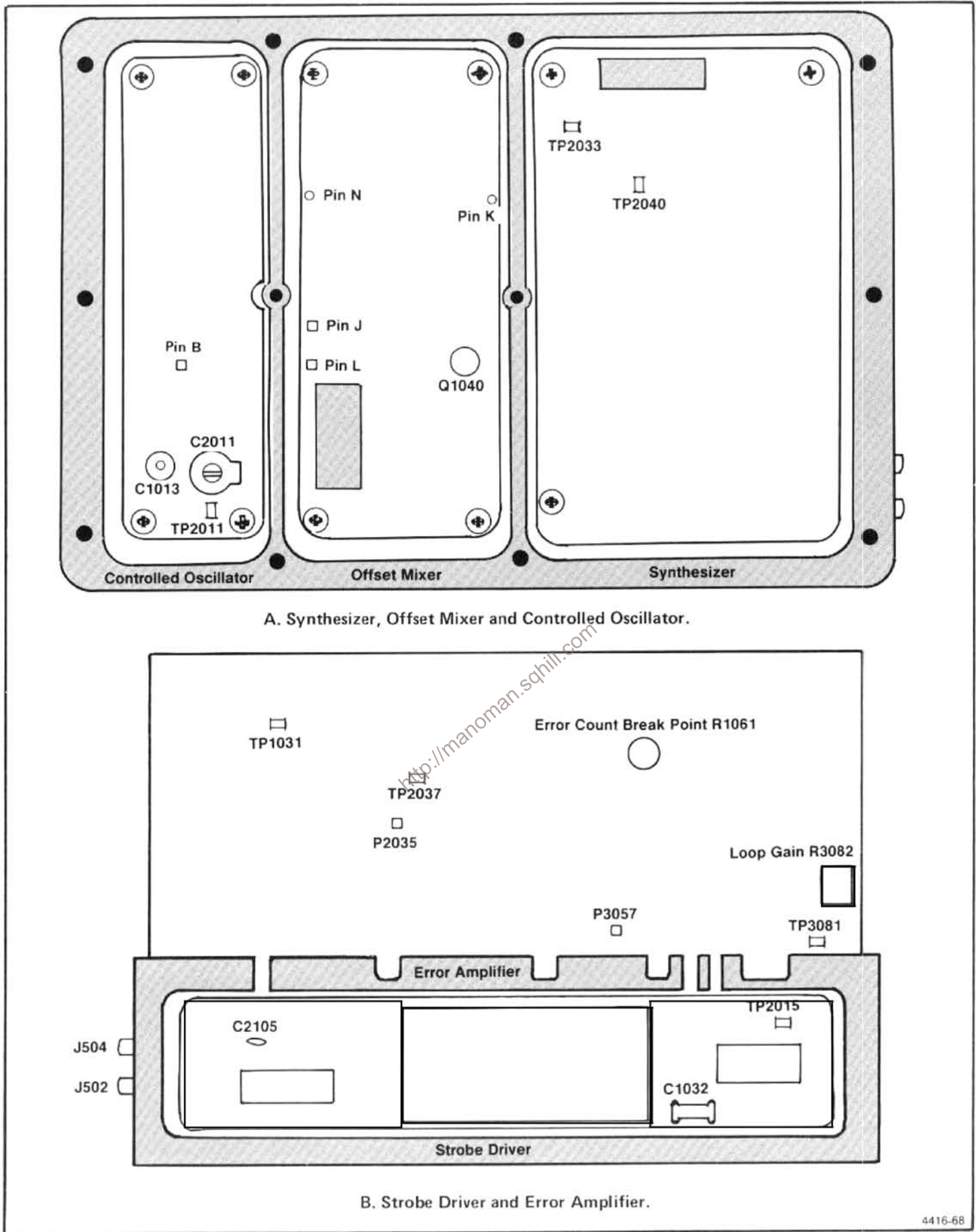


Figure 5-34. Adjustments and test points in the Phase Lock assembly.

(2) Connect the test oscilloscope to TP2038 (Figure 5-34B) and set test oscilloscope Time/Div to 20 ms. Check for a waveform with an amplitude that is approximately 6 V peak-to-peak.

(3) Press HELP to enable phase lock and note that the message indicates "LOCK ENABLED". Connect the test oscilloscope to TP3081 (Figure 5-34B) and adjust R3082 from stop to stop and note that the beat note signal varies in amplitude. Press <SHIFT> to abort the Cal routine.

(4) Set the TIME/DIV to AUTO, FREQUENCY RANGE to band 2 (1.7-5.5 GHz), and FREQUENCY SPAN/DIV to 50 kHz.

(5) Pull P3057 (Figure 5-34B), this turns the strobe to the Phase Gate on. Turn Loop Gain R3082 fully counterclockwise.

(6) Connect the test oscilloscope probe to TP3081 and trigger the test oscilloscope on the signal at TP2037 (U2048-6) shown in Figure 5-34B. Set the test oscilloscope Time/Div to 5 ms and Volts/Div to 0.5 V. Note the beat notes. Beat notes are produced by the difference between strobes from the phase lock (one every 5 MHz) and the particular frequency the 1st LO is tuned to.

(7) Increase FREQ SPAN/DIV to MAX, set RESOLUTION BANDWIDTH to 100 Hz, and TIME/DIV to AUTO. Deactivate VIEW A and VIEW B if needed.

(8) As the sweep scans across the span, note the position of the smallest beat note. Tune the CENTER FREQUENCY to position the frequency dot at this location, then reduce the FREQ SPAN/DIV to 20 MHz. Set TIME/DIV to 1 s and activate VIEW A.

(9) Check that the beat note is 3 V peak-to-peak or more. If this does not occur, it is an indication the Phase Gate is defective.

(10) Install P3057, disconnect the test oscilloscope trigger and probe connections. Ensure that P3057 is installed correctly; its absence will produce spurious responses on the display.

(11) Reduce FREQ SPAN/DIV to 200 kHz and ensure that phase lock occurs, by the absence of error message and a sweep. Replace the covers on the assembly and reinstall the module in the instrument. Perform the phase lock noise check as described in the Performance Check section.

h Check Strobe Driver—Excessive noise on the display and intermittent lock are indications that the strobe pulse out of the Strobe Driver is noisy or low in amplitude. This can be caused by a mismatch in input or output impedance to the band-pass filter FL2064. The following procedure is required if the filter or any component that affects the input or output impedance match is replaced.

(1) With the instrument in phase lock mode (FREQ SPAN/DIV 200 kHz or less), connect a test oscilloscope probe to TP2087. Note the amplitude of the 5 MHz strobe signal. Amplitude of the sinusoidal strobe signal is normally 5 to 6 V peak-to-peak.

(2) If the strobe signal amplitude is low and noisy, change the value of select capacitors C1032 and C2105 to obtain the maximum strobe pulse amplitude at TP2087. Value of these capacitors range from 3.3 to 27 pF.

(3) If the signal amplitude is still low, connect a frequency counter probe to TP2015. Frequency must range from 5.0067 to 5.0188 MHz. Frequency is a function of the Controlled Oscillator assembly and counter U1022.

This concludes the Adjustment Procedure. Repeat the appropriate Performance Check to verify specification.

MAINTENANCE

INTRODUCTION

This section describes procedures for reducing and preventing instrument malfunction, troubleshooting methods, corrective maintenance, and procedures for recalibrating those assemblies that normally do not require routine calibration.

Removing the Instrument from its Cabinet

To prepare the rackmount or benchtop version for maintenance or adjustment, refer to the Rackmount/Benchtop part in the Options section for instructions on removing the instrument from its cabinet. The following applies to the standard 494/494P instrument:

1. Set the instrument on its face or front panel.
2. Loosen the four screws through the back rubber feet.
3. Pull the cover up and off the 494/494P.
4. Place the instrument on the work space (bench) and reconnect the power cord.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by the body, never by the leads.
7. Do not slide the components over any surface.
8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
9. Use a soldering iron that is connected to earth ground.
10. Use only special anti-static suction type or wick type desoldering tools.

Static-Sensitive Components

This instrument contains electrical components that can be damaged by static discharge. See Table 6-1 for the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV can occur in unprotected environments.



Static discharge can damage any semiconductor component in this instrument.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers, on metallized or conductive foam. Label packages that contains static-sensitive assemblies or components.
3. Discharge body static voltage by wearing a grounded wrist strap while handling these components. Static-sensitive assemblies or components should be handled and serviced only at static-free work stations by qualified service personnel.

Table 6-1
RELATIVE SUSCEPTIBILITY
TO STATIC DISCHARGE DAMAGE

Semiconductor Classes	Relative Susceptibility Levels ^a
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

^aVoltage equivalent for levels:

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V(est.)
 2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
 3 = 250 V 6 = 600 to 800 V 9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, performance check, and if needed a recalibration. The preventive maintenance schedule that is established for the instrument should be based on the environment in which the instrument is operated and the amount of use. Under average conditions (laboratory situation) a preventive maintenance check should be performed every 1000 hours of instrument operation.

Elapsed Time Meter

A 5000 hour elapsed time indicator, graduated in 500 hour increments, is installed on the Z-Axis/RF Interface circuit board. This provides a convenient way to check operating time. The meter on new instruments may indicate from 200 to 300 hours elapsed time because most instruments go through a factory burn-in time to improve reliability. This is similar to using aged components to improve reliability and operating stability.

Cleaning

Clean the instrument often enough to prevent dust or dirt from accumulating in or on it. Accumulation of dirt and grease acts as a thermal insulating blanket and prevents efficient heat dissipation. It also provides high resistance electrical leakage paths between conductors or components in a humid environment.

Exterior. Clean the dust from the outside of the instrument by wiping or brushing the surface with a soft cloth or small brush. The brush will remove dust from around the front-panel selector buttons. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

Interior. Clean the interior by loosening accumulated dust with a dry soft brush, then remove the loosened dirt with low pressure air to blow the dust clear. (High velocity air can damage some components.) Hardened dirt or grease may be removed with a cotton tipped applicator dampened with a solution of mild detergent in water. Do not leave detergent on critical memory components. Abrasive cleaners should not be used. If the circuit board assemblies need cleaning, remove the circuit board by referring to the instructions under Corrective Maintenance in this section.

After cleaning, allow the interior to thoroughly dry before applying power to the instrument.



Do not allow water to get inside any enclosed assembly or components such as the hybrid assemblies, RF Attenuator assembly, potentiometers, etc. Instructions for removing these assemblies are provided in the Corrective Maintenance part of this section. Do not clean any plastic materials with organic cleaning solvents such as benzene, toluene, xylene, acetone or similar compounds because they may damage the plastic.

Lubrication

Components in this instrument do not require lubrication.

Fixtures and Tools for Maintenance

Table 6-2 lists kits and fixtures that are available to aid in servicing the 494/494P:

Table 6-2
SERVICE KITS AND TOOLS

Nomenclature	Tektronix Part No.
Service Kit	006-3286-00
consisting of:	
1 Front panel extender	067-0973-00
1 Power module extender	067-0971-00
1 Accessories Interface extender	067-0972-00
1 Ribbon cable	175-2901-00
3 Coaxial cables, Seaelectro male-to-Seaelectro female	175-2902-00
1 VR module handle	367-0285-00
1 Circuit board extender assembly kit, consisting of:	672-0865-01
1 Left extender board	670-5562-00
2 Right extender boards	670-5563-00
1 Right GPIB extender board	670-8493-00
1 Frame (extrusion for circuit board extender)	426-1527-00
6 Screws, panhead with flat and lockwashers	211-0116-00
Screwdriver, flat, with 1/4 to 3/8-inch bit.	
Screwdriver, Posidrive® 440-2.	
Wrench, 5/16-inch open-end (used to remove or replace semi-rigid coaxial cable connectors).	
Hex drive wrenches, 3/32, 5/64, 7/64-inch (used to remove hex screws that hold module assemblies and their covers in place).	

Visual Inspection

After cleaning, carefully check the instrument for such defects as defective connections, damaged parts, and improperly seated transistors and integrated circuits. The remedy for most visible defects is obvious. If heat-damaged parts are discovered, try to determine the cause of overheating before the damaged part is replaced; otherwise, the damage may be repeated.

Transistor and Integrated Circuit Checks

Most transistors and integrated circuits are soldered on the boards to prevent pin contact problems. Periodic checks of the transistors and integrated circuits is not recommended. The best measure of performance is the actual operation of the component in the circuit. In most cases any degradation in performance will be detected by the microcomputer when it runs its power up routine. Performance of these components is also checked during the performance check or recalibration; any sub-standard transistors or integrated circuits will usually be detected at that time.

When handling MOS FET's, keep the shorting strap in place until the transistor is in its socket.

Performance Checks and Recalibration

The instrument performance should be checked after each 1000 hours of operation or every six months if the instrument is used intermittently to ensure maximum performance and assist in locating defects that may not be apparent during regular operation. Instructions for conducting a performance check are provided by the Performance Check section of the service instructions.

Saving Stored Data in Non-Volatile Memory for 494P Instruments

If either the Memory or GPIB board are removed from the instrument, data stored in non-volatile memory will be lost because the back-up battery on the GPIB board is disconnected. A program for storing data on tape is provided at the end of this section.

TROUBLESHOOTING

The 494/494P contains firmware that will troubleshoot the frequency control system and the power supply. Troubleshooting procedure for this system and the power supply is provided in the Diagnostics part of this section. Also included with this part is a description of the 494/494P trace modes and their actions. After the defective assembly or component has been located, refer to the Replacing Assemblies and/or Sub-assemblies part of this section for removal and replacement instructions.

The following aids and techniques may help locate a problem or trouble in the instrument.

Troubleshooting Aids

Diagrams—Functional block and circuit diagrams, on foldout pages in the Diagrams section, contain significant waveforms, voltages, and logic data information. Any necessary information as to how the data was acquired, such as operational state of the instrument, is provided on the diagram or adjacent to it. Refer to the Replaceable Electrical Parts list section for a description of all assemblies and components. Diagrams are arranged in signal flow sequence and by sections, such as RF section, IF section, frequency control section, etc., with an accompanying functional block diagram.

Schematic diagrams list the Tektronix Part No. (670 xxxx-) for the assembly or board along with the assembly number (A50) and name. The last two digits or suffix of the part number are not indicated on the diagram; however, they are listed in the Electrical Parts section. These two digits reflect changes or modifications to the assembly or board. When a change is made to the assembly, the suffix rolls one digit. The diagram indicates these changes with a grey tint drawing of the original circuit or if a component changes value the symbol is enclosed with a grey tint box. When a major modification is made to an assembly or board and it is no longer compatible with earlier instruments, a new part number is assigned and a separate schematic with associated illustrations is added. All diagrams indicate the new part number and the instrument serial number break. If the assembly is compatible with earlier instruments and the change is significant enough to require a separate schematic, this will also be identified.

NOTE

Corrections to the manual and instrument modifications, if significant, are documented by adding inserts, bound into the rear of the manual, until the information is added to the manual text. Check this "Change Information" section for these changes to the manual or the instrument.

Circuit Board Illustrations and Component Locator Charts—Electrical components, connectors, and test points are identified on circuit board illustrations that are located on the inside fold of the corresponding circuit diagram or the back of the preceding diagram. A grid on the circuit board illustration and the circuit schematic, plus a look-up table, provide the means to quickly locate components on either the diagram or the circuit board.

In most cases, circuit numbers are assigned according to the physical location of the component on the board or assembly. The first digit designates the row of a grid, the second the column, with the last two reserved as an expander. Three digit numbers designate chassis mounted components.

General Troubleshooting Techniques

Before using test equipment, to measure across static-sensitive components or assemblies, be certain that voltages or current supplied by the test equipment does not exceed the limits of the components to be tested.

Try to isolate the problem to a component through signal analysis. Determine that circuit voltages will not damage the replacement.

Semiconductor Checks—Semiconductor failures account for the majority of electronic equipment failures. Most semiconductors are soldered to the boards to reduce pin contact problems. The following guidelines should be observed if you substitute any of these components.

1. Turn the power off before removing an assembly or board.
2. Use a de-soldering tool and 25 W or less soldering iron to remove the components.
3. Use only good components for substitution. Be sure the new component is inserted into the board properly before soldering. Refer to the manufacturer's data sheet or Figure 6-1 for IC and transistor lead configuration. IC sockets have a square or rectangular socket to identify pin 1 of the device.

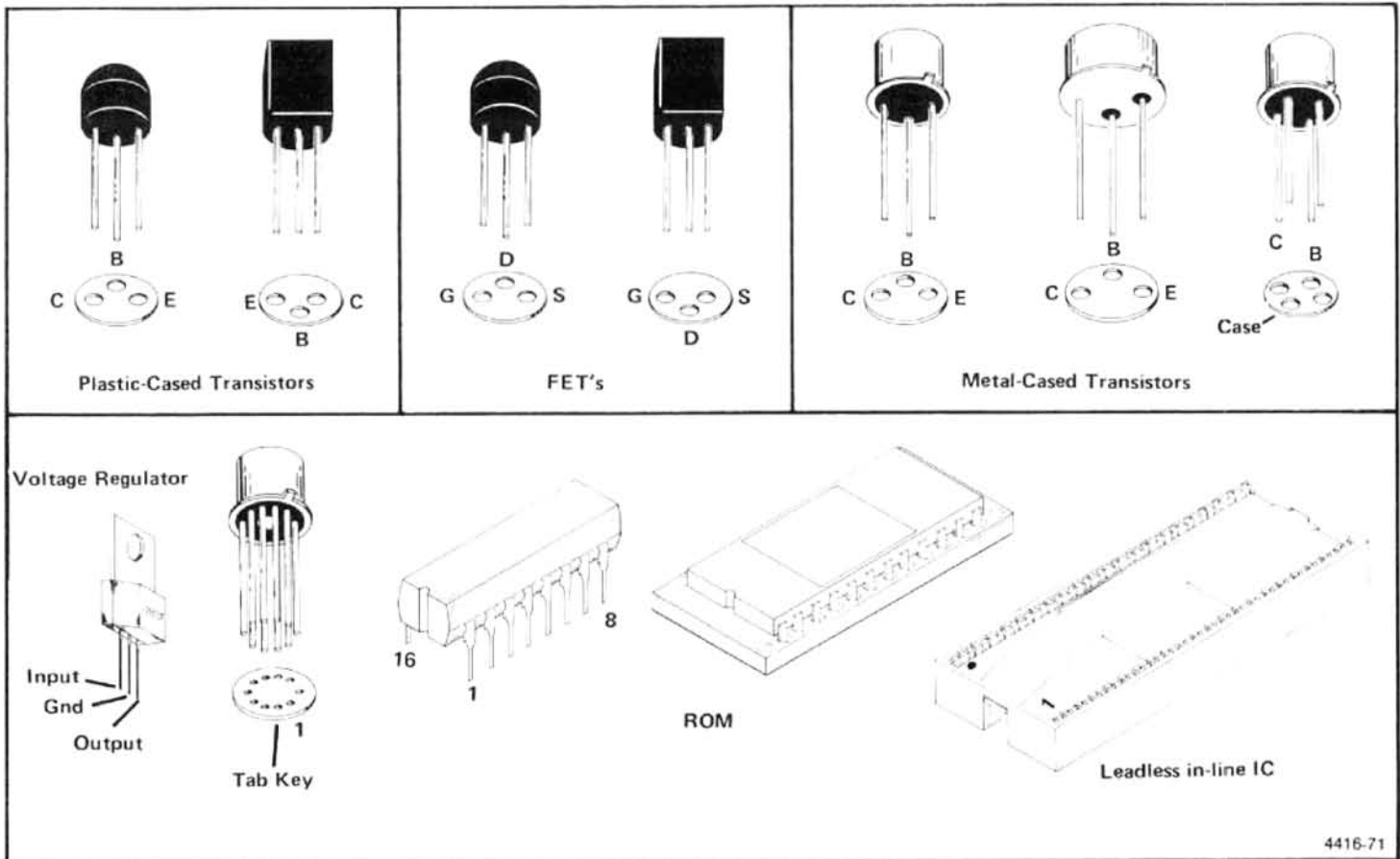


Figure 6-1. Electrode configuration for semi-conductor components.

NOTE

If a substitute is not available, check the transistor or MOS FET with a dynamic tester such as the TEKTRONIX Type 576 Curve Tracer. Static type testers, such as an ohmmeter, can be used to check the resistance ratio across some semiconductor junctions if no other method is available; however, **DO NOT MEASURE RESISTANCE ACROSS MOS FET's** because they are very susceptible to static charges. Use the high resistance ranges ($R \times 1k$ or higher) so the external test current is limited to less than 6 mA. If uncertain, measure the external test current with an ammeter. Resistance ratios across base-to-emitter or base-to-collector junctions usually run 100:1 or higher. The ratio is measured by connecting the meter leads across the terminals, note the reading, then reverse the leads and note the second reading.

Diode Checks—Most diodes can be checked in the circuit by taking measurements across the diode and comparing these with voltages listed on the diagram. Forward-to-back resistance ratios can usually be taken by referring to the schematic and pulling appropriate transistors and pin connectors to remove low resistance loops around the diode.

CAUTION

Do not use an ohmmeter scale with a high external current to check diode junctions. Do not check the forward-to-back resistance ratios of mixer diodes. See Replacing the Dual Diode Assembly under Removing and Replacing Assemblies.

Diagnostic Firmware

The 494/494P has firmware that contains diagnostic routines that can be used with the Diagnostic part of this section to troubleshoot the Frequency Control system and diagnose Power Supply problems. This part follows General Troubleshooting information. Refer to this part to help isolate problems within this loop. The following are also some general suggestions that may help isolate a problem when troubleshooting.

Troubleshooting Steps

1. Ensure that the problem exists in the 494 by checking the operation of associated equipment and recheck the operation of the 494/494P.

2. Try to isolate the problem to a circuit or at least board level by evaluating operational symptoms; for example, absence of the frequency dot could be caused by a malfunction in the video summing stage, the marker generator, or switching circuits.

3. Three levels of block diagrams are provided to aid in understanding the theory of operation. The most detailed level is adjacent to the schematic and usually provides signal and voltage levels at critical points within the circuits. Signal levels are usually the levels required to produce full screen deflection.

4. Instructions on how to remove or replace those assemblies, which are not obvious, are provided in this section. Refer to this part before removing any assembly for testing or repairing.

5. Visually inspect the area or assembly for such defects as broken or loose connections, improperly seated components, overheated or burned components, chafed insulation, etc. Repair or replace all obvious defects. In the case of overheated components, try to determine the cause of the overheated condition and correct before applying power.

6. Use successive electrical checks to try to locate the problem. An oscilloscope or signature analyzer is a valuable test item for evaluating circuit performance. If applicable, check the calibration adjustments; however, before changing an adjustment note its position so it can be returned to its original setting. This will facilitate recalibration after the trouble has been located and repaired.

7. Determine the extent of the repair needed; if complex, we recommend contacting your local Tektronix Field Office or representative. If minor, such as a component replacement, see the Replaceable Parts list for replacement information. Removal and replacement procedure of the assemblies and sub-assemblies are described under Corrective Maintenance.



When measuring voltages and waveforms, use extreme care when placing meter leads or probes. Some circuit boards have a high component density, access to points within circuits is limited. An inadvertent move of test leads or probe can short a circuit and generate transient voltages that can destroy many static sensitive components.

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DIAGNOSTIC

This part consists of explanations and procedures for troubleshooting the frequency control system and the power supply using diagnostic firmware that is in the 494/494P.

TROUBLESHOOTING THE 494/494P USING THE ERROR MESSAGE DISPLAY

Introduction

This part contains procedures for troubleshooting the frequency control system and the power supply. When the micro-processor detects a failure or error in the Frequency Control loops, or a failure in the Power Supply voltages, it will cause the 494/494P to display an error message near center screen for a few seconds; this is followed by an error status message near the top of the screen which remains as long as the error or problem exists.

These error messages pertain to problems that exist under current instrument operational modes or front panel settings; for example, an error that pertains to the hardware in the phase lock loop will exist only when the instrument is in the phase lock mode (narrower span/div settings).

NOTE

Because the frequency control loop may be unlocked when using the internal reference frequency in a "cold" instrument, no error message is displayed for the internal reference unlocked condition. However, "INT-UNLK" is displayed at the REFERENCE OSCILLATOR position for the normal instrument readout. The procedure that deals with "FREQUENCY REFERENCE UNLOCKED" message should be followed if "INT-UNLK" appears after the instrument is warm.

The following troubleshooting procedures are keyed to the brief error messages. Some problems may produce more than one error message in which case the 494/494P will display only the predominant error. A listing of all error messages will be displayed if you press <SHIFT> HELP. Combinations of error messages may help determine and expedite the process of finding the problem.

Some of the procedures use firmware diagnostics aid routines which can only be accessed by placing switch #3 of the Options switch (S1038) on the Memory board in the open position.

Combination of Error Messages

The following is a list of error message combinations and suggestions as to their cause. If the problem is not resolved with the following suggestions, or if the combination of error messages displayed is not covered, proceed to the listing of each error message and how to troubleshoot the problem.

"POWER SUPPLY OUT OF REGULATION" in combination with any other message(s).

A missing or inaccurate supply voltage is probably causing the other errors. Proceed to the "POWER SUPPLY OUT OF REGULATION" procedure which follows.

"FREQUENCY REFERENCE UNLOCKED" in combination with any or all of "TUNING FAILURE — 1ST LO," "TUNING FAILURE — 2ND LO," "PHASELOCK FAILURE — 1ST LO," and "COUNT NOT ACCURATE"

The 100 MHz oscillator probably has failed. If the "COUNT NOT ACCURATE" message appears when in counter mode, there is probably no oscillator output. Check, by applying the CAL OUT to the RF INPUT and tune to 100 MHz, with the FREQ SPAN/DIV set to 10 MHz, and AUTO RESOLN activated.

If the counter mode does not produce an error message, there is output from the 100 MHz oscillator; however, the oscillator frequency may be off. If the oscillator frequency has shifted enough to cause other problems, the crystal oscillator, and not other portions of the reference loop, has failed. Note, however, when using the internal reference frequency, the loop may not lock for up to 5 minutes, after initial turn on. This is normal during instrument warmup time. Such a condition is not a real failure and cannot drive the 100 MHz oscillator far enough to produce the other error messages. If this combination of error messages occurs within 5 minutes of power-up, wait until the instrument warms up or use an external reference to see if the frequency reference system has really failed.

“TUNING FAILURE — 1ST LO” and “TUNING FAILURE — 2ND LO”

Select the counter mode, and if the “COUNT NOT ACCURATE” message appears, refer to the next part of this procedure. The CF Control board is probably the cause, particularly if signals do not tune or do not tune smoothly. The problem is probably the voltage reference or in the digital control section.

“TUNING FAILURE — 1ST LO,” “TUNING FAILURE — 2ND LO,” and “COUNT NOT ACCURATE.”

The failure is probably on the Counter board or in the 100 MHz path from the 3rd Converter through the Auxiliary Synthesizer board to the Counter board.

Procedure Format

The format for these procedures is such that the problem is diagnosed in a descending order. The aim, to isolate a problem down to one part of the system, usually an assembly (such as a module or board) or a functional section of the assembly. After the problem has been isolated to the assembly or circuit level, refer to the diagrams and circuit description, as suggested under General Troubleshooting Techniques, for further isolation.

The procedures are structured as follows:

Error Message

Troubleshooting procedure

1. _____
- a. _____
- b. _____ (E)
- 1) _____
- 2) _____ (E)
2. _____ etc

Steps at the same level are either sequential or alternative steps, based on measurement or observation. Proceed to the lower-level steps only if the conditions of the higher-level steps are met. If the conditions are not met, proceed to the next step at the same level. An “(E)” at the end of a step, signifies this is as far as this procedure can take you to locate the problem.

Several of the troubleshooting procedures require that frequencies be counted and compared to either an expected value or the number counted by the internal 494/494P counter. To prevent any errors, the external frequency counter and the 494 counter should be operated from the same reference. If the external counter has a reference frequency output that has the proper frequency and amplitude level—the recommended frequency counter has this output—connect its output to the EXT REF INput for the 494/494P. The 494/494P counter and the external counter can also use the same external reference. If the counter and analyzer cannot be operated from the same reference, the error introduced may be up to several hundred Hz/GHz of measured frequency.

These procedures, unless specified, assume the frequency range is either band 1 (0–1.8 GHz) or band 2 (1.7–5.5 GHz).

Some failures, in the frequency control system, may appear only at specific oscillator frequencies. If this occurs, in a higher frequency range, the fundamental frequency of the appropriate oscillator should be determined so it can be set to the same frequency in the lower bands. This can be done by: 1) Switch #3 of S1038 (Options) on the Memory Board to the "open" position. 2) Press <SHIFT> READOUT and select from the readout menu, "1" for the 1st LO readout or "2" for the 2nd LO readout. 3) After noting the frequency of the oscillator, press <SHIFT> READOUT and "0" to return to the normal center frequency readout mode.

Since the instrument's power is usually switched on and off during troubleshooting, the power-down settings, that are automatically stored in register 0 of nonvolatile memory, should be recalled so the instrument settings and operating mode duplicate those that existed when the error message was generated.

The following, describes each error message and the procedures recommended to locate the problem.

"POWER SUPPLY OUT OF REGULATION"

Any out-of-tolerance voltage will cause this error message to be displayed. A power supply status circuit within the power supply will change the status LED on the Z-Axis board from green to red when any supply, except –17 V, changes by more than 25%. An error message will be also be displayed. An apparent power supply failure can be produced when either the supply fails or a circuit demands excessive current and blows a protective fuse or produces a current limit condition. The following procedure should determine those voltages that are out of range and whether the failure is in the supply or in a circuit outside the supply. Use a DVM to measure voltages.

Troubleshooting Procedure

WARNING

The 494/494P uses a high efficiency power supply, with the primary ground potential different from chassis or earth ground. An isolation transformer, with a turns ratio of 1:1 and a 500 VA minimum rating, should be used between the power source and the 494/494P power input receptacle. The transformer must have three-wire input and output connectors with a through ground between input and output. Stancor GIS1000 is an example of a suitable transformer. A jumper should also be connected between the primary ground side to chassis ground (emitter of Q2061 and the ground terminal of the input filter FL301).

If the power supply is separated from the instrument and operated on the bench, hazardous potentials exist within the supply for several seconds after power is disconnected. This is due to the slow discharge of capacitors C6101 and C6111. DS5112 (next to C6111) lights when the potential exceeds 80 V.

1. Verify that the power supply status LED, on the Z-Axis board, is red. If the LED is green, there is probably a failure in the microprocessor interface. **(E)**
2. Measure the power supply voltages at the test points on the Z-Axis board. To access the test points, remove the hold down cover over the Sweep and Z-Axis boards.



300 V and 100 V are present on the Z-axis board.

The ranges for each supply are listed in Table 6-3. These are tolerance limits which are much tighter than the limits used by the power supply sensing circuit. A supply that exceeds these limits may not trigger the error message or cause the instrument to malfunction. The +15 V supply is adjustable and affects the other supplies. Refer to the Adjustment Procedure section of the manual for adjustment information if a supply is just out of tolerance.

**Table 6-3
POWER SUPPLY RANGES**

Supply	Range	Test Point	Circuit Protection
+300 V	280 V to 310 V	TP1052	Fuse (F1033)
+100 V	95 V to 105 V	TP1048	Fuse (F1035)
+17 V	16.8 V to 18.6 V	TP1047	Fuse (F2013)
+15 V	14.85 V to 15.15 V	TP1046	Current limit
+9 V	8.5 V to 10.5 V	TP1011	Fuse (F1017)
+5 V	4.8 V to 5.2 V	TP1044	Current limit
-5 V	-4.8 V to -5.2 V	TP1036	Current limit
-7 V	-7 V to -8.5 V	TP1037	Fuse (F1013)
-15 V	-14.85 V to -15.15 V	TP1035	Current limit
-17 V ^a			Fuse (F3038)
Gnd		TP1034	Ground Reference

^aThe -17 V supply is not monitored by the power supply status circuit nor does it have a test point on the Z-Axis board. If this supply fails, the cooling fan will not run. (The fan will also not run if the ambient temperature is low.) The -17 V supply will probably affect other supplies as well.

- a. If all supplies are within limits and the power supply status LED is red, the problem is probably in the power supply status circuit on the Z-Axis board. R1065 may be misadjusted; adjust R1065 to see if the LED changes to green. If it changes, set R1065 at the center of the "green" range. **(E)**
- b. If the +17 V or -17 V supply and any other supply or supplies are inaccurate, or if both the +9 V and +5 V supplies are inaccurate, the trouble is likely in the Power Supply. **(E)**
- c. If the voltage is high (in absolute value), the trouble is probably in the Power Supply. **(E)**
- d. If the voltage from a fused supply is inaccurate, the trouble is probably in the Power Supply. **(E)**
- e. If the voltage from a fused supply is absent, it indicates the fuse could be blown. To access the fuses, remove the cover at the top left hand corner of the Power Supply module (as viewed from the front of the instrument). A blown fuse generally indicates that one of the circuits that this supply furnishes is defective; however, a fuse may open without an overcurrent condition. Replace the fuse and try again. If the fuse blows, the trouble is definitely in one of the circuits the supply furnishes.

If the fuse is not blown and the voltage is still absent, it indicates the trouble is in the Power Supply. **(E)**

- f. If the voltage from a current limited supply is absent or low, the problem could be the supply, or circuits the supply furnishes may be drawing excessive current. Turn the POWER off, then disconnect the suspect assemblies or modules from the supply and re-measure the voltage, see Table 6-4; or, remove the Power Supply from the instrument and measure the unloaded voltages on the Power Supply connector.

Table 6-4
POWER SUPPLY EDGE CONNECTOR VOLTAGES

Supply	Pin on Edge Connector
+300 V	W
+100 V	20
+17 V	U
+15 V	C,D,3
+9 V	T,16
+5 V	R,S,14,15
-5 V	H
-7 V	17
-15 V	E,F,6

- 1) If the supply voltage is correct with assembly or module removed, or when the voltage with the power supply removed is normal, the circuits this supply furnishes are causing the problem. **(E)**
- 2) If the voltage for the unloaded supply voltage is still inaccurate, the power supply is defective. **(E)**

“FREQUENCY REFERENCE UNLOCKED”

This error message is displayed when a comparator on the tuning voltage line for the 100 MHz VCO, detects that the voltage is outside its normal range. The unlocked condition is normal for up to 5 minutes after power-up of a “cold” instrument, when using the internal reference. This time is required for the 10 MHz reference to reach operating temperature and frequency. If the internal reference is unlocked, the “INT-UNLK” message is displayed on the Normal readout, but no error message is displayed.

The following procedure should isolate the failure to either the Reference Oscillator, the 3rd Converter, the Reference Lock module, or the reference switching circuitry.

Troubleshooting Procedure

1. Check to see if the error occurs when using the internal reference, the external reference, or either reference. If there is no external reference available, the following procedure can be used to check external reference input.

Set the FREQUENCY to 0.00 kHz, FREQ SPAN/DIV to 500 Hz, REF LEVEL to -30 dBm, MIN RF ATTENUATION to 0 dB, RESOLUTION BANDWIDTH to 1 KHz, TIME/DIV to 0.5 s, and Triggering to FREE RUN.

Connect the 10 MHz IF output to the EXT REF INput connector. As the instrument sweeps, the IF frequency will move through the external reference lock range. The REFERENCE OSCILLATOR readout should change to EXT for part of the sweep. The “FREQUENCY REFERENCE UNLOCKED” error message will appear during part of the sweep.

- a. If the REFERENCE OSCILLATOR readout does not change to EXT when the external input is used, check that the input external reference signal meets the input frequency and amplitude specifications. If it does, the external input buffer is malfunctioning. **(E)**
 - b. If the error message appears only when the external reference input is used, check to see that the external reference signal meets the input frequency and amplitude specifications. If it does, failure of the internal/external signal multiplexing is indicated. **(E)**
 - c. If the error message is present only when the internal reference is used (after the proper warmup time has been met), measure the output signal at P260 of the 10 MHz frequency standard.
 - 1) If the 10 MHz output signal is absent, measure the voltage at pin 2 of P1026. If this voltage is +2.0 V or more, failure of the frequency standard is indicated. **(E)**
 - 2) If this voltage is below +2.0 V, disconnect P1026 from the Mother board.
 - a) If the voltage remains low, failure of the internal reference shutdown circuit is indicated. **(E)**
 - b) If the voltage rises to above 2.0 V, failure of the frequency standard is indicated. **(E)**
 - 3) If there is a 10 MHz signal, check that it meets the frequency and amplitude specifications for the internal reference.
 - a) If signal characteristics meet the specifications, failure of the Reference Lock Module is indicated. **(E)**
 - b) If the signal does not meet specifications, failure of the frequency standard is indicated. **(E)**
2. Measure the frequency of the 100 MHz calibrator signal at the CAL OUT connector.
 - a. If the calibrator frequency is off more than 1.5 kHz from 100 MHz, failure of the 100 MHz voltage-controlled crystal oscillator is indicated. **(E)**
 - b. If the frequency is within 1.5 KHz of 100 MHz, measure the oscillator tuning voltage on Pin 1 of P1017. The normal voltage range is 0 to +12 V. With the loop unlocked, the voltage should be at or slightly beyond one of the limits.
 - 1) If the tuning voltage and the calibrator frequency are on the same side of the centers of their respective ranges (6 V and 100 MHz), C1038, in the VCO circuit, may be misadjusted. If this adjustment does not correct the problem it is not in the VCO by somewhere else in the loop. **(E)**
 - 2) If the tuning voltage and the calibrator frequency are on opposite sides of the centers of their respective ranges (6 V and 100 MHz), failure of the VCO is indicated. **(E)**

"TUNING FAILURE — 1ST LO"

The 1st LO is set by a combination hardware/software loop. There are two distinct hardware blocks to the loop: the block that measures the oscillator frequency and the block that sets the oscillator to frequency. The microprocessor system "closes the loop" by determining how far the oscillator must be moved to bring it to the desired frequency. Setting is an iterative process wherein the microprocessor indirectly counts the 1st LO, moves it as needed, and counts again. The 1st LO Tuning Failure error message is displayed when the 1st LO has not been set correctly after a number of iterations which varies with instrument settings.

The 1st LO Control Diagnostic Aid displays data on the crt screen which can be used to determine which part of the loop has failed. A typical display is shown below.

1ST LO CONTROL DIAGNOSTIC AID		
	<u>NOMINAL</u>	<u>DAC SET</u>
TUNE VOLTS	-6.79 V	-6.80 V
SENSE VOLTS	3.43 V	3.43 V
	<u>DESIRED</u>	<u>COUNTED</u>
1ST LO FREQ	2.720 504 GHZ	2.719 735 GHZ
MIXER FREQ	45.896 MHZ	46.665 MHZ
1ST LO SETTING ACCURACY		4.981 MHZ
AUXILIARY SYNTHESIZER		212.800 MHZ
PRESS "SHIFT" TO EXIT		

The first two lines list the voltage to be expected at the output of the 1st LO section of the Center Frequency Control and the voltage across the sense resistor of the 1st LO Driver. The nominal values are based on the Desired 1st LO Freq and the nominal tuning sensitivity of the oscillator. The DAC Set values are based on the setting of the 1st LO tuning DAC's. The DAC Set values can differ from the Nominal values because the system cannot be exactly calibrated, the tuning sensitivity of the oscillator is possibly not its nominal value, and the DAC's will be moved in an attempt to set the oscillator.

The Desired 1st LO Freq is the frequency to which the processor is trying to move the oscillator. The Counted 1st LO Freq is the frequency the microcomputer has calculated from, the internally counted harmonic mixer output frequency, the Auxiliary Synthesizer frequency, and the assumed harmonic number of the Auxiliary Synthesizer. Because of this last assumption, if the 1st LO is not near the Desired Frequency, the Counted Frequency will not be the actual oscillator frequency, even though the counter is functioning.

The Desired Mixer Freq is the difference between the the Desired 1st LO Freq and the nearest harmonic of the Auxiliary Synthesizer. (The Auxiliary Synthesizer harmonic will always be higher in frequency than the desired 1st LO frequency.)

The 1st LO Setting Accuracy is the maximum permitted difference between the actual and desired LO frequencies. The setting process will end when the difference becomes less than, or equal to, this value. The tolerance depends on frequency span and band.

The Auxiliary Synthesizer Freq is the frequency that is programmed into the $\pm N$ synthesizer.

This troubleshooting procedure should localize a problem to the oscillator, the oscillator setting block, or the oscillator counting block. If the failure is not in the oscillator, it is further localized within one of the hardware blocks.

Troubleshooting Procedure

1. Press <SHIFT> EXT to display the Diagnostic Aids menu, then select "1" to display the 1st LO Control Diagnostic Aid information. (If the error message "UNDEFINED FUNCTION" appears after the first step, check that #3 switch of S1038 (Options), on the Memory Board, is in the "open" position.)
2. If the Counted 1st LO Freq is within the 1st LO Setting Accuracy of the Desired Freq readout, press <SHIFT> to return to normal operation. Now determine if the error occurs, for the same center frequency, at frequency spans/division above 5 MHz only, or at spans less than 5 MHz/div. (Frequency range must be 0-1.8 GHz or 1.7-5.5 GHz.)
 - a. If the frequency control error occurs only at frequency spans of 5 MHz/div or more, the capacitor switching relay, on the 1st LO assembly, is probably shorted. **(E)**
 - b. If the error occurs with a frequency span/div of 5 MHz or less, the 1st LO is probably defective. **(E)**
3. Measure the voltage across the sense resistor (R1040) on the 1st LO Driver board. If this voltage is within 50 mV of the DAC Set value, measure the frequency on the 1ST LO Output connector. This measured frequency should be within 50 MHz of the frequency calculated by multiplying 800 MHz/V by the voltage that was measured across the sense resistor R1040.
 - a. If the calculated and measured frequencies are within 50 MHz of each other and the measured frequency agrees with the internally Counted 1st LO Freq readout or differs from it by a multiple of the Auxiliary Synthesizer Freq, return to normal operation (by pressing <SHIFT>). Now attempt to calibrate the CF Control board and the 1st LO Driver board by pressing <SHIFT> PULSE STRETCHER and select "1", for the CF Control board, or "2", for the 1st LO Driver board, from the menu. Exit from the CF Control board calibration routine by pressing <SHIFT> when the step for R4040 is displayed. If you are able to complete the calibration routine, check to see if the error message is still present. If it is, or if the calibration routines cannot be completed, continue troubleshooting with step 3c. **(E)**
 - b. If the calculated and measured frequencies are within 50 MHz, but do not meet the conditions in step 3a, measure the Auxiliary Synthesizer output frequency at P1060 on the Auxiliary Synthesizer board.
 - 1) If the Auxiliary Synthesizer output frequency is correct, measure the input frequency from the Harmonic Mixer with a spectrum analyzer, at the cable connection to P261 on the Auxiliary Synthesizer board. (A counter would probably give an erroneous reading because of the harmonic mixing process). The frequency measured with the spectrum analyzer should equal the Desired Mixer Freq + (the measured 1st LO frequency—the Desired 1st LO Freq) if the calculated frequency is between 10 MHz and 90 MHz. If the calculated frequency is outside the 10 MHz to 90 MHz range, the 1st LO frequency is far from the desired value. Repeat the previous steps in this procedure.
 - a) If the Harmonic Mixer output frequency is correct, measure the frequency at edge connector 15, on the Auxiliary Synthesizer board, with a counter. This should be 1/100 of the Harmonic Mixer output frequency.
 - (1) A correct frequency measurement indicates the Counter board is defective. **(E)**

- (2) An incorrect frequency measurement indicates the Auxiliary Synthesizer is defective. **(E)**
- b) The Harmonic Mixer is probably defective if no signal is present at the output or the signal frequency is incorrect. **(E)**
- 2) If the output frequency, at P1060 is incorrect, measure the tune voltage for the 200–220 MHz VCO, between TP1066 and TP1074 on the Auxiliary Synthesizer board. The range of the tuning voltage is normally +5 V to +12 V.
- a) If the tune voltage is within the center of its normal range and the output frequency at P1060 is stable (varies no more than 1–2 Hz), the programmable divider in the phase-locked loop is probably defective. **(E)**
- b) If the tune voltage is in the center portion of its normal range and the output frequency at P1061 is unstable, the loop amplifier is probably defective. **(E)**
- c) If the tune voltage and oscillator frequency are at the end or outside their range, in the same direction (high or low), C1070 in the VCO may be misadjusted. If adjustment of the capacitor does not correct the problem it is not in the VCO but somewhere else in the loop. **(E)**
- d) If the tuning voltage and the Auxiliary Synthesizer frequency are in opposite directions from the center of their respective ranges (8.5 V and 210 MHz), the VCO is probably defective. **(E)**
- e) If the calculated and measured frequencies differ by more than 50 MHz, remove the jumper plug P3043 on the 1st LO Driver board and measure the oscillator current.



The oscillator coil has significant inductance. Interrupting the oscillator current will generate high voltage. Remove/replace P3043 or connect/disconnect a current meter after the power is off. (Typical voltages at P3043 can range as high as 35 V.)

The coil current should be: 40 mA/V^1 (V^1 is the sense resistor voltage, as previously measured across R1040). The measured current should be within 1% of this value.

- 1) If the measured and calculated currents are within 1%, return to normal operation (by pressing <SHIFT>) and determine if the frequency control error occurs with frequency span/div of 5 MHz or less, or above 5 MHz/div, with the same center frequency. (The frequency range should be in either band 1 (0–1.8 GHz) or band 2 (1.7–5.5 GHz).
- a) If the frequency control error occurs only with frequency spans of 5 MHz/div or less, one of the noise filter capacitors on the 1st LO Assembly is probably defective. **(E)**
- b) If the error occurs with frequency spans greater than 5 MHz/div, the 1st LO is probably defective. **(E)**
- 2) If the measured and calculated currents are not equal, the problem is likely in the final stage of the LO Driver. **(E)**

4. Measure the 1st LO tuning voltage at edge connector 47, of the Center Frequency Control board. This voltage should be within 200 mV of the listed DAC Set value.
 - a. If the voltage is within this limit, failure of the 1st LO Driver board is indicated. **(E)**
 - b. If the voltage is not within the limit, failure of the Center Frequency Control board is indicated. **(E)**

“TUNING FAILURE — 2ND LO”

The 2nd LO is set by a combination hardware/software loop. There are two distinct hardware blocks in the loop; the block which measures the oscillator frequency and the block which sets the oscillator to frequency. The microprocessor “closes the loop” by determining how far the oscillator must be moved to bring it to the desired frequency. Setting is an iterative process wherein the microprocessor counts the oscillator frequency, moves it as needed, and counts again. The error message is displayed if the 2nd LO is not set to the desired frequency after a number of iterations, depending on instrument settings.

The 2nd LO Control Diagnostic Aid displays data which can be used to determine which part of the loop has failed. A typical display is shown below. (Ensure that the #3 switch of the Options switch, on the Memory board, is in the open position.) Press <SHIFT> EXT and select 2nd LO Control (#2) from the menu.

<u>2ND LO CONTROL DIAGNOSTIC AID</u>		
	<u>NOMINAL</u>	<u>DAC SET</u>
TUNE VOLTS	0.01 V	0.19 V
	<u>DESIRED</u>	<u>COUNTED</u>
2ND LO FREQ	2.182 000 GHZ	2.182 140 GHZ
OFFSET FREQ	18.000 000 MHZ	17.860 MHZ
OFFSET SETTING ACCURACY		540.672 KHZ
PRESS “SHIFT” TO EXIT		

The Tune Volts is the voltage that would be expected at the output of the 2nd LO section of the Center Frequency Control. The Nominal voltage is the value needed for the Desired frequency of the oscillator in a perfectly calibrated system. The DAC Set voltage should be produced by the present setting of the 2nd LO tuning DAC's. The DAC Set voltage may differ from the Nominal value because the system may not be fully calibrated and the DAC's will be moved to try to set the oscillator.

The Desired 2nd LO Freq is the frequency to which the microcomputer is trying to move the oscillator. The Counted 2nd LO Freq is that frequency the microcomputer has calculated from the Counted Offset Freq.

The Offset Freq is the frequency of the low-frequency offset VCO in the 2nd LO Assembly. In the 2182 MHz LO, this frequency is the difference between 2200 MHz and the LO frequency. (The 719 MHz LO is derived from the 2182 MHz LO, and the frequency relationships are more complex.) Again, the Desired Freq is the frequency the microcomputer is trying to set the offset, and the Counted Freq is the value read by the internal counter.

The Offset Setting Accuracy is the maximum permitted difference between the actual and desired offset frequencies. The setting process ends when the difference becomes less than or equal to this value. The tolerance depends on frequency span and band.

The following procedure should localize the failure to the 2nd LO assembly, the hardware setting block, or the hardware counting block.

Troubleshooting Procedure

1. Display the diagnostic information for the 2nd LO control loop as outlined above.
2. If the Counted Offset Freq and the Desired Offset Freq are within the Offset Setting Accuracy, the 2nd LO probably has failed.
3. If the Counted Offset Freq is within 100 kHz of the Desired Offset Freq, make sure that P1048 is properly seated on J1048. If the fine tune ground lead is not making good contact, the tuning voltage can shift sufficiently to cause setting failures. **(E)**
4. If the Counted Offset Freq readout is within 100 kHz of the Desired Offset Freq, the oscillator may be out of calibration. Return to normal operation by pressing <SHIFT>. Try to calibrate the 2nd LO by pressing <SHIFT> PULSE STRETCHER and select "4" (2nd LO) from the menu. Now, follow the instructions of the displayed messages. If you are able to complete the calibration routine, check to see if the error condition still exists. If the error is still there, or you were unable to complete the calibration routine, proceed to the next step. **(E)**
5. Measure the 2nd LO Tune Volts at TP1044 on the Center Frequency Control board.
 - a. If the 2nd LO tuning voltage is within 200 mV of the DAC Set value, measure the 2nd LO frequency at the front-panel 2ND LO Output connector.
 - 1) If the measured frequency does not agree with the internally Counted readout, the Counter board is probably at fault. **(E)**
 - 2) If the frequency agrees with the Counted value, measure the mixed down frequency at the cable going to P513 on the Counter board. This frequency should equal: Desired Offset Freq + (Desired 2nd LO Freq — the measured 2nd LO frequency)
 - a) If this frequency is present, measure the 2182 MHz oscillator tuning voltage on the feedthrough capacitor C2203 between the 16–20 MHz Phase Lock circuit and the 2182 MHz Microstrip Oscillator in the 2182 MHz Phase Locked 2nd LO Assembly. The normal range of this voltage is 0 V to –12.5 V. With the phase locked loop unlocked, this voltage will probably be slightly outside one end of the range.
 - (1) If the absolute value (magnitude) of the tuning voltage and the oscillator frequency are off in the same direction from the centers of their respective ranges [6 (–6) V and 2182 MHz], the Microstrip Oscillator has probably failed. **(E)**
 - (2) If the absolute value (magnitude) of the tuning voltage and the oscillator frequency are off in the opposite direction from the center or their respective ranges [6 (–6) V and 2182 MHz], some other part of the lock loop, besides the Microstrip Oscillator, has probably failed. **(E)**

- b) If the mixed-down frequency is absent, either the 2200 MHz Reference, the 2182 MHz Microstrip Oscillator or the 2200 MHz Reference Mixer probably has failed. **(E)**

- b. If the tuning voltage is not within 200 mV of the DAC Set value, the Center Frequency Control board probably has failed. **(E)**

“COUNT NOT ACCURATE”

This error message is displayed when the internal counter is not receiving the proper signal from the 10 MHz IF. The 3rd IF Counter Diagnostic Aid lists troubleshooting information on the crt. The following is a typical display of this diagnostic aid.

<u>3RD IF COUNTER DIAGNOSTIC AID</u>		
	<u>NOMINAL</u>	<u>COUNTED</u>
3RD IF FREQ	10.000 000 MHZ	10.000 448 MHZ
PRESS "SHIFT" TO EXIT		

The Nominal 3rd IF Freq is the frequency to be expected at the IF output to the counter when counting a center-screen signal. The Counted 3rd IF Freq is the frequency measured by the 494/494P counter.

This procedure should help isolate the failure to the Log Amplifier or the Counter board.

Troubleshooting Procedure

1. Set the amplitude of a stable signal, such as the calibrator signal, at the top graticule line (full screen) at center screen.

2. Display the diagnostic information for the IF counter by pressing <SHIFT> HELP and select #3 to display the 3rd IF Counter Aid information. (If an error message "UNDEFINED FUNCTION" appears after the 1st step, check the setting of switch #3 of the Options swith S1038, on the Memory board. It must be in the "open" position.)

3. Measure the signal at P622 of the Log and Video Amplifier board. With a full screen signal, this signal level should be -43 dBm.
 - a. If there is not a signal or its amplitude is less than -50 dBm, it indicates a problem in the Log and Video Amplifier board. **(E)**

- b. If the proper signal is present, it indicates the problem is in the Counter board. (E)

“PHASELOCK FAILURE — 1ST LO”

The following procedure assumes that the oscillator is at the correct frequency, so the problem must be in the phase lock system.

The 1st LO Phase Lock Diagnostic Aid crt display shown below displays data for troubleshooting the 1st LO phase lock loop.



While the troubleshooting information is displayed, the 1st LO is repetitively being stepped ± 750 KHz. If “LOCK DISABLED” is displayed, the lock loop is open between the output of the phase gate and the input to the FM coil. If lock is enabled, the loop is closed, and the fourth line of the display changes to “LOCK ENABLED PRESS “HELP” TO DISABLE”.

The 1st LO Freq readout is the frequency the oscillator should be at when locked. The frequency that is measured at the front-panel 1ST LO Out connector will not check exactly with this value because the oscillator is unlocked and stepping in frequency.

The Strobe Freq is the frequency at P502 and P504 of the Phase Lock module.

This procedure should help localize the failure to the Phase Gate or to a section of the phase lock circuitry.

Troubleshooting Procedure

Before troubleshooting data on the phase lock loop is displayed, the Freq Span/Div must be in those spans that enable the phase lock mode (200 kHz or less for band 1).

1. Press <SHIFT> EXT then select “0”, from the diagnostic aids menu, to display the “1st LO Phase Lock Diagnostic Aid” information. (If an error message “UNDEFINED FUNCTION” appears after the 1st step, it indicates switch #3 of S1038 (Options) on the Memory board is not in its “open” position.)

2. With an oscilloscope, examine the signal at P242 on the Phase Gate. Beat notes (bursts of signal at up to 500 kHz) at a 10 Hz rate should be present as the oscillator is stepped. Beat note amplitude should be about 6 V peak-to-peak. The amplitude of the positive and negative peaks should not differ by more than 20%.
 - a. If beat notes are present, press HELP to enable the lock. Check the Error Amplifier output at TP2037, on the Error Amplifier board in the Phase Lock module. Output signal amplitude should be approximately 6 V peak-to-peak and its frequency should be 10 Hz. The up and down out-of-range signals, on edge connectors 8 and 10 of the Error Amplifier board, should be toggling between 0 V and +5 V.
 - 1) If there is a signal at TP2037 but one or both of the out-of-range lines is not toggling, the out-of-range comparator on the Error Amplifier board, or the sensing circuit on the Phase Lock Control board, has probably failed. This could cause problems in maintaining lock but not in acquiring lock. If the instrument does not acquire lock, note the out-of-range problem and continue troubleshooting with step 3).
 - 2) If there is no signal at TP2037, the Error Amplifier has probably failed. **(E)**
 - 3) If there is a signal at TP2037, the switching circuit that connects the output of the Error Amplifier to the FM coil of the 1st LO has probably failed. **(E)**
 - b. If beat notes are present, but their amplitude is less than 3.8 V (peak-to-peak), or the amplitude difference of the positive and negative excursions is more than 20%, the Phase Gate is probably defective. **(E)**
 - c. If there are no beat notes, measure the strobe frequency, at P504 on the Phase Lock module.
 - 1) If the strobe frequency is the same as the readout on the diagnostic aid display, it is possible, but not probable, that the 1st LO system is miscalibrated and that the 1st LO is near the wrong harmonic of the Auxiliary Synthesizer. Press <SHIFT> to return to normal operation and look at the calibrator line that is closest in frequency to the frequency (in Band 1) at which the error occurs. If the frequency indicated for the calibrator line is correct (a multiple of 100 MHz), the Phase Gate has probably failed.

If the frequency indicated is incorrect, attempt to calibrate the 1st LO system by pressing <SHIFT> PULSE STRETCHER and select 0 (Overall System Cal) from the menu. Exit from the calibration routine when the display for R4040, on the CF Control board appears by pressing <SHIFT>. If the calibration can not be completed, or it does not result in the correct frequency indication for the calibrator line, troubleshoot the 1st LO system using the procedure under "TUNING FAILURE — 1st LO" error message step 3b. **(E)**

- 2) If there is no strobe signal, check for a signal on feedthrough "M", on the Strobe Driver board in the Phase Lock module.
 - a) If there is a signal, the Strobe Driver has probably failed. **(E)**
 - b) If there is no signal, the Controlled Oscillator has probably failed. **(E)**
- 3) If the frequency of the strobe signal is erroneous, but is stable (within 1-2 Hz), in the normal strobe range of 5.006477 MHz to 5.018868 MHz, the programmable divider in the Synthesizer has probably failed. **(E)**

- 4) If the listed Strobe Freq is below 5.007 100 MHz and the actual strobe frequency is slightly above the desired frequency, or above 5.018 240 MHz and the actual strobe frequency is slightly below the desired frequency, attempt to calibrate the Phase Lock Synthesizer. Press <SHIFT>, to return to normal operation, then press <SHIFT> PULSE STRETCHER and select "5" from the menu. If you are able to complete the calibration, check to see if the error message is still present. If it is still displayed, or the calibration routine could not be completed, proceed to the next step as if the strobe frequency was not within the above range. **(E)**
- 5) If the listed Strobe Freq is outside the range in the preceding step, measure the tune voltage for the VCO, at feedthrough "H" on the Controlled Oscillator board in the Phase Lock module. The normal range is from 5.9 V to 11.3 V. With the loop unlocked, the voltage will probably be near or beyond one end of the range.
 - a) If the voltage is around the center of the range, the loop filter and amplifier, on the Error Amplifier board, are probably at fault. **(E)**
 - b) If the tuning voltage and the strobe frequency are displaced from the center of their range (8.6 V and 5.013 MHz) in the same direction, the VCO is good and something else within the loop has failed. **(E)**
 - c) If the tuning voltage and the strobe frequency are displaced in opposite directions from the center of their range, the VCO has probably failed. **(E)**

494/494P TRACE MODES

Trace Mode provides information on how the frequency control system is working. It is accessed by pressing <SHIFT> GRAT ILLUM then select either "0", "1", "2", "3", or "4", from the menu.

The sequence <SHIFT> GRAT ILLUM "1", starts tracing the 1st LO control actions. The sequence <SHIFT> GRAT ILLUM "2", starts tracing the 2nd LO control actions. The sequence <SHIFT> GRAT ILLUM "3", starts tracing signal counts. Information from these three trace modes is stored in RAM and can be displayed by pressing <SHIFT> GRAT ILLUM "4". This mode displays up to 16 lines of data gathered by the trace modes.

The first field of the display indicates which mode was active at the time the information was gathered. For modes 1 and 2 (1st LO Control and 2nd LO Control), the second field of the display indicates which attempt at tuning or correcting the oscillator the data is for. The next field contains the tuning DAC settings before a tune or correction took place. The first three digits are the upper DAC settings, the next three digits the lower DAC settings. The next field contains the DAC settings after the tuning or correction was attempted. Again, the first three digits are the upper DAC, and the next three digits the lower DAC settings. The next field indicates the time delay between setting the DACs to the new values and reading the resulting frequency, in units of millisecond. The final field contains the frequency of the oscillator in question, after the tune or correction attempt. Actually, the displayed frequency is the beat note frequency from the auxiliary mixer for the 1st LO (in KHz), and the 16-20 MHz oscillator frequency for the 2nd LO.

The second field for the signal count mode (3rd mode) indicates the frequency of the 2nd LO (which is the frequency of the 16-20 MHz oscillator). The next field shows the frequency of the 10 MHz IF, and the last field the frequency of the 1st LO.

The sequence <SHIFT> GRAT ILLUM "0", terminates trace actions and erases the RAM of all data.

Alternate Frequency Display

The Alternate Frequency Display mode selects an alternate frequency display instead of the normal Center Frequency display. These alternate frequencies are selected with the key sequence <SHIFT> READOUT followed by "0", "1", "2", or "3" as indicated by the menu.

The normal Center Frequency is displayed with the sequence <SHIFT> READOUT "0".

The frequency of the 1st LO is displayed with the sequence <SHIFT> READOUT "1". This display is updated each time the 1st LO frequency is counted.

The frequency of the 2nd LO is displayed by pressing <SHIFT> READOUT "2". This display is updated each time the frequency of the 2nd LO is counted.

The frequency of the 10 MHz IF is displayed after the sequence <SHIFT> READOUT "3", has been entered. This display is updated each time the IF is counted, which is at the end of each sweep while trace mode is on.

Auxiliary Synthesizer Control

The Auxiliary Synthesizer Control can be turned on continuously, or turned on only during correction for the 1st LO tunes. This mode is toggled (turned on continuously or during 1st LO corrections) by pressing <SHIFT> LINE. A message will come on screen indicating which mode the Auxiliary Synthesizer is in.

Correction Disable/Enable

Correction of the 1st and 2nd LO frequencies can be disabled or enabled by pressing <SHIFT> INT. When corrections are disabled, the oscillator frequencies are counted but no further action is taken. This mode can be used to monitor the drift of the oscillators by activating the respective trace mode. When corrections are disabled, the 1st LO cannot be phase locked!

Synthesis Disable/Enable

Synthesis of the LO frequencies can be disabled or enabled by pressing <SHIFT> FREE RUN. When synthesis is disabled, the local oscillators can be tuned however their frequencies are not counted. When synthesis is disabled, the 1st LO cannot be phase locked!

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CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and instrument repair. Special techniques and procedures that may be required to remove and replace assemblies and/or components in this instrument are described here.

Handling Static Sensitive Components

Most semiconductor types, both separately and in assemblies, are susceptible to damage to static charge, see Table 6-1 for voltage levels. We recommend static sensitive procedures be implemented for all operations involving semiconductor handling.

Obtaining Replacement Parts

All electrical and mechanical parts are available through your local Tektronix Field Office or representative. The Replaceable Parts list section contains information on how to order these replacement parts.

NOTE

Some components that are heat sinked to the circuit board extrusion or module wall, are soldered to the board after the board is mounted in place. This is necessary to avoid cracking the IC case when the mounting screw is tightened. These components are identified by a note on the schematic drawing. Their part number appears with chassis mounted components in the Replaceable Electrical Parts list.

Parts orientation and lead dress should be duplicated because some components are oriented so as to reduce interaction between circuits or to control circuit characteristics.

Any component that has been replaced with a different or improved part will be substituted when you order a replacement. If the change is complex, your local Field Office or representative will contact you concerning the change. After repair, the circuits may need recalibration.

Parts Repair and Return Program

Assemblies containing hybrid circuits or substrates in a semi-sealed module, and complex assemblies such as the YIG oscillator, 829 MHz converter, or phase gate detector, can be returned to Tektronix for repair under the repair and return program.

Tektronix repair centers provide replacement or repair service on major assemblies as well as the unit. Return the instrument or assembly to your local Field Office for this service, or contact your local Field Office for repair and exchange rates.

Firmware Version and Error Message Readout

This feature of the 494/494P provides readout of the firmware version when the power on/off is cycled. During the initial power-up cycle, the instrument firmware and front panel firmware versions flashes on screen for approximately two seconds. The Replaceable Electrical Parts list section, under Memory board (A54), lists the ROM's and their Tektronix part number for each firmware version.

Whenever an error occurs in an operational routine, an error message on screen describes the nature of the error. Messages are also displayed, when running a calibration procedure or diagnostic test, that inform the user as to the status of the instrument or guide the user through an adjustment procedure (see Diagnostics part of this section).

Selected Components

Components that are selected to meet Tektronix specifications, carry only Tektronix part numbers in the Replaceable Parts list. In some cases the value of a component is to compensate for parameter differences between active components. These are identified as selectable on the circuit diagram and in the Replaceable Electrical Parts list. The Replaceable Parts list description for the component gives either a nominal value or range of value. If the procedure for selection is not obvious, such as setting the gain or response of a stage, the procedure for selection is explained in the adjustment part of recalibration procedure.

Replacing EPROM's or ROM's

Firmware for the microcomputer is contained in ROM's on the Memory and GPIB boards. Refer to the Replaceable Electrical Parts list (Vol. 2) under these assemblies (A54 Memory and A56 GPIB) for the versions and IC part numbers. Most IC's are soldered into sockets on the board to reduce problems that occur due to poor contact because of corrosion or loose pins. Refer to replacing Transistor and Integrated Circuit (IC's) for procedure.

Transistor and Integrated Circuit Electrode Configuration

Lead identification for transistors, MOS FET's, and IC's, is shown in Figure 6-1. IC pin-outs for Vcc and ground are shown either with a table or box on the schematic diagram. Refer to Soldering Technique in Corrective Maintenance part for unsoldering and soldering instructions. The socket for the IC has a square or rectangular socket for pin 1.

Diode Color Code

The cathode of each glass encased diode is indicated by a stripe, a series of stripes, or a dot. Some diodes have a diode symbol printed on one side. Figure 6-2 illustrates diode types and polarity markings that are used in this instrument.

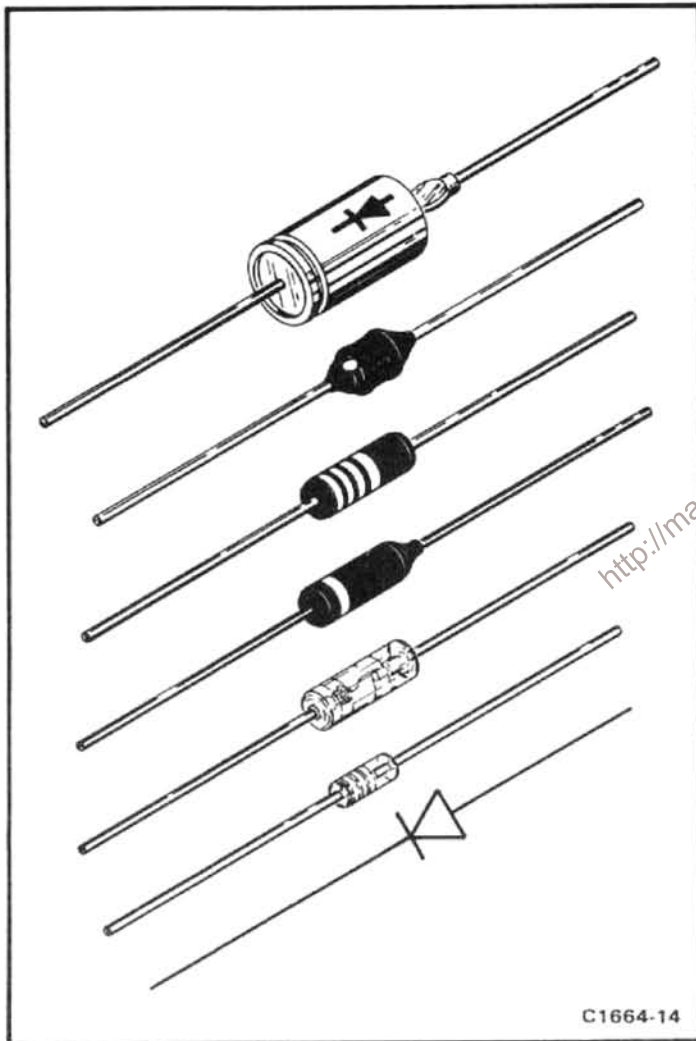


Figure 6-2. Diode polarity markings.

Multiple Terminal (Harmonica) Connectors

Some intercircuit connections are made through pin connectors that are mounted in a harmonica type holder. The terminals in the holder, are identified by numbers that ap-

pear on the holder and the circuit diagrams. Connectors are identified on the schematic and board with either the prefix letter " P" or "J" followed by a circuit number. Connector orientation to the circuit board is keyed by a triangle on the holder and the circuit board (see Figure 6-3). In some cases, the triangle or arrow is screened on the chassis adjacent to the connector. Some connectors contain more than one section.

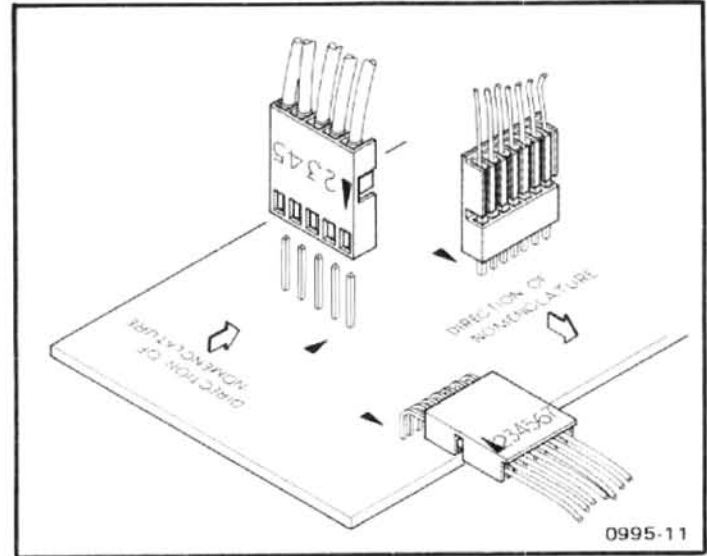


Figure 6-3. Multipin (harmonica) connector configuration.

Resistor Values

Many types of resistors (such as composition, metal film, tapped, thick film resistor network package, plate, etc.) are used in the 494/494P. The value is either color coded in accordance with the EIA color code, or printed on the body of the component.

Capacitor Marking

The capacitance value of ceramic disc, plate, and slug, or small electrolytic capacitors, is marked in microfarads on the side of the component body. The ceramic tubular capacitors and feedthrough capacitors are color coded in picofarads. Tantalum capacitors are color coded as shown in Figure 6-4.

Soldering Techniques



Disconnect the instrument from its power source before replacing or soldering components.

Some of the circuit boards in this instrument are multi-layer; therefore, extreme caution must be used when a sol-

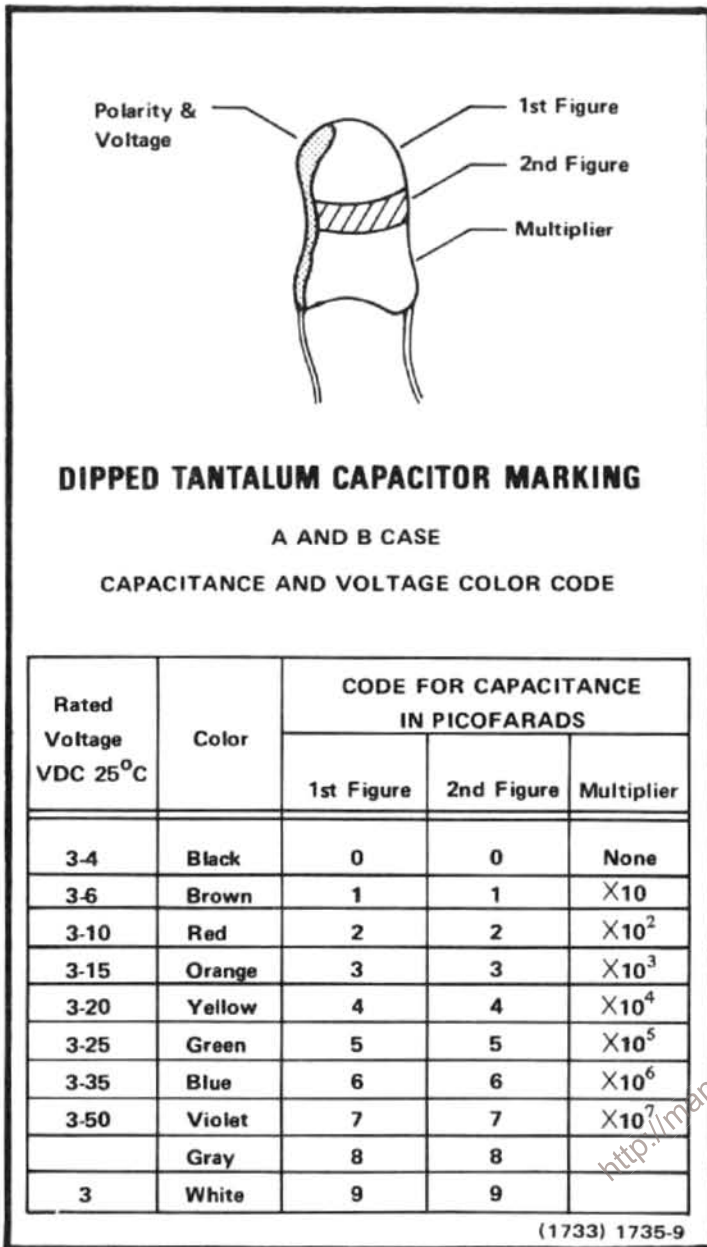


Figure 6-4. Color code for some tantalum capacitors.

dered component is removed or replaced. Excess heat from the soldering iron and bent component leads may pull the plating out of the hole. We suggest clipping the old component free. Leave enough lead length so the new component leads can be soldered in place. If you desire to remove the component leads, use a 15 W or less pencil type iron. Straighten the leads on the back side of the board; then when the solder melts, gently pull the soldered lead through the hole. A desoldering tool should be used to remove the old solder. Use a desoldering tool that has a low build-up of static charge, such as Silverstat Soldapullit desoldering tool, when unsoldering IC's or transistors from their sockets.

Replacing the Square Pin for the Multi-pin Connectors

It is important not to damage or disturb the ferrule when removing the old stub of a broken pin. The ferrule is pressed into the circuit board and provides a base for soldering the pin connector.

If the broken stub is long enough, grasp it with a pair of needle nose pliers, apply heat, with a small soldering iron, to the pin base of the ferrule and pull the old pin out. (The pin is pressed into the ferrule so a firm pull is required to pull it out.)

If the broken stub is too short to grasp with pliers, use a small dowel (0.028 inch in diameter) clamped in a vise to push the pin out of the ferrule after the solder has melted.

The old ferrule can be cleaned by reheating socket and placing a sharp object such as a toothpick or small dowel into the hole. A 0.031 inch drill mounted in a pin vise may also be used to ream the solder out of the old ferrule.

Use a pair of diagonal cutters to remove the ferrule from the new pin; then insert the pin into the old ferrule and solder the pin to both sides of the ferrule.

If it is necessary to bend the new pin, grasp the base of the pin with needle-nose pliers and bend against the pressure of the pliers to avoid breaking the board around the ferrule.

Servicing the VR Module

The VR module requires mechanical support when it is installed on board extenders. Mechanical support is provided by moving the mounting plate at the upper side of the module (Figure 6-5A) to the bottom side. This allows installation of a mounting screw through a support bracket into the mounting plate screw hole as shown in Figure 6-5B. For better support, we recommend using a second bracket on the other end. Remove the bracket, turn it over and install it so the threaded studs are below the module.

REPLACING ASSEMBLIES AND SUBASSEMBLIES

Most assemblies or sub-assemblies in this instrument are easily removed and replaced. The following describes

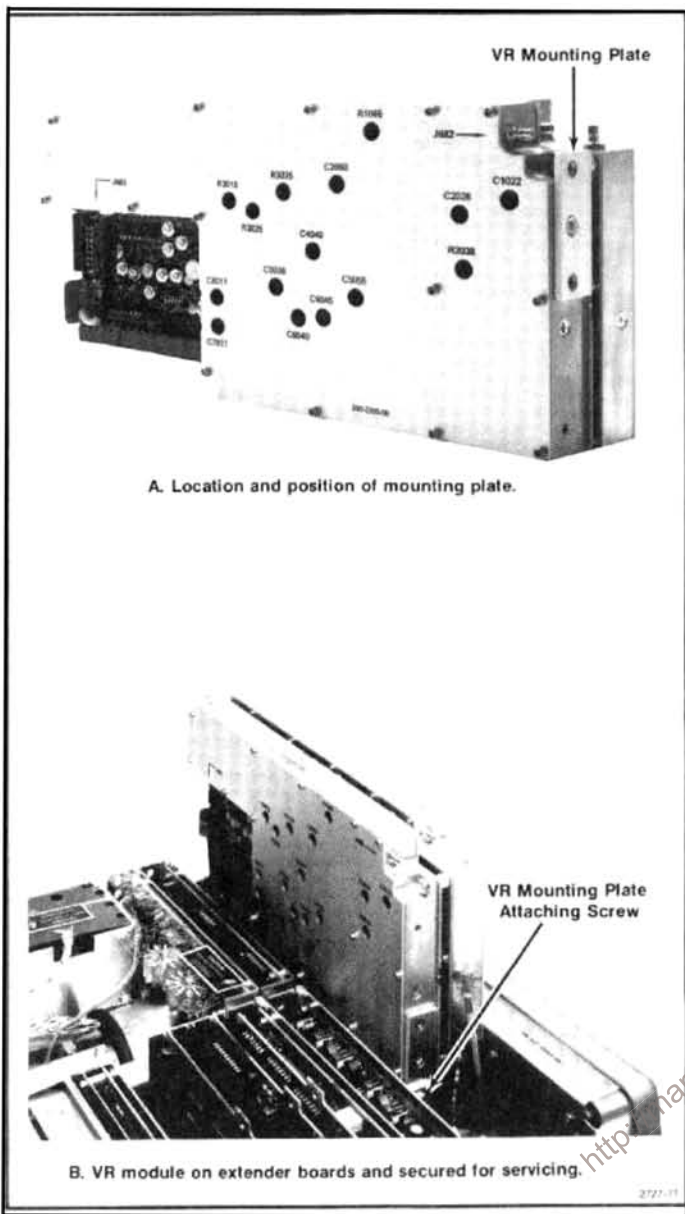


Figure 6-5. Preparing the VR assembly for servicing, showing how it is supported when on an extender board.

procedures for replacing those assemblies that require special attention. Top and bottom views of the 494/494P are shown in Figures 6-6 and 6-7. These illustrations show the location and identify most assemblies by their name and assembly number.

Removing and Installing the GPIB Board for the 494P Instrument

The GPIB board connects to the GPIB port on the back panel, through a GPIB Extender board (A56A1), a ribbon cable (W560), and a GPIB Interface board (A30A57) in the Power Supply module. The GPIB Extender board edge connector is clamped to the connector on the GPIB board by means of a locking key that extends through the connector. When the key is turned, so it faces inward, the connector is

clamped. To release the connector, so the GPIB board can be removed, proceed as follows:

1. Unscrew the mounting screws that hold the metal shield over the GPIB, Processor, and Digital Storage boards and remove the shield.

2. Lift the key to the GPIB Extender board connector up so it just clears the board and turn it 90°, so it faces the rear of the instrument. This will spread the connector so the GPIB board can now be pulled from the connector on the Mother board.

3. Use a board puller to pull the GPIB board free from the Mother board.

Install the board as follows:

1. With the key for the GPIB Extender board connector turned so the connector is spread (top of the key facing to the rear of the instrument), slide the GPIB board through the guides and onto the Mother board connector. Ensure that the board is well seated.

2. Turn the key 90° to lock the connectors of the GPIB Extender board and the GPIB board together. Push the key down to its rest position.

3. Re-install the shield over the GPIB, Processor, and Digital Storage boards.

NOTE

If the version number message "0" keeps coming up on the crt, or if the instrument does not respond to a change in address with the GPIB ADDRESS switches, it indicates that the GPIB board is not seated properly onto the Mother board connector, or that the GPIB and GPIB Extender connectors are not making contact.

Removing or Replacing Semi-rigid Coaxial Cables

Performance of the instrument is easily degraded if these connectors are loose, dirty, or damaged. The following procedure will help ensure that the connection is good enough to maintain proper performance.

1. Use a 5/16 inch open-end wrench to loosen or tighten the connectors. It is good practice to use a second wrench to hold the rigid (receptacle) portion of the connector to prevent bending or twisting the cable.

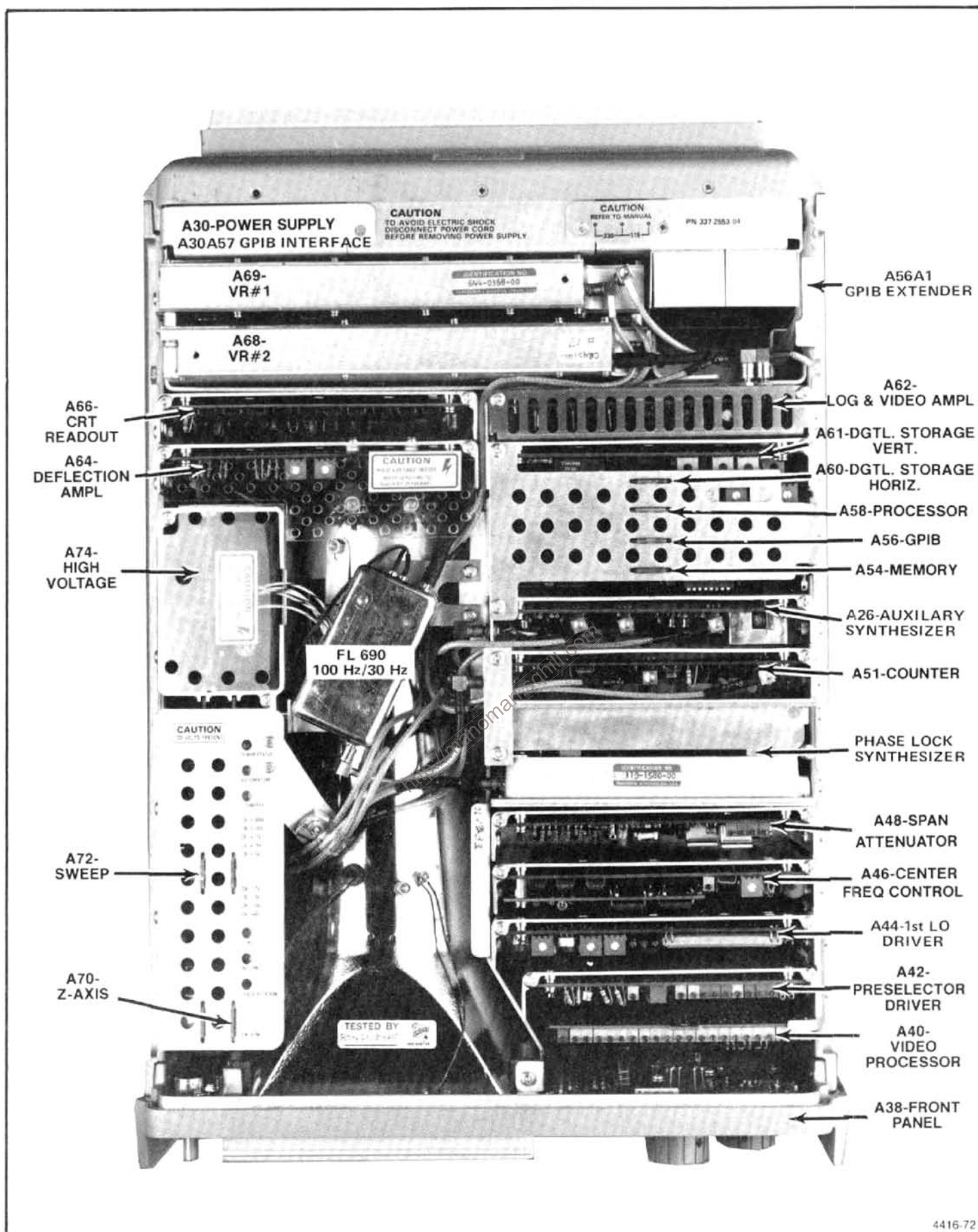


Figure 6-6. Top deck of the 494/494P identifying major assemblies or circuit boards.

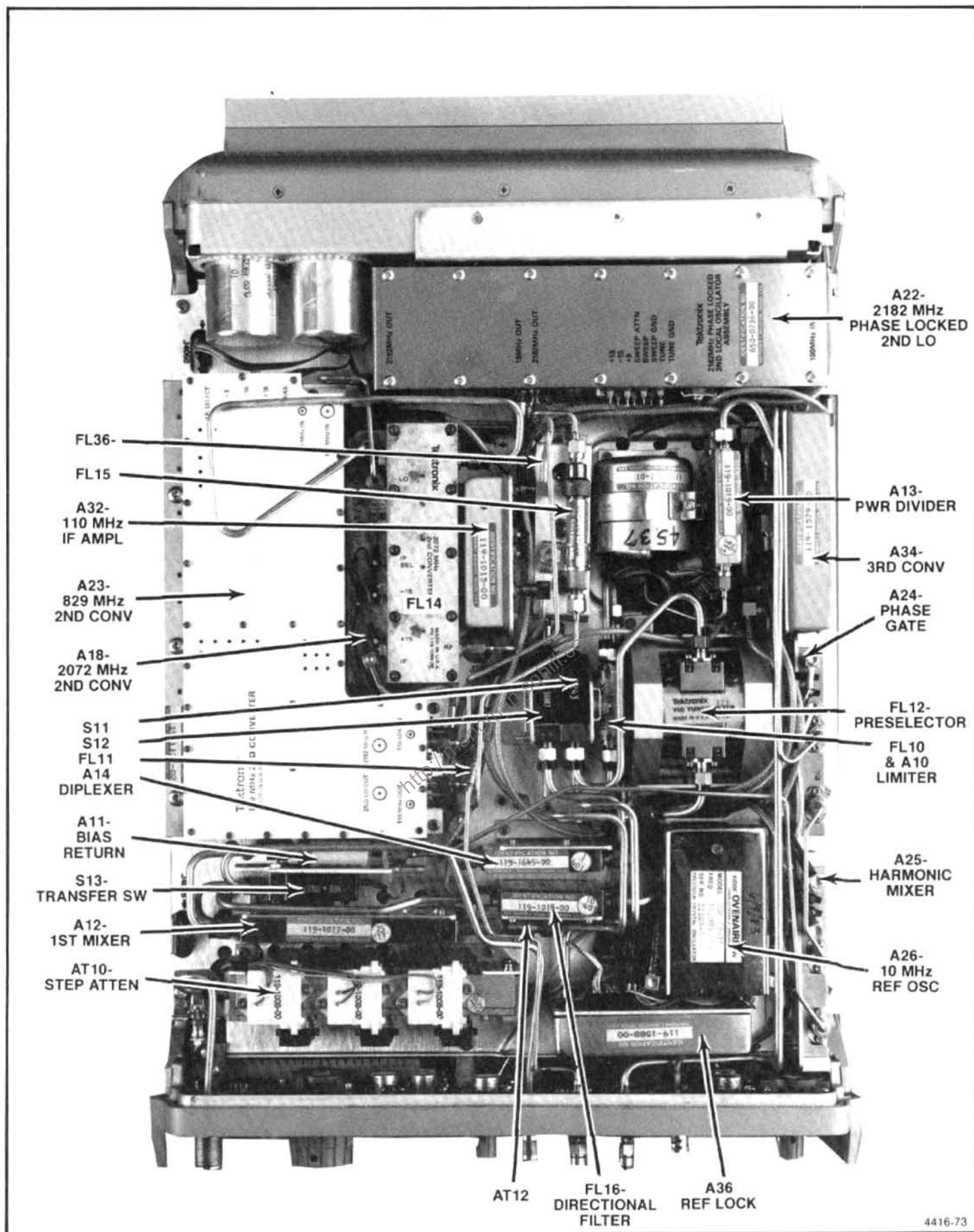


Figure 6-7. RF deck of the 494/494P identifying major assemblies.

2. Ensure that the plug and receptacle are clean and free of any foreign matter.

3. Insert the plug connector fully into the receptacle before screwing the nut on. Tighten the connection to 8 inch pounds to ensure that the connection is tight. Do not overtighten (15 to 20 inch pounds) because this can damage the connector.

Replacing the Crt

Removal

1. Remove the snap-in printed bezel and crt light filter.

2. Use an 8/64 inch Allen wrench to remove the four bezel screws, unplug and remove the inner bezel.

3. Unsolder the ground wire from the front panel casting and unplug the crt cables at their respective board connections (High Voltage module, Deflection Amplifier board, and Z-Axis board).

4. Slide the crt, with its shield, out through the front panel.

5. Remove the crt shield as follows:

- a. remove the tube base cap and unplug the socket;
- b. remove the two side screws that hold the upper shield in place, then remove the shield;
- c. loosen the screws that clamp the plastic bracket around the crt, then remove the bracket.

Replacement

1. Install the plastic bracket so the back on the clamp is 5.07 inches from the back of the crt socket guide.

2. Replace the crt shield plus the socket and base shield by reversing the removal procedure. The finished crt assembly length, with cap installed, must equal 11.05 inches. If it is longer, the assembly may short circuit the Deflection Amplifier circuit board when it is installed.

3. Place the 494/494P on its rear panel then loosen the four crt blue plastic mounting blocks on the front casting so they can be readily positioned when the crt is installed.

4. Install the crt, with shield assembly, through the front panel; seat the wedges on the side of the crt, into the blue plastic mounting blocks.

5. Position the cast bezel and implosion shield in place to ensure that there is clearance between the crt face and the bezel. (The bezel must bottom on the front casting.)



It is very important that the four mounting blocks are loose enough so the bezel retaining screws can be tightened without the bezel touching the crt face. If not the crt or the bezel may crack when the screws are tightened.

6. Remove the bezel and tighten the mounting block screws evenly in a cross pattern to approximately 8 inch pounds. Make sure the crt stays centered in the blue plastic mounting blocks as the screws are tightened.

7. Replace the bezel and implosion shield, reconnect cables to their respective board connectors, and resolder the ground lead to its terminal.

8. Replace crt light filter and snap-in printed bezel.

Repairing the Crt Trace Rotation Coil

The trace rotation coil is part of the crt assembly. If the coil is damaged beyond repair, the crt with the coil must be replaced.

If the "finish" (red) lead is broken, remove the tape and unwind one or two turns so it can be respliced and soldered to the lead wire. Rewind and retape.

If the "start" (black) lead is broken and the lead is too short to re-splice, attempt to fish out the broken end so one or two turns can be unwound, re-splice and solder to the lead; then rewind and retape.

Front Panel Assembly

It is not necessary to remove the front panel assembly to replace any of the pushbuttons. (Refer to Replacing Front Panel Pushbuttons, that follows this procedure.) The crt is removed with the front-panel assembly.

Removal

1. Set the instrument upright on its rear panel, then unscrew and remove the mounting nuts and washers for the RF INPUT, EXT MIXER, and the two 1st and 2nd LO OUTPUT connectors.

2. Remove the two screws that hold the front panel to the RF deck (center and left side).

3. Unplug the CAL OUT coaxial cable from the 3rd Converter; then disconnect the five crt cables from the Z-Axis/RF Interface, High Voltage module, and Deflection Amplifier.

4. Looking at the top of the instrument, remove the one screw that holds the front panel to the side extrusion between the crt and the right side of the instrument. Remove the four screws that hold the front panel to the side rails.

5. Pull the front panel up and off the Mother board.

Replacement

Replace the front panel by reversing the removal procedure.

Front Panel Board

NOTE

A replacement Front Panel board comes with switches and controls for the 494P. Before replacing an existing board, remove the switches and controls on the new board that are not used on the 494 version instrument.

Removal

1. Remove the front panel assembly as previously described, then remove all the knobs.

2. Place the front panel on its face and remove the eleven circuit board screws plus the screw that heat-sinks and holds IC U6090 on the board. Note that the screw next to the connector plug has a fiber washer.

3. To prevent losing the grounding rings or bushings, between the front panel controls and the front panel casting, hold the circuit board against the front panel casting while turning the complete assembly so it rests on the base of the crt assembly.

4. Gently lift the casting from the circuit board. Ensure that the grounding rings remain on the shaft of all controls as the casting is removed.

Replacement

Reverse the removal procedure, ensuring that the fiber washer is on the board screw next to the connector plug. This washer prevents the screw from shorting a circuit board run to the front panel casting.

3. Align connectors P5041 and P1034 with their respective Mother board and Interface board connectors, then press the module into place between the side rails.

4. Replace the four module holding screws and the three flange screws.

Replacing Front Panel Pushbutton Switches

Removal of the front panel assembly is not required to replace any pushbutton switch. The procedure follows.

1. Remove the front panel knobs. Loosen and remove nuts and washers for the RF INPUT, EXTERNAL MIXER, and the 1st and 2nd LO connectors.

2. Remove the screw under the CENTER FREQUENCY tuning knob that holds the panel to the front panel casting.

3. Loosen the black screws through the crt bezel so the panel can be moved enough to lift it off the casting.

4. Unplug and replace the desired switches.

Main Power Supply Module



To avoid damage to the Mother board connector J5041 and Interface connector J1034, during removal or installation of the Power Supply module, use the following procedure.

Removal

1. Disconnect the power cord, set the 494/494P on its face or front panel and remove the instrument cover.

2. On the circuit board side of the instrument, unplug the coaxial cable connector P620 from the Log and Video Amplifier assembly. On the RF deck side disconnect the plug for the cable to the Reference Lock assembly, at the lower right corner of the Power Supply module.

3. For 494P instruments, remove the cable clamp for the GPIB interconnect cable and unplug P560 to the GPIB Extender board.

4. Remove the three screws that hold the power module to the RF deck flange (bottom right side), then remove the four screws that hold the power supply module to the side rails.

5. With the instrument on its face and the RF deck on the near side, pull the left side of the power module from its side-rail (no more than 1.5 inch). Now grasp both sides of the module and lift to separate the module from the Mother board.

WARNING

Because C6111 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the power switch is turned off. A relaxation oscillator, formed by C5113, R5111, and DS5112, indicate the presence of voltages in the circuit until the potential across the filter capacitors is below 80 V.

6. Loosen and remove the two screws that hold the mounting bracket for P361. Lift the cover off the module and unplug P3045 to the Fan Drive board. The power supply should now be accessible.

Replacement

1. Reinstall P361 mounting bracket then plug P3045 onto the power supply board and replace the cover.

2. Set the instrument face down with the RF deck on the near side, then hold the power supply module over the instrument so the right side is touching the side-rail and the left side is about 1.5 inch above its side-rail.

3. Align connectors P5041 and P1034 with their respective Mother board and Interface board connectors, then press the module into place between the side rails.

4. Replace the four module holding screws and the three flange screws.

5. Reconnect the coaxial cables and GPIB cable, if appropriate, then install the cable clamp.

6. Replace the instrument cover.

High Voltage Power Supply

Before the High Voltage Power Supply circuit board can be unplugged and removed, a screw, through the side-rail into a nylon standoff bushing at the bottom corner of the board, must be removed.

Removing and Replacing the 1st LO (YIG Oscillator) A16

1. Unplug and remove the multipin connectors to the assembly. Cut the tie-down that holds the black encased RF coil to the semi-rigid cable.

2. Using a 5/16 inch open-end wrench, loosen and disconnect the semi-rigid coaxial cable.

3. Loosen and remove the four mounting screws that hold the assembly to the RF deck. Remove the 1st LO assembly.

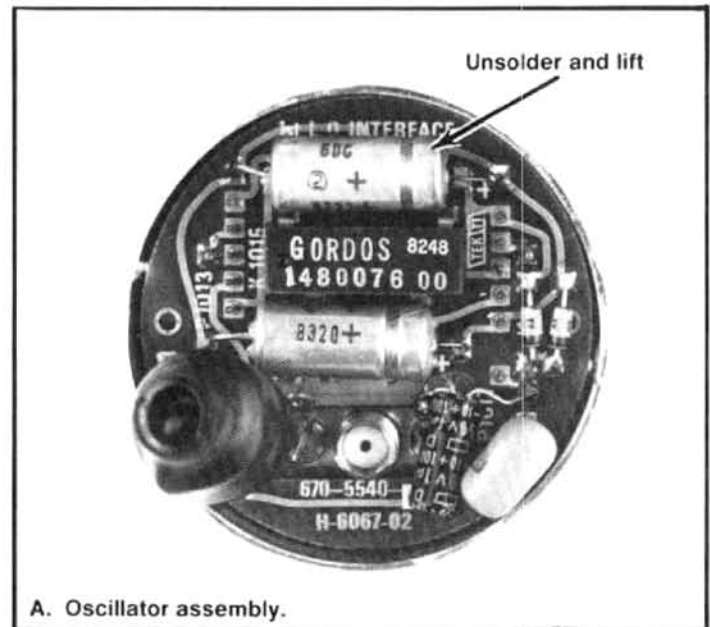
4. To replace the assembly, reverse the removal procedure. Use a tie-down to re-tie the RF coil to the semi-rigid cable to prevent vibration from breaking the coil leads

Replacing the 1st (YIG) Local Oscillator Interface Board

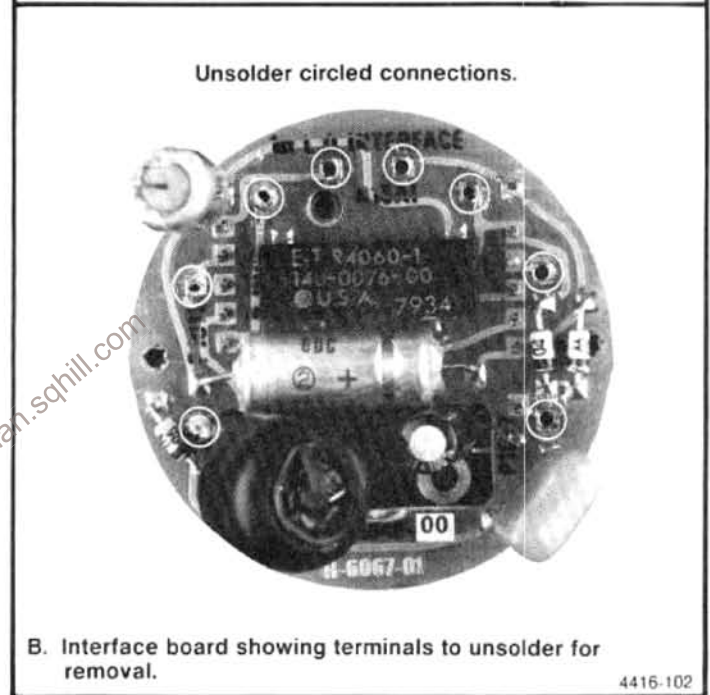
The YIG oscillator assembly includes an interface circuit board that can be replaced. To replace the board refer to Figure 6-8 and the following procedure. Use a desoldering tool to remove the solder as the leads are unsoldered.

1. Unsolder and lift one end of C1014 (820 μ F capacitor) at the top of the board.

2. Unsolder and lift one end of VR1010.



A. Oscillator assembly.



B. Interface board showing terminals to unsolder for removal.

4416-102

Figure 6-8. Removing the YIG oscillator interface board.

3. Unsolder and lift the + lead of C1016 from the YIG terminal.

4. Unsolder the eight leads to the YIG and lift the board off the assembly.

Fan Assembly

Removal

1. Remove the power supply as described in this section.

2. Remove the six screws that hold the power supply cover in place. Take the coaxial cable out of the plastic retainer clip and lift the power supply cover with fan up, so harmonica connector P3045 can be disconnected and the cover removed.

3. Remove the nuts and lockwashers that hold the fan brackets from the back side of the power supply housing. The fan will fall free from the brackets.

4. The resilient mounts at the corners of the fan frame should be replaced if a new fan is to be installed or fan vibration is generating spurs on the display.

Replacement

1. Insert four resilient mounts into the corners of the fan, flush with the fan frame.

2. Install the fan assembly on one of the fan brackets to the power supply housing by attaching its lock washers and nuts to the back of the housing.

NOTE

Fan brackets should be installed as in Figure 6-9.

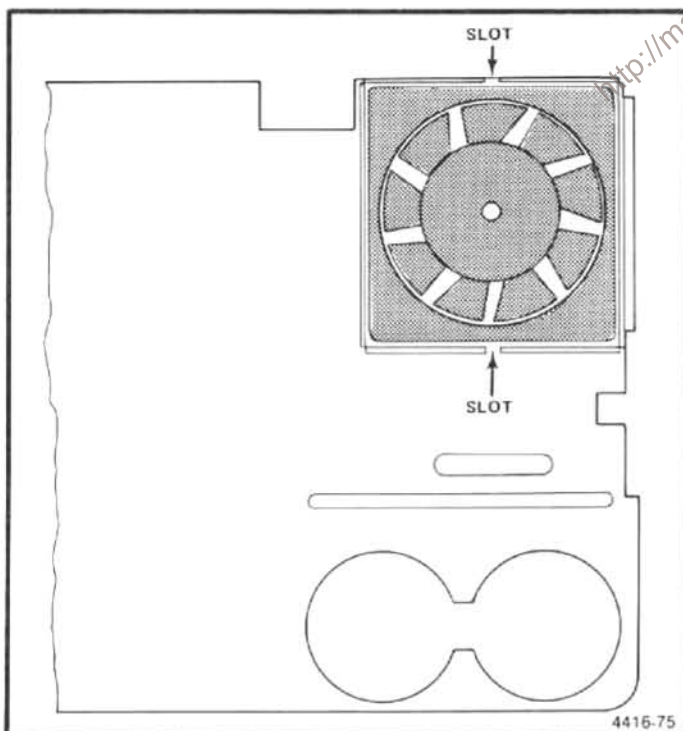


Figure 6-9. Fan assembly mounting.

3. Insert the posts of the brackets into the holes provided in the resilient mount and install the remaining bracket, with lockwashers and nuts, to the back side of the power supply housing.

4. Reconnect the fan to the Fan Drive board then replace the cover, with the fan, onto the power supply module.

5. After installing the six screws that hold the cover in place, ensure that the fan assembly moves freely. Replace the coaxial cable in the plastic retaining clip.

6. Reinstall the Power Supply assembly as directed under Power Supply Replacement. Apply power and check for normal fan operation.

MAINTENANCE ADJUSTMENTS

The following procedures are not part of the regular calibration. They are only applicable when these assemblies are replaced or after major repair.

110 MHz IF Assembly Return Loss Calibration—(Table 6-5 lists test equipment required to adjust this assembly.)

1. Test equipment setup is shown in Figure 6-10. The IF assembly must be removed to gain access to the adjustments.

2. Apply 110 MHz at 2 V peak-to-peak (+10 dBm) through 35 dB attenuation to the RF Input of the VSWR bridge. Connect the RF Out of the VSWR bridge, to the RF Input of the spectrum analyzer. (Do not connect the 110 MHz IF to the VSWR bridge.)

3. Set the test spectrum analyzer Center Frequency to 110 MHz, Frequency Span/Div to 5 MHz, Resolution Bandwidth to 3 MHz, Vertical Display to 10 dB/Div, and Ref Level to -20 dBm.

4. Adjust the step attenuator for a full screen (-20 dBm) display.

5. Connect the 110 MHz IF input to the VSWR bridge and connect a $50\ \Omega$ termination to the output of the IF amplifier. Now plug the power cable P3045 into the + and -15 V source and ground the case of the assembly.

Table 6-5
EQUIPMENT REQUIRED FOR RETURN LOSS ADJUSTMENT

Test Equipment	Characteristics	Recommended Type
Spectrum Analyzer	Frequency range ≥ 110 MHz	TEKTRONIX 49X-Series or 7L18 Spectrum Analyzer
Signal Generator	Frequency 110 MHz at +10 dBm	TEKTRONIX SG 503 for the TM 500-Series
VSWR Bridge		Wiltron VSWR Bridge, Model 62BF50
10 dB and 1 dB Step Attenuators	50 Ω , 0 dB to 40 dB	Hewlett-Packard 355C & 355D Step Attenuator
Termination	50 Ω	Tektronix Part No. 011-0049-01
Adapter	Bnc-to-Sealectro	Tektronix Part No. 175-0419-00

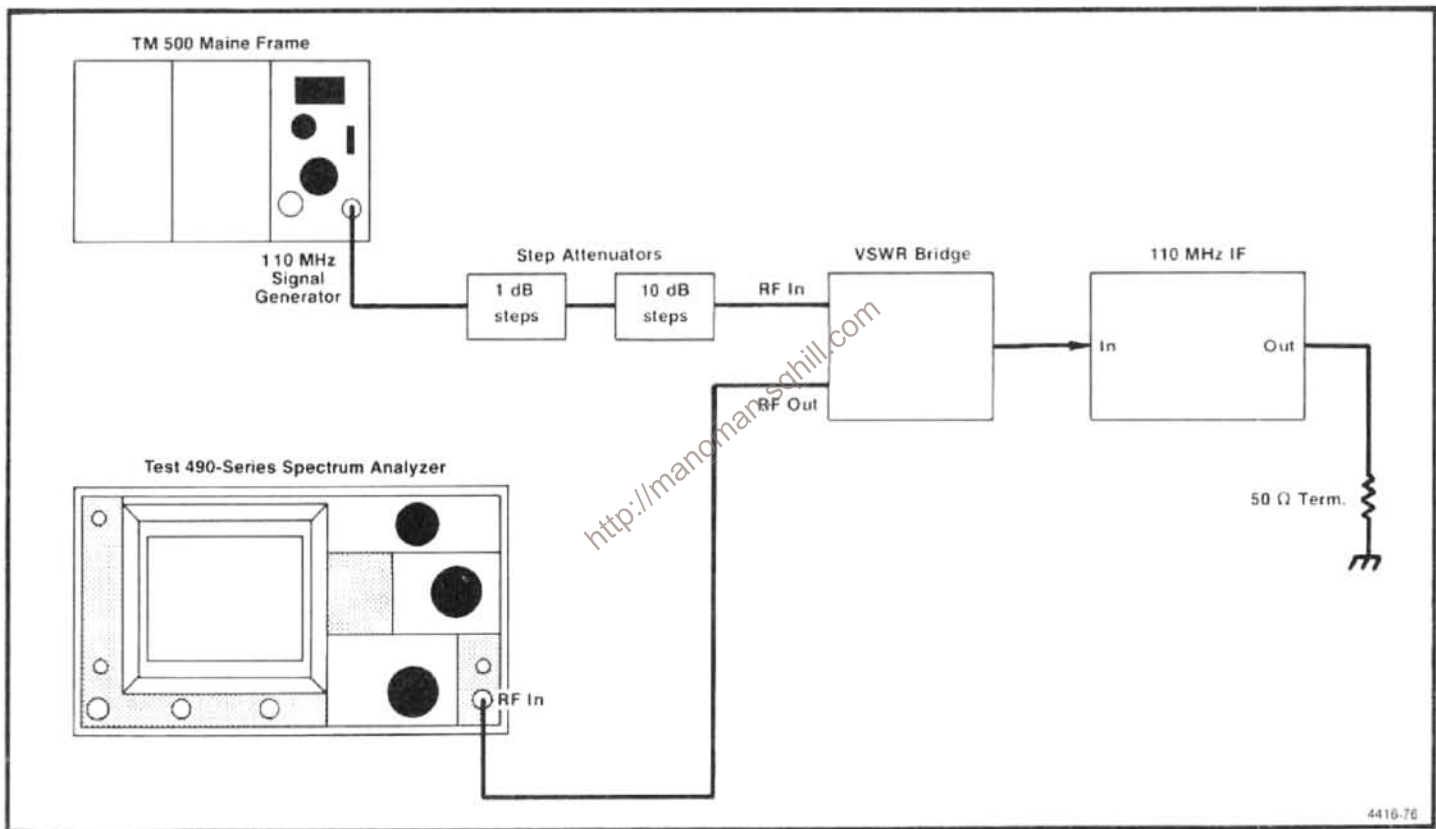


Figure 6-10. Test equipment setup for adjusting return loss in the 110 MHz IF assembly.

6. Adjust C2047 and C1054 (Figure 6-11) simultaneously for minimum signal amplitude on the spectrum analyzer display. Minimum amplitude must be at least 35 dB down from the full screen reference of -20 dBm.

7. Disconnect test equipment setup and replace the 110 MHz IF assembly.

2072 MHz 2nd Converter

The 2072 MHz Converter assembly consists of a four-cavity 2072 MHz band-pass filter, mixer, and 110 MHz low-pass filter. Because of the interaction between the 1st, 2nd, and 3rd converters, and the critical lengths of the interconnect RF cables, adjustments to the band-pass filter and mixer is not possible with the assembly in the instrument.

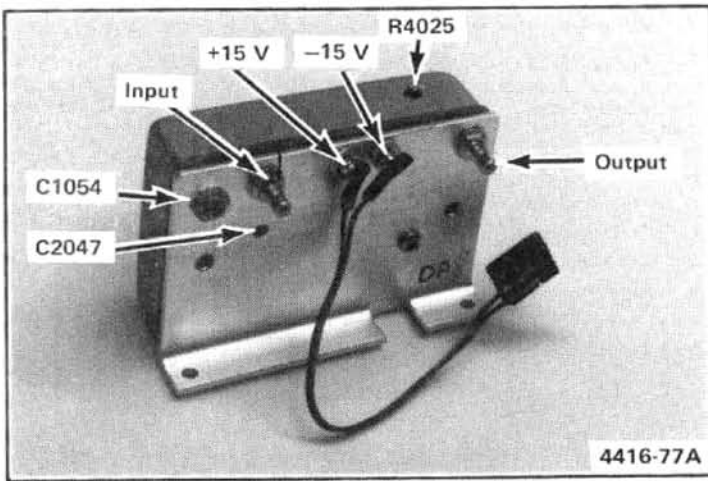


Figure 6-11. 110 MHz IF assembly showing the location of test points and adjustments.

The assembly is precalibrated at the factory prior to installation, therefore, we recommend replacing the assembly and returning the defective one to Tektronix, Inc. The following procedure describes adjustments that can be made to the low-pass filter.

110 MHz Three Cavity Filter

Alignment of this filter is not required unless the 494/494P fails to meet bandwidth specifications. The filters are adjusted for center frequency and response shape so the resolution bandwidth is within specifications. The adjustment procedure is as follows:

1. With the CAL OUT signal applied to the RF INPUT, tune the signal to center screen and reduce the RESOLUTION BANDWIDTH to 1 kHz.

2. Tune the signal to center screen to establish center frequency reference; then increase the RESOLUTION BANDWIDTH to 1 MHz.

3. Adjust the tuning slugs for best response shape, centered around the reference (Figure 6-12). Ensure bandwidth (6 dB down) is 1 MHz.

4. Check resolution bandwidth accuracy over the range of the RESOLUTION BANDWIDTH selector as per instructions in the Performance Check section to ensure that bandwidth is within specification.

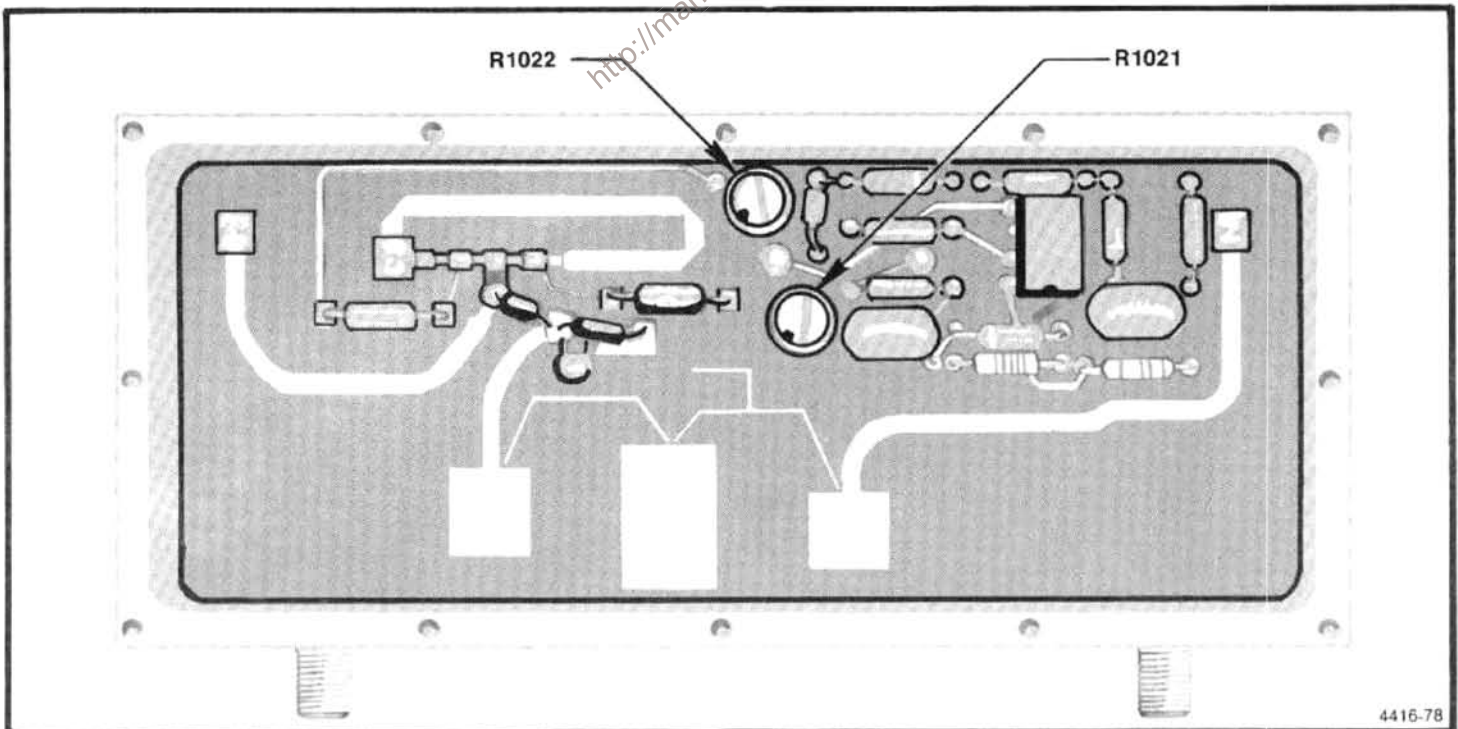


Figure 6-12. 110 MHz filter adjustments.

829 MHz Converter Maintenance

Some circuit boards in this assembly contain critical length printed elements. When damaged, these elements are usually not repairable; therefore, the circuit board must be replaced. Even though replacement boards are precalibrated and repair can be accomplished by replacing the board, we recommend sending the instrument or assembly to your Tektronix Service Center for repair and calibration.

The 829 MHz band-pass filter in the IF section, and the 719 MHz LO in the LO section, require adjustment only if the board has been damaged or active components (transistor or varactor) have been replaced. The following describes preparation for service and replacement procedures. The first two steps describe how to gain access to either the LO or the IF section; the remaining steps describe adjustment procedure for each section.

1. To gain access to the LO section

- a. Switch POWER off; use a 5/64 Allen wrench to loosen and remove the cover screws.
- b. Remove the cover.
- c. Refer to step 3 for adjustment procedure.

2. To gain access to the IF section

- a. Switch POWER off; use a 5/16 inch wrench to disconnect and remove all coaxial connectors to the 829 MHz converter.
- b. Unscrew and remove the six mounting screws, unplug the input power connector P4050, then remove the 829 MHz converter assembly.

- c. Turn the assembly over and remove the cover for the IF section.

- d. To troubleshoot or calibrate the circuits, set the assembly at a location so the input power plug P4050 can be reconnected to the Mother board. Be sure to observe plug orientation (pin 1 to pin 1).

- e. Refer to step 4 (within this procedure) for adjustment procedure.

3. 719 MHz Oscillator Range Adjustment

- a. Adjustment requires the following test equipment:

A frequency counter with a frequency range to 1 GHz (nine digit readout), sensitivity of 20 mV rms prescale, 15 mV rms direct (such as TEKTRONIX DC 508A); a digital voltmeter with a 3.5 digit readout (such as TEKTRONIX DM 502A); test leads for the DVM, a 50 Ω coaxial cable with bnc connectors (Tektronix part number 012-0482-00) and a sma male-to-bnc female adapter (Tektronix part number 015-1018-00).

- b. The 2nd LO range is 714.5 MHz to 723.5 MHz (with the cover off). 719 MHz is the optimum center frequency. Frequency of the oscillator is controlled by the Tune Volts from the 25 MHz Phase Lock circuit (located at TP1011) which varies from +5 V (low end) to +11.9 V (high end) with +6.75 to +7.5 V as the limits for operation at 719 MHz. Set the digital voltmeter to measure 12 V then connect it between TP1011 (Figure 6-13) and ground.

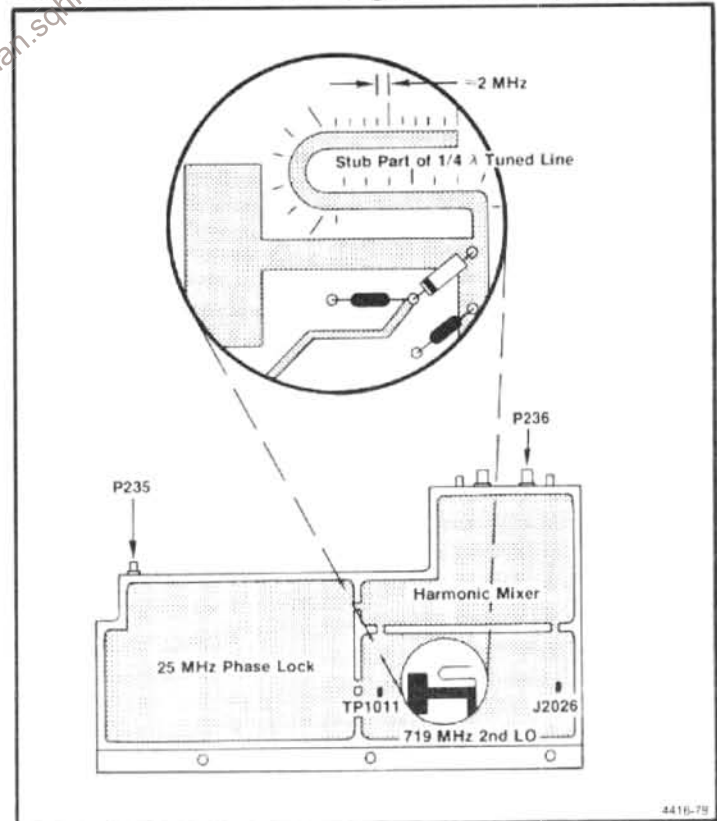


Figure 6-13. LO section of the 829 MHz converter showing test points and connectors.

c. Disconnect the 100 MHz reference from the 3rd Converter by unplugging P235 (Figure 6-13). The oscillator should go to its upper limit and the voltmeter indicate about 11.9 V.

d. Connect the 75 MHz–1000 MHz input of the frequency counter through a 50 Ω coaxial cable to the front panel 2nd LO OUTPUT connector.

e. The 719 MHz oscillator frequency is a function of the length of the printed 1/4 wavelength transmission line. Minor adjustments to the oscillator frequency are made by shortening the U-shaped transmission line stub, off the main line. Graduation marks (see Figure 6-13) along the side of the stub provide a guide to calculate frequency correction. Each minor mark from the end or cut across the stub, represents an approximate change of 2 MHz.

Check the frequency by noting the reading on the frequency counter. If above 723.900 MHz, the stub must be lengthened. Solder a bridge across the cut and recheck frequency. Nominal frequency for an uncut stub is 710 MHz.

f. Shorten the line so the frequency is near 723.500 MHz. For example: The frequency difference between the desired and the actual divided by 2 MHz, equals the number of minor divisions from the line end for the new cut. Make a cut across the line and check that the new frequency is between 723.100 and 723.900 MHz. Repeat as necessary.

g. Cover the 719 MHz oscillator cavity with the 829 MHz Converter cover, press down to ensure good shielding, and note the frequency readout of the counter. Frequency should fall within 723.600 and 724.400 MHz.

h. Reconnect P234 (100 MHz) and P237 (2182 MHz) and confirm that phase lock is operating by noting that the voltage on TP1011 is between 6.75 and 7.5 V. This completes the adjustment of the 719 MHz LO. Replace the cover and reinstall the 829 MHz converter assembly.

4. 829 MHz Coaxial Band-pass Filter Adjustment

NOTE

This procedure is necessary if the position of one of the variable capacitor loops (tabs) has been altered, changing the bandpass characteristics of the filter.

a. Test equipment required:

Spectrum analyzer with tracking generator (such as 49X-Series Spectrum Analyzer with TR 503 Tracking Generator; or 7L13 with a TR 502 Tracking Generator); Frequency Counter (such as TEKTRONIX DC 508); Return Loss Bridge (such as Wiltron Model 62BF50).

b. Unsolder and reconnect the jumper, on the 829 MHz Amplifier board, to the test Peltola jack J1029 (see Figure 6-14).

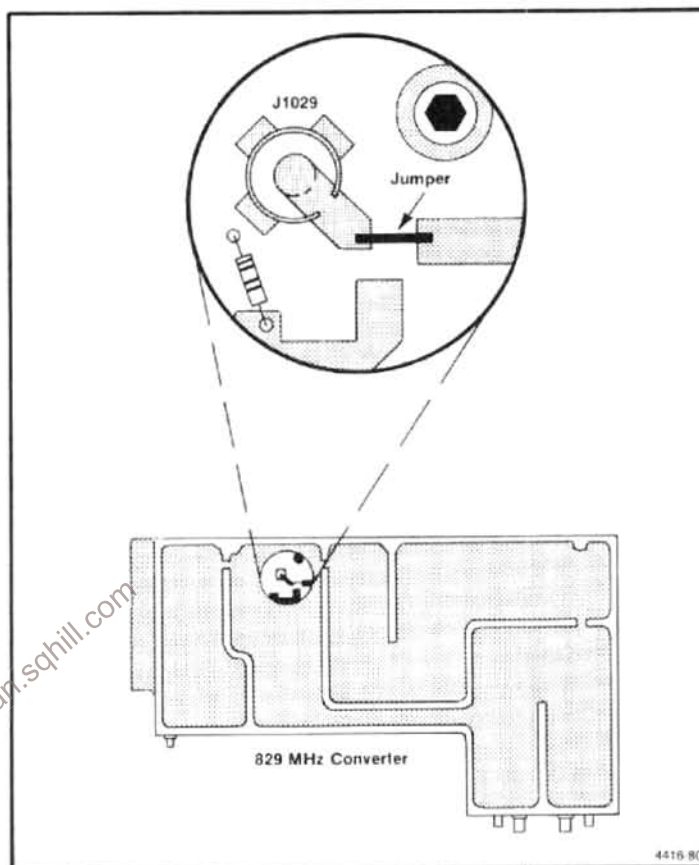


Figure 6-14. Location of test jack and jumper on the 829 MHz amplifier board.

c. Connect the spectrum analyzer, tracking generator, and frequency counter together as a system, with the frequency counter connected to the Auxiliary RF Output of the tracking generator (see Figure 6-15).

d. Connect the spectrum analyzer/tracking generator system through the return loss bridge to the Peltola jack (J1029) on the 829 MHz amplifier board (see Figure 6-15). Reconnect P235 (100 MHz reference signal) and P237 (2182 MHz input) to the LO section of the converter.

Terminate the 110 MHz Output (J232) connector with 50 Ω , using a bnc-to Sealectro adapter and 20 dB bnc attenuator. Pull the IF SELECT line high by switching to band 2 (1.7–5.5 GHz).

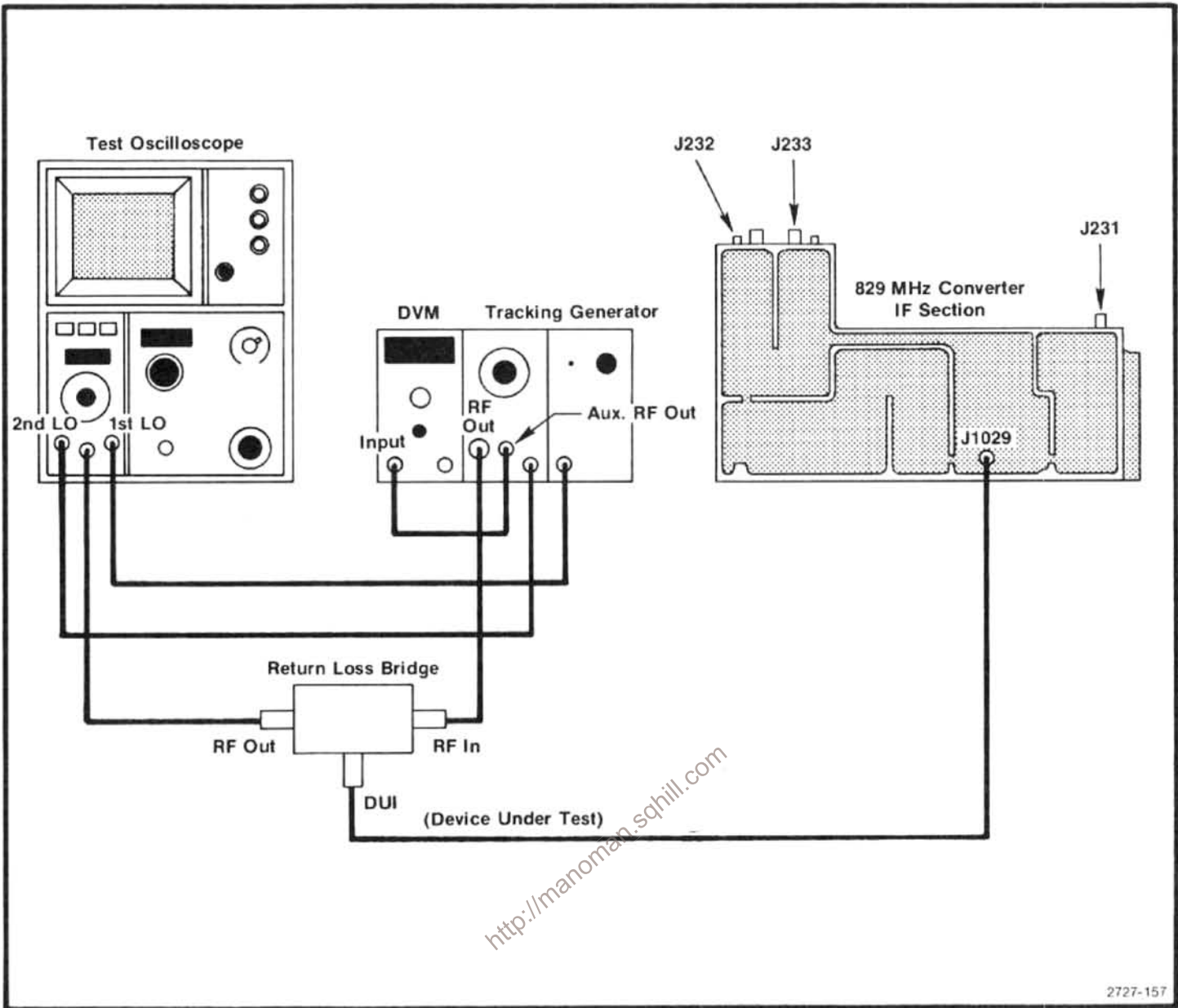


Figure 6-15. Test equipment setup for aligning the 829 MHz filter.

e. Set the test spectrum analyzer Reference Level to -20 dBm, Vertical Display mode to 2 dB/div, Resolution Bandwidth to 300 kHz, and Freq Span/Div to 20 MHz. Tune the Center Frequency for a readout of 829.00 MHz on the frequency counter.

f. Adjust the $1/4$ wavelength lines in the filter in sequence, starting with the resonator at the 829.1 MHz input (see Figure 6-16). Adjustment is made by shorting the adjacent resonator to ground with a low inductance conductor, such as a broad blade screwdriver, then bend the loop or tab of the respective stub with a non-metallic tuning tool to change the series capacitance of the resonator.

g. With the adjacent resonator (second) shorted to ground, adjust the series capacitance by bending the tab so the response on the spectrum analyzer display is centered at 829 MHz (see Figure 6-17A).

h. Now move the shorting strap (screwdriver) to the next resonator and adjust the tab of the second resonator for a response as indicated in Figure 6-17B.

i. Remove the short from the third resonator and short the fourth resonator. Adjust the third resonator for a response similar to that shown in Figure 6-18A.

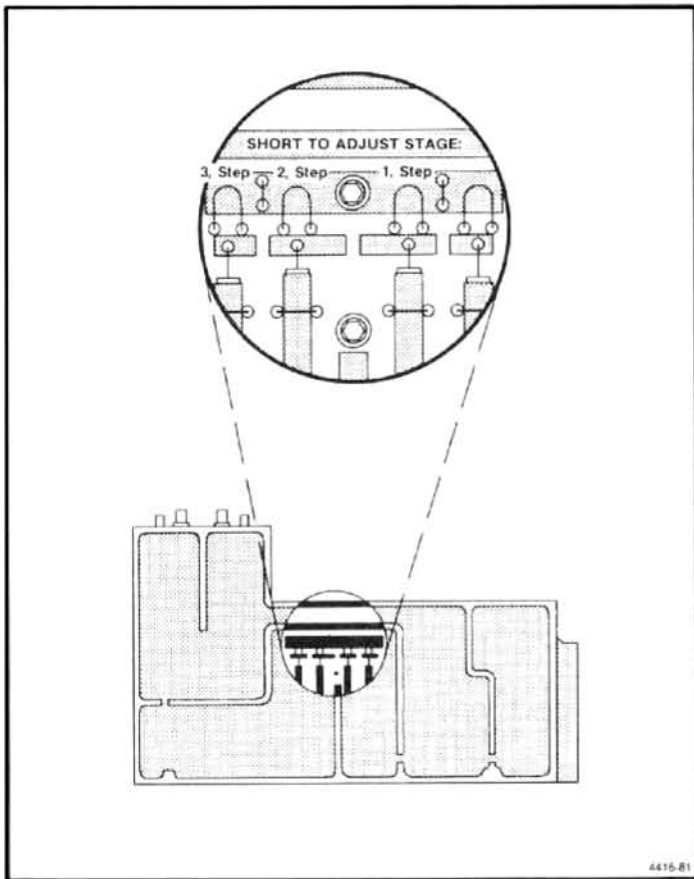


Figure 6-16. Filter tune tabs in the 829 MHz converter.

j. Repeat the procedure for the final (fourth) resonator for a response similar to that shown in Figure 6-18B.

k. Check that the return loss is equal to or greater than 12 dB.

l. Disconnect the return loss Device Under Test lead to the Peltola jack J1029 on the 829 MHz Amplifier board, then unsolder and reconnect the jumper to the amplifier output.

m. Replace the 829 MHz Converter cover and reinstall the assembly in the 494/494P.

Troubleshooting and Calibrating the 2182 MHz Phase Locked 2nd LO

The assembly contains a microstrip phase locked 2182 MHz oscillator and its phase locking circuits. The 14-22 MHz Phase Lock board is contained in the mu metal housing; the 2182 MHz Oscillator, 2200 MHz Reference, and 2200 MHz Reference Mixer are contained in the machined aluminum housing.

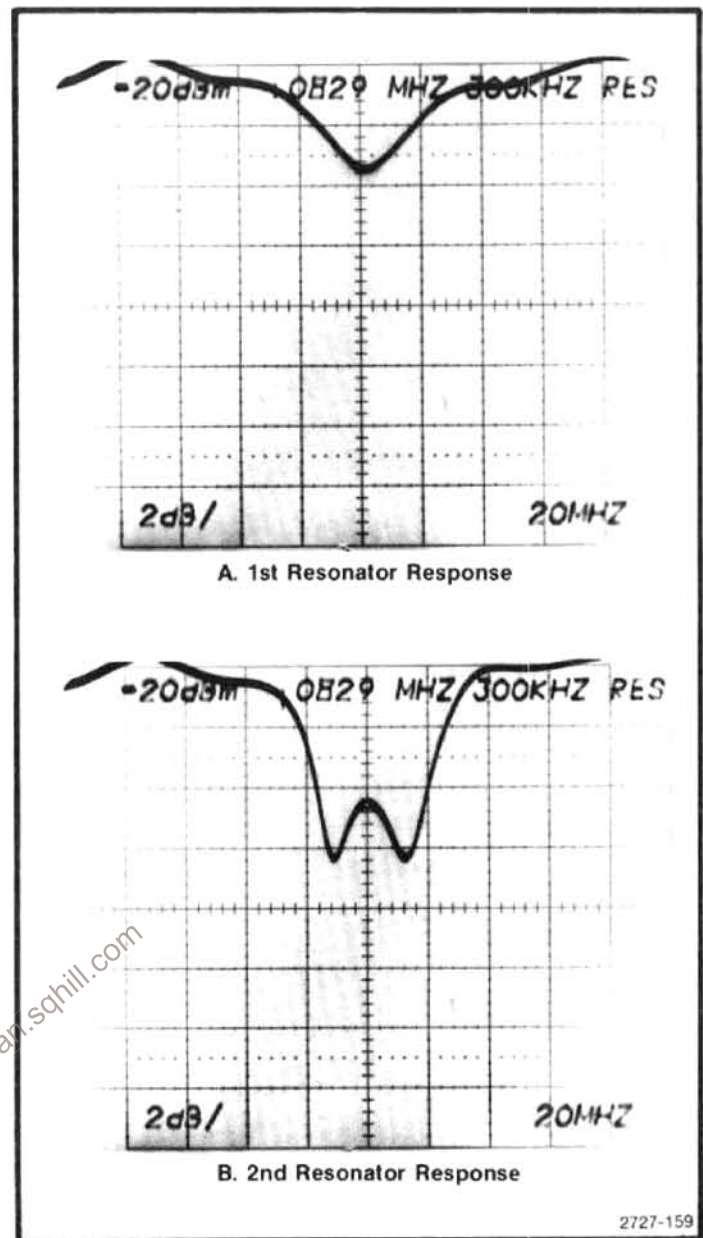


Figure 6-17. Typical response when the first and second resonators of the 829 MHz filter are adjusted correctly.

The 2182 MHz Microstrip Oscillator and the 2200 MHz Reference Mixer contain critical length printed elements. These elements are difficult to repair; therefore, the board should be replaced if damaged. If either the varactor diode or the oscillator transistor for the 2182 MHz Oscillator is replaced and the oscillator frequency is beyond adjustment with the frequency adjust tab, described in this procedure, the circuit board must be replaced.

Even though replacement boards are precalibrated at the factory and repair can be accomplished by replacing the board, we recommend sending the instrument or assembly to your Tektronix Service Center for repair to insure best performance.

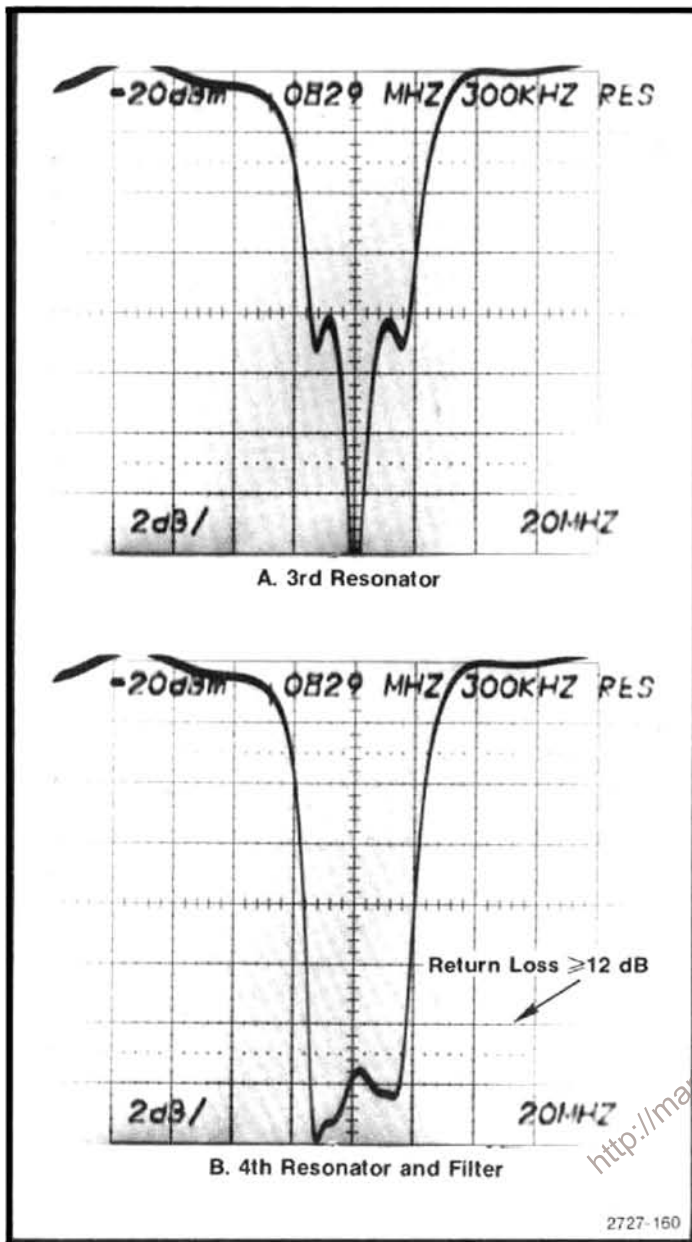


Figure 6-18. Typical response when the third and fourth resonators are tuned correctly.

Table 6-6
EQUIPMENT REQUIRED FOR 2nd LO CALIBRATION

Test Equipment	Characteristics	Recommended Type
Spectrum Analyzer	Frequency range to 2.2 GHz	TEKTRONIX 49X-Series
Signal Generator	Calibrated 100 MHz, with ± 20 kHz accuracy and an amplitude that is settable to 0 dBm.	Hewlett-Packard Mode 8640 A/B
Digital Voltmeter	Measures to within 0.01 V, impedance ≥ 1 M Ω .	TEKTRONIX TM 500-Series DM 501A, DM 502A, or DM 5010
Variable Power Supply	0 to 12.5 V, accurate to 0.1 V	TEKTRONIX TM 500-Series, such as PS 501 or PS 5010
Terminations (2)	50 Ω , 3mm connectors	Tektronix Part No. 011-0049-01

The 2182 MHz Phase Locked 2nd LO should only require calibration when a component within the assembly has been replaced. This procedure is in two parts, the LO section and the Phase Lock section. Equipment required to calibrate both the LO section is listed in Table 6-6 and equipment for the Phase Lock section in Table 6-7.

1. Preparation

a. Test equipment setup is shown in Figure 6-19. Turn the POWER off. Place the 494/494P Spectrum Analyzer upside down so the RF deck is exposed. Use a 5/16 inch wrench to loosen and remove the two semi-rigid cable connections to the assembly. Remove the flexible coaxial cable connection to the 100 MHz input.

b. Remove the 14 screws that hold the cover on the mu-metal section and remove the cover. Unsolder the leads to feedthrough capacitors C2203 and C2204. (These are the center two feedthroughs that feed through the circuit board, as shown in Figure 6-23.)

c. Replace the cover using two or three screws to hold the cover in place. Remove the 2nd LO assembly mounting screws and carefully remove the 2nd LO assembly so the power input connections remain intact. Turn the assembly over so the machined aluminum housing is up and place the assembly on a flat surface. Use a 5/64 Allen wrench to remove the screws holding the lid on the machined aluminum housing. Place the screws in a safe place; then remove the lid for the aluminum housing, exposing the three RF circuit boards within the oscillator section.

d. Install a 50 Ω terminator on the 2182 MHz buffered output port, P222, (see Figure 6-20). Set the variable power supply to 0 V. Connect the plus (+) terminal to the 2nd LO housing and the negative (-) terminal to the exposed end of C2203 and L2031, through a 1 k Ω resistor.

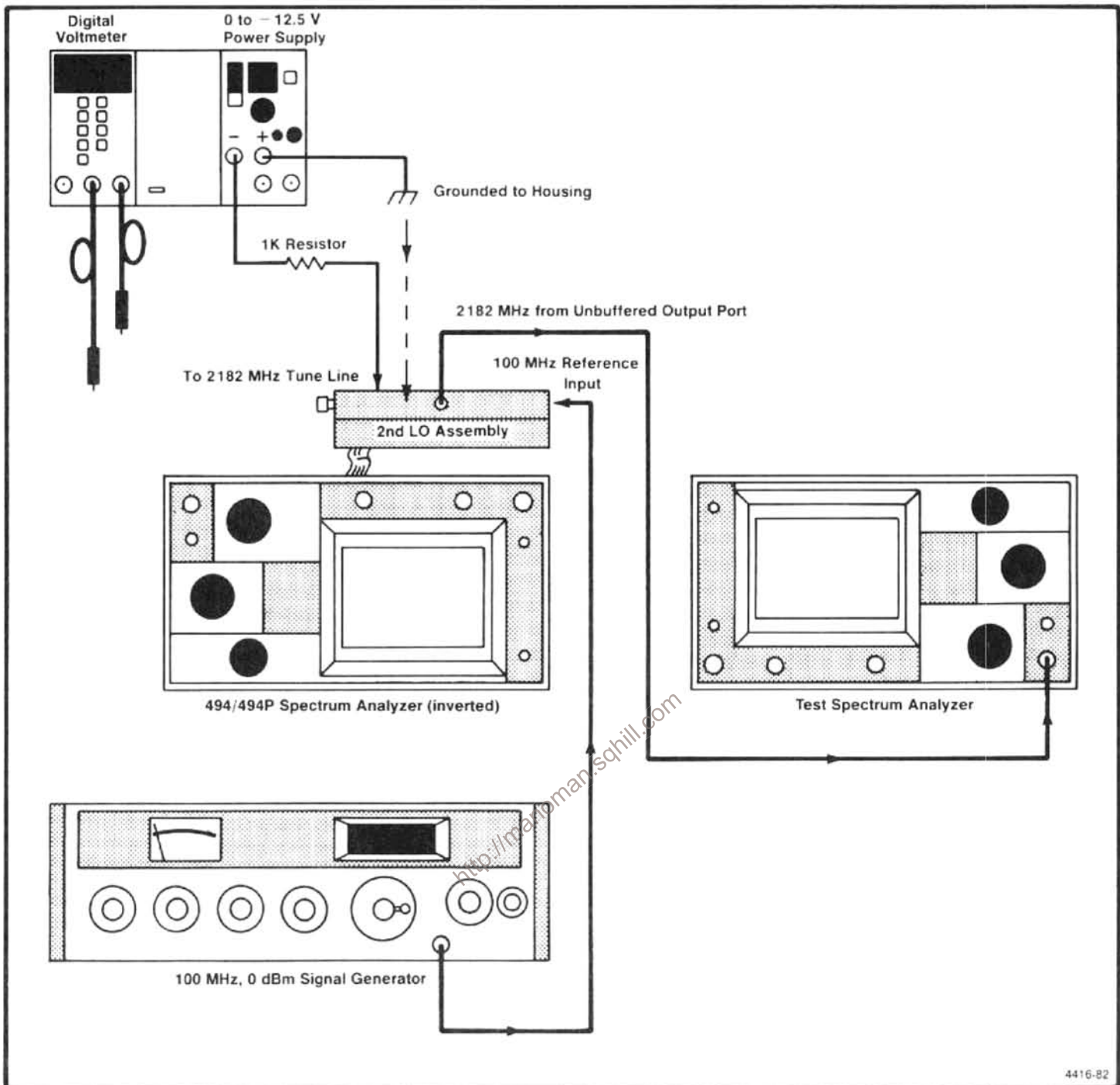


Figure 6-19. Test equipment setup for calibrating the oscillator section of the 2182 MHz Phase Locked 2nd LO.

e. Apply a 100 MHz, 0 dBm signal from the signal generator to the 100 MHz Reference input port, P221. (Frequency must be within 20 kHz of 100 MHz.)

f. Connect a test spectrum analyzer to the 2182 MHz unbuffered output port, P220. Set the test analyzer Center Frequency to 2182 MHz, Freq Span/div to 20 MHz, Vertical Display to 10 dB/Div, and the Reference Level to +10 dBm. Do not position any of the cables over the 2nd LO assembly oscillator section because they can affect the frequency of the oscillator.

g. Bend the feedback and frequency adjusting tabs, C1021 and C1022 (see Figure 6-20), with your finger so they are approximately 30° above the board surface.

2. Adjust and Check Oscillator Frequency (Refer to Figure 6-20)

a. Switch the Power to both the 494/494P and the variable power supply on. Adjust the voltage output from the variable power supply to 5.0 V. Voltage on C2203 should now equal -5 V and a signal should appear on the test spectrum analyzer.

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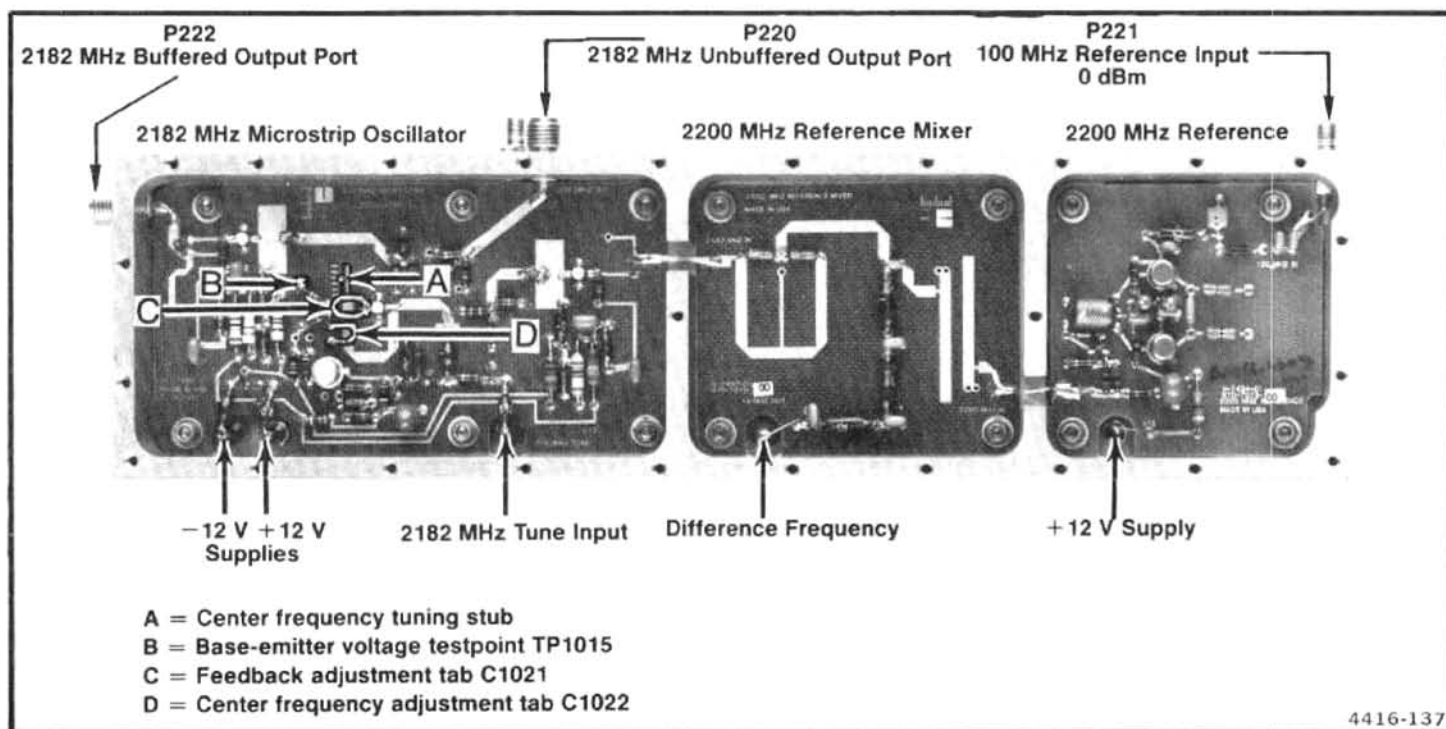


Figure 6-20. Adjustments and test point locations within the 829 MHz Converter oscillator section.

b. Check for a collector voltage across C2023 of +10.0, ± 0.7 V.

c. Check V_{be} at TP1015 (B in Figure 6-20). If V_{be} is greater than +0.5 V, push the feedback adjustment tab down slightly and if less than -0.3 V, lift the tab. If V_{be} is greater than +0.8 V, replace the microstrip oscillator board. If V_{be} is more negative than -1 V, check the bias circuitry. Adjust the tab so V_{be} is +0.15 V, ± 0.05 V at TP1015. Do not touch the feedback tab while measuring voltages.

d. Check for an oscillator frequency of 2182 MHz, ± 5 MHz. Bend the frequency adjustment tab C1022 (D in Figure 6-20) to bring the oscillator within tolerance. (Bend the tab up to increase frequency and down to lower frequency.) If unable to bring the oscillator frequency within range, replace the 2182 MHz microstrip oscillator board.

3. Measure Output Power

NOTE

Before making power measurements, ensure that the unused port is terminated into 50 Ω . Unterminated ports will degrade both frequency and power measurements.

a. Check for 0 dBm ± 3 dB output power at the unbuffered port, P220.

b. Connect the test spectrum analyzer to P222, terminate P220, then check for an output level of +10 dBm ± 3 dB from the buffered port.

4. Check the 2200 MHz Reference Mixer

a. Use a probe, consisting of a short length of semi-rigid coaxial cable with a dc block (see Figure 6-21), to connect the output of the reference mixer at C2204 to the input of the test spectrum analyzer. Ground the outer shield of the coaxial cable against the 2nd LO housing.

b. Confirm that the output signal frequency is 18 MHz ± 1 MHz. Adjust the tab C1022 (Figure 6-20) for the 2182 MHz Microstrip Oscillator, to bring the 18 MHz within the 1 MHz tolerance.

c. Confirm that the output level of the 18 MHz signal is approximately -36 dBm. If the level is below -46 dBm, check the signal levels from the 2200 MHz Reference Mixer and the 2182 MHz Microstrip Oscillator (-28 dBm, ± 8 dB from the 2200 MHz Reference Mixer and +8 dBm, ± 3 dB from the oscillator).

5. Check the Tune Range

a. Adjust the variable supply to vary the voltage to the 2182 MHz tune line from 0 to -12.5 V and note the frequency change at C2204 (output of the 2200 MHz Reference Mixer).

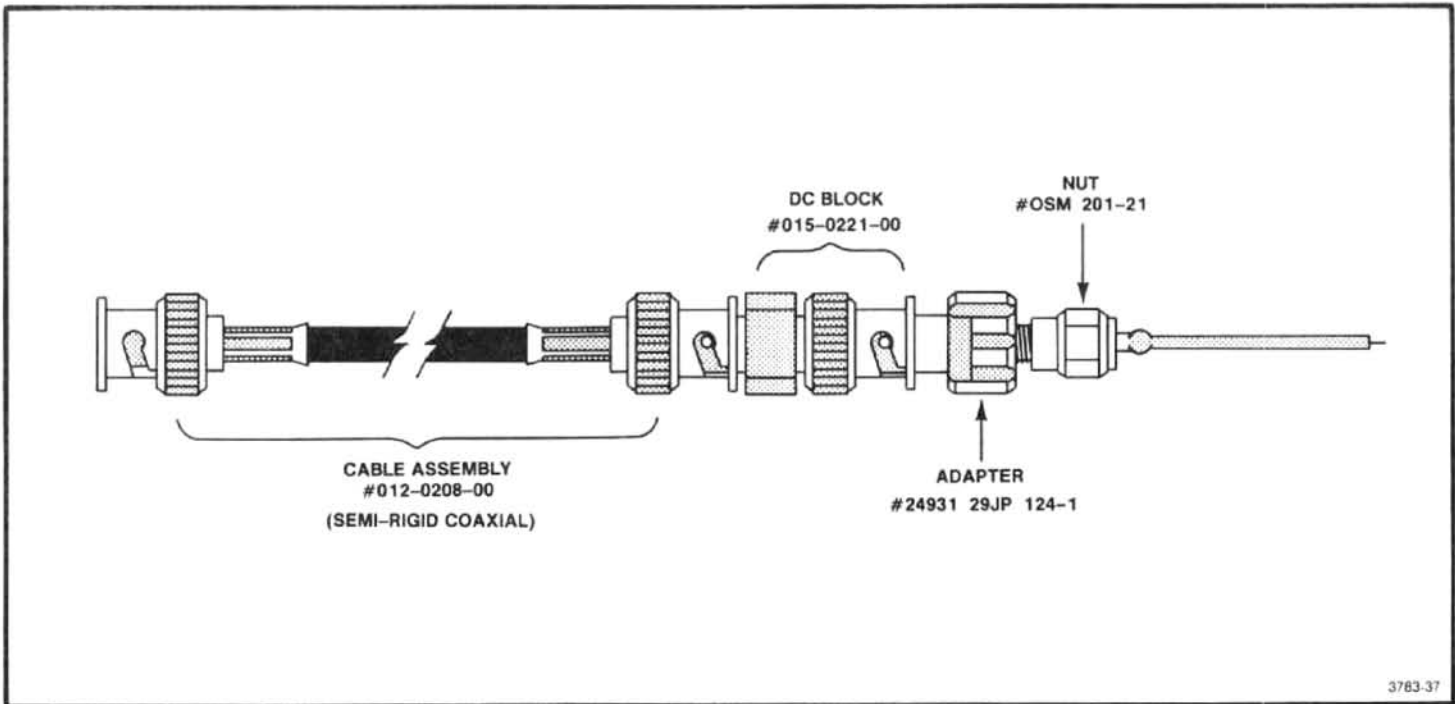


Figure 6-21. Construction details of a coaxial test probe for the 2182 MHz Phase Locked 2nd LO.

b. Frequency change or tune range should equal 20 to 35 MHz for a voltage change of 0 to -12.5 V on the tune line.

6. Reassembly

a. Disconnect and remove the connections from the variable power supply and the test spectrum analyzer.

b. Replace the lid for the oscillator housing and install the 26 screws. Install the screws loosely, then tighten them starting from the center of the lid and progress along the edges toward the corners to insure that no gaps exist between the lid and the housing. Any gaps will allow RF leakage that can produce spurious responses.

c. Reinstall the assembly on the RF deck. Remove the $50\ \Omega$ terminations and reconnect the cables. Use a $5/16$ inch

open-end wrench to tighten the semi-rigid coaxial connectors to 8 to 10 inch-pounds.

d. Remove the mu-metal lid and reconnect the leads to feedthrough capacitors C2203 and C2204, on the Phase Lock board (Figure 6-23). Replace the lid and install the 14 screws. Tighten the screws from the center toward the corners of the lid to prevent gaps between the lid and the housing. Do not overtighten because the screws are easily stripped.

Troubleshooting and Calibrating the 16–20 MHz Phase Lock Section

This side of the assembly contains the 16–20 MHz Phase Lock circuit board (see Figure 6-23). Replacing oscillator components in this section may alter sweep linearity and frequency of the 16–20 MHz oscillator. The following checks and calibration should aid in repairing and returning the assembly to satisfactory operation.

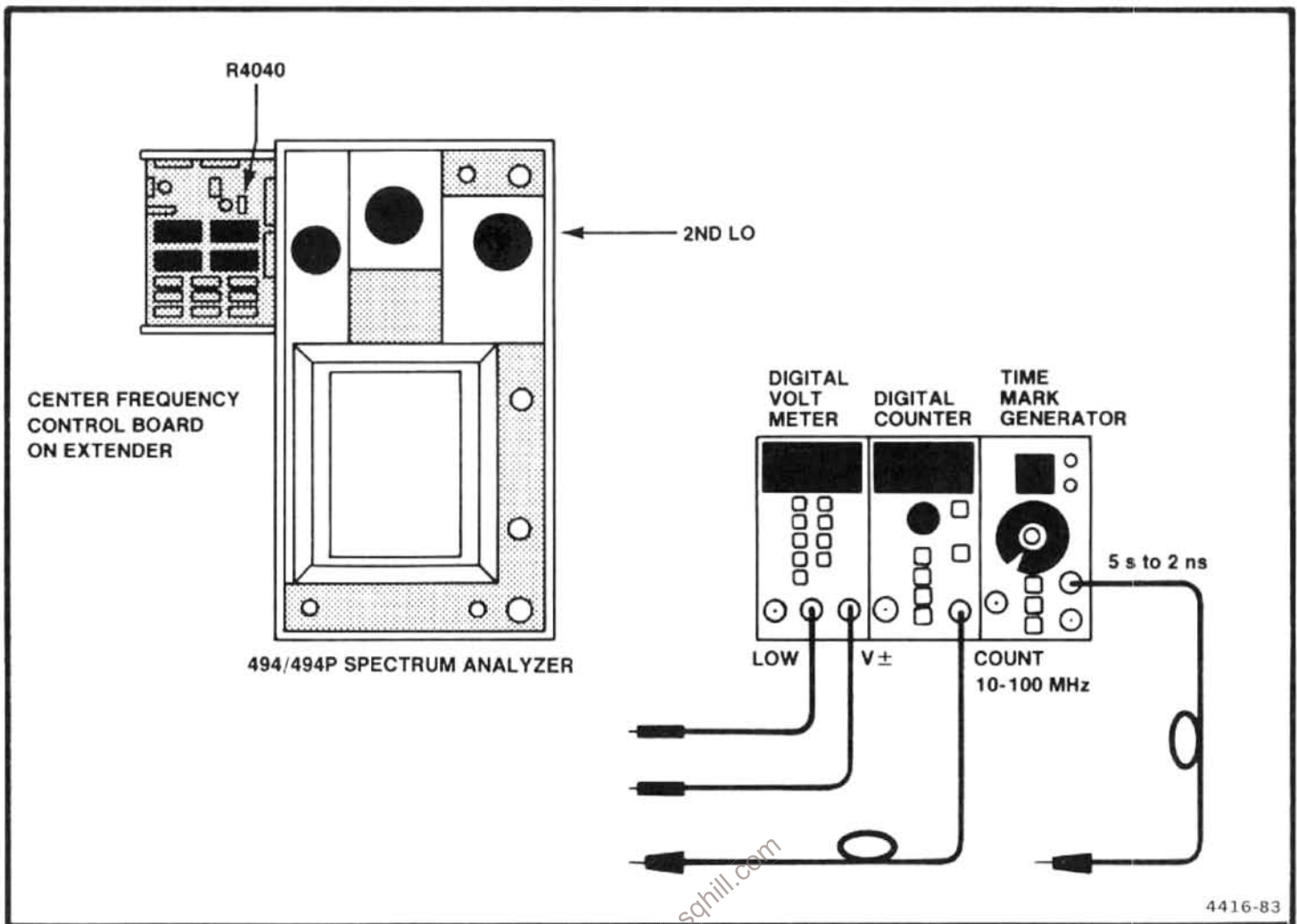


Figure 6-22. Test equipment setup for calibrating the Phase Lock section of the 2182 MHz 2nd LO.

Table 6-7
EQUIPMENT REQUIRED FOR CALIBRATING THE
16-20 MHz PHASE LOCK CIRCUIT

Test Equipment	Characteristics	Recommended Type
Digital Voltmeter	Floating input, measures to within 0.01 V _{dc}	TEKTRONIX TM 500-Series DM 501A, DM 502A, or DM 5010
Frequency Counter	Frequency to 80 MHz	TEKTRONIX TM 500-Series DC 503A, DC 508A, DC 509, DC 5009, or DC 5010
Time-Mark Generator	Marker output, 1 s to 1 μs; accuracy 0.001%	TEKTRONIX TG 501
Service Kit Extender board		Tektronix Part No. 672-0865-00

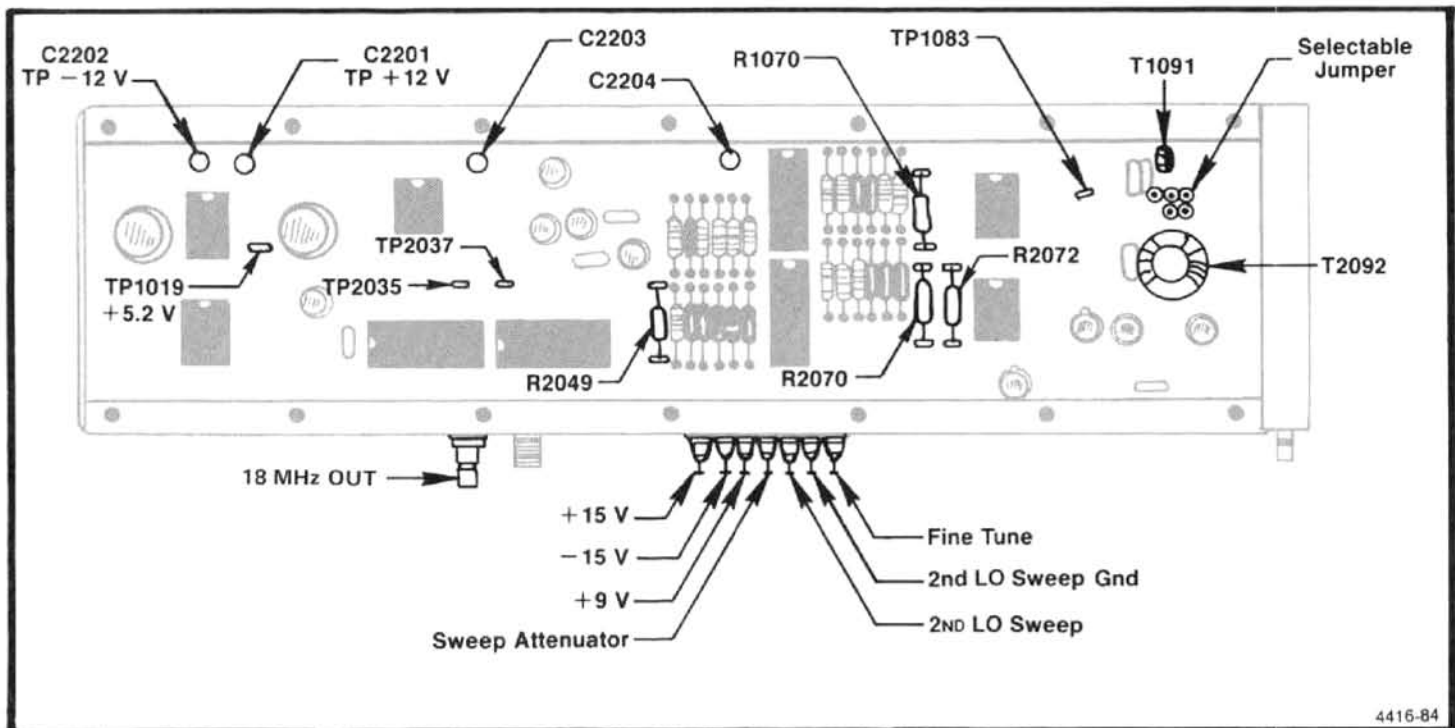


Figure 6-23. Test points and component location pertaining to calibrating the 16-20 MHz Phase Lock circuit for the 2182 MHz 2nd LO.

1. Preliminary

a. Test equipment setup is shown in Figure 6-22. Remove and install the Center Frequency Control board on an extender board.

b. Switch POWER on and set the FREQ SPAN/DIV to 1 MHz.

2. Check Voltages

a. Check all input voltages at the feedthrough capacitors in the housing wall. Refer to Figure 6-23 or the data printed on the lid. Voltage at the sweep and tune input lines should equal $0\text{ V} \pm 0.05\text{ V}$ with the FREQ SPAN/DIV $\geq 500\text{ kHz}$.

b. Switch the POWER off. Remove the lid from the metal housing assembly to gain access to internal circuitry.

c. Switch POWER on, then check the internal regulated voltages; $+12\text{ V} \pm 0.4\text{ V}$ at C2201, $-12\text{ V} \pm 0.4\text{ V}$ at C2202, and $+5.2\text{ V} \pm 0.25\text{ V}$ at TP1019 (see Figure 6-23). Check the output of the shaper at TP1083 for $0.0\text{ V} \pm 0.3\text{ V}$.

3. Setting Center Frequency

a. Connect a frequency counter to TP2035 and note the frequency. If the frequency is $18 \pm 0.050\text{ MHz}$ no correction

is necessary; proceed to part 4 (Setting Tune Sensitivity and Range). If outside the range proceed as follows:

1) Turn POWER off. Unsolder and remove one end of Shaper Offset resistor R1070. Unsolder the wire strap between T2092 and T1091, at the T1091 end, and lift it free.

2) Solder a flexible wire jumper to the T2092 end; then, by means of a plastic tuning tool, attach the free end to one of the three pads for T1091 and note the frequency readout of the counter.

CAUTION

If this flexible wire touches ground while the circuit is operating, the supply regulators can be damaged. The regulators are not protected against a short circuit.

3) If one of the pads provides a frequency that is within the range of $17.5 \pm 0.25\text{ MHz}$, solder the wire strap to this pad. If the frequency is still outside the range, move the jumper to the other pad for T2092 and repeat the procedure. Frequency must equal $17.5 \pm 0.25\text{ MHz}$.

b. Turn POWER OFF. Substitute a 10 turn $25\text{ k}\Omega$ potentiometer in series with a $5\text{ k}\Omega$ resistor in place of R1070.

c. Turn POWER on and with the counter connected to TP2035, adjust the potentiometer for a frequency readout of 18 MHz \pm 50 kHz.

d. Switch POWER off, measure the total resistance value and replace R1070 with a 1% resistor of this measured value. Switch POWER on and recheck the frequency to ensure that it is 18 MHz \pm 50 kHz. Disconnect the counter from TP2035.

4. Setting Tune Sensitivity and Range

a. Center the Fine Tune adjustment R4040, on the Center Frequency Control board and the 2nd LO Sweep adjustment R1067, on the Span Attenuator board (Figure 6-24).

b. Decrease the FREQ SPAN/DIV from above 200 kHz to 200 kHz or less. The 2nd LO is now in the center of its tune range.

c. Press <SHIFT> INT to disable frequency correction; then press <SHIFT> READOUT and select frequency display of 2nd LO (2) from the menu. Readout will now indicate the 2nd LO frequency.

d. Tune the 2nd LO to one end of its range where the frequency readout no longer changes. Note the frequency and measure the voltage on the Tune Line at the input feed-through capacitor (Figure 6-23).

e. Tune the 2nd LO to the other end of its range and again note the frequency and the new voltage reading.

f. Calculate the frequency change per volt (frequency range versus voltage range). Frequency change per volt should equal 1280 kHz \pm 5% or range between 1216 kHz and 1344 kHz.

g. If the frequency/volt change is low, decrease the value of select resistor R2072 and increase the value of R2070 (Figure 6-23). Keep the ratio of R2072 and R2070 the same. If the frequency/volt change is high, increase R2072 and decrease R2070.

h. Press <SHIFT> PULSE STRETCHER and select 2nd LO for calibration. Perform the procedure that is called out to adjust the Fine Tune Range R4040 and Fine Tune Sensitivity R3040 to calibrate the 2nd LO tuning range.

5. Setting Sweep Range

a. Apply 5 μ s time markers from the Time Mark Generator to the RF INPUT. Set the FREQ SPAN/DIV to 500 kHz then back to 200 kHz to center the 2nd LO frequency.

b. Adjust the REF LEVEL to display the 200 kHz markers then center one of the markers with the CENTER FREQUENCY control.

c. Adjust the 2nd LO Sweep R1067, on the Span Attenuator board (Figure 6-24), so the comb lines on opposite sides of the screen, are exactly 8 major divisions apart.

6. Check and Adjust Tune Linearity

a. With Frequency Corrections disabled (see part 4c), apply 5 μ s markers from a Time Mark Generator to the RF INPUT. Set the FREQUENCY to 20 MHz, FREQ SPAN/DIV to 200 kHz and activate AUTO RESOLN. Adjust the REF LEVEL so a comb of 200 kHz markers is displayed.

b. Turn the CENTER FREQUENCY control counterclockwise until the center frequency stops tuning, decrease FREQ SPAN/DIV to 50 kHz then tune the CENTER FREQUENCY up until a marker signal is one major division from the left edge of the graticule. A comb line (or marker signal) should appear on or near the first major division in from the right side of the screen.

c. If the right marker is not exactly 8 divisions from the left marker, note the error to the nearest 0.5 minor division.

d. Turn the CENTER FREQUENCY control clockwise, to increase center frequency, until the next marker signal is one division in from the left edge and again note the spacing between this marker and the marker near the right edge.

e. Continue this process of tuning up in frequency until the center frequency stops tuning, noting the signal spacing at each check point.

f. If the peak-to-peak error is 2.5 minor divisions (25 kHz) or less, the linearity over the center 2 MHz of sweep is satisfactory; if more, the shaper needs adjustment or repair.

g. Switch the FREQ SPAN/DIV to 200 kHz, tune to the low end of the sweep range and note the linearity over the center eight divisions of span, then tune to the high end of the 2nd LO range and again note the linearity. Peak-to-peak deviation should not exceed 0.5 minor division.

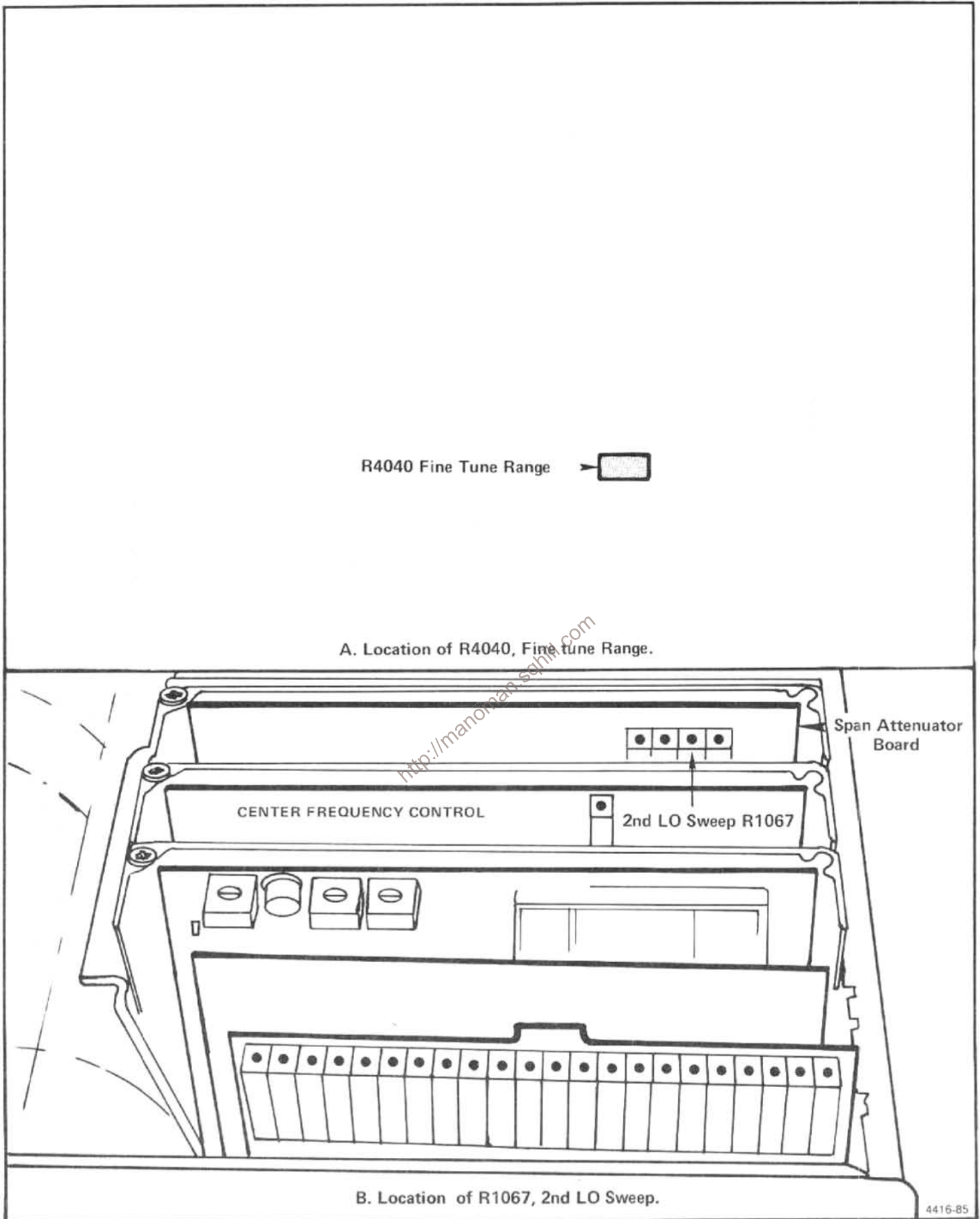


Figure 6-24. Location of R4040 on the CF Control board.

h. If the shaper needs adjustment or repair proceed as follows:

1) A shaper diode or resistor may be defective if the comb line spacing is consistent for part of the tuning range and 30 kHz or more off for the other parts of the sweep. To test the diodes for forward conduction, tune to the low end of the range and short R2049 (Figure 6-23). The output of U1073A (pin 1) should equal about +3 V. U1059 diodes B through G and U2059 diodes A through F should all have a 0.48 V forward drop. Use a floating or digital voltmeter to check the drop.

2) Switch POWER off then temporarily replace Shaper resistor R2049 with a 20 k Ω potentiometer. Switch POWER on, and adjust the potentiometer to obtain the best overall linearity; decreasing resistance will decrease the spacing between comb lines in the upper portion of the tune range and spread the spacing for the lower portion. Increasing the resistance of R2049 will reverse the effect. When the correct setting is found, turn POWER off, measure the resistance, and replace with a fixed resistor of the same or near the same value.

7. Conclusion

a. Replace the housing lid with its 14 screws.

b. Tighten the screws sequentially, starting from the center of the lid and progressing toward the corners to prevent gaps between the lid and the housing. Use care to not strip the screws as you tighten them.

c. This completes the 2182 MHz Phase Locked 2nd LO calibration. Refer to "Frequency Control System Calibration" in the Adjustment section for recalibrating the system.

Troubleshooting Aids for the 2182 MHz Phase Locked 2nd LO Assembly

NOTE

If the Phase Locked assembly is in the instrument, set the FREQ SPAN/DIV to 500 kHz or more so the 2nd LO is not swept.

The difference frequency from the 2200 MHz Reference Mixer is amplified and fed to output port P224. Nominally the signal at the 18 MHz port is 18 MHz with an output level of approximately -5 dBm into 50 Ω . This port is convenient for monitoring the operation of the 16 to 20 MHz voltage controlled oscillator. When phase lock is operating, the difference frequency exactly equals the frequency of the VCO. If loop lock is not functioning properly, the difference frequency signal will either disappear completely or tune to its

range limit of approximately 6 MHz or 30 MHz. Note that when the loop is unlocked, RF leakage from the 16-20 MHz oscillator buffer can be seen at P224 with a level of approximately -35 dBm. The amplified difference frequency can be monitored at TP2035.

Another check of phase lock operation can be done by measuring the dc voltage on the 2182 MHz Tune Line at feedthrough capacitor C2203. Nominally this voltage is approximately -5 V when phase locked. Use a FREQ SPAN/DIV of 500 kHz or greater before measuring. If there is no difference frequency, the voltage will be about 0 V. A voltage of -13 V may indicate loss of signal from the VCO.

Narrow-band noise on the 2nd LO signal may be due to noise modulation of the 16-20 MHz VCO. Monitor the signal at the 18 MHz port to see if the oscillator signal is noisy. Noise on this line is often caused by noise on the ± 12 V lines. Use a differential oscilloscope with 1 Hz to 300 Hz bandwidth limits to check supply noise. Measure the ac differential between the supply and the 2nd LO housing. Less than 5 μ V peak-to-peak of noise will cause noticeable performance degradation. Output noise from the shaper is typically less than 5 μ V peak-to-peak.

When making power measurements of microwave circuitry, at circuit board interfaces, use a coaxial probe with very little stray inductance (see Figure 6-21). Ground the outer conductor of the probe to the circuit housing as close as possible to the measurement port. Disconnect other loads from the measurement point.

110 MHz Oscillator in the 3rd Converter

A variable capacitor, C1038, inside the cover (Figure 6-25), should only need adjusting after replacing a component or components in the 100 MHz oscillator circuit.

1. With the cover removed, connect a DVM between TP3042 and TP1011 (ground) and adjust C1038, with a non-metallic tuning tool, for a reading of +5 V. (In the 494/494P, J2042 does not have a plug on it.)

2. The Cal Amplitude adjustment, R1041, is described in the Adjustment procedure section.

Reference Lock Module

If a Frequency Reference Lock failure error message is displayed, and through troubleshooting procedure it narrows to this module, apply a 1 MHz reference signal to the back panel EXT REF Input connector or to P2025 on the Reference Lock module. If the system now locks, the timing

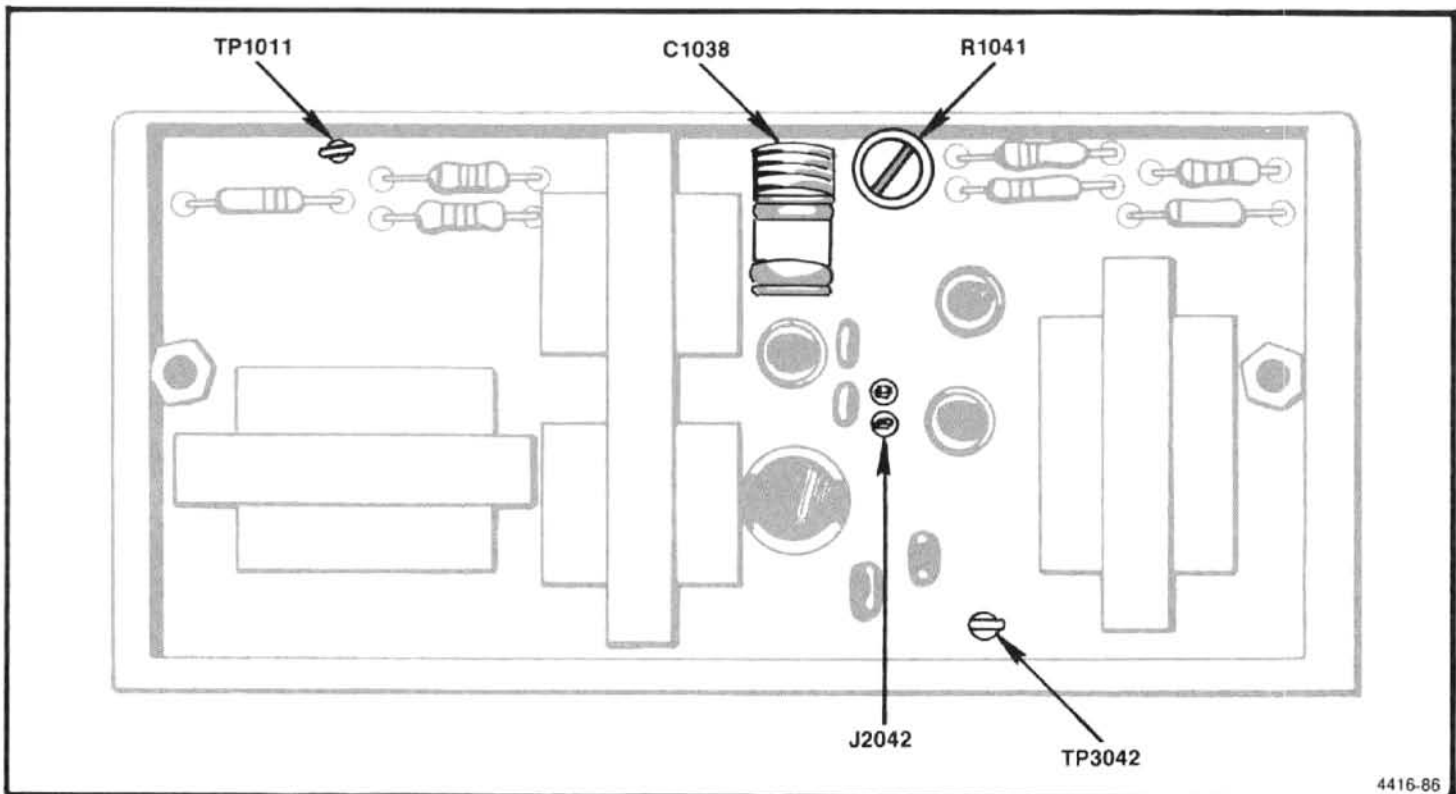


Figure 6-25. Test points and adjustments in the 3rd Converter.

circuit for the Frequency Synchronizer U2046A, needs adjusting. The procedure is as follows.

1. Switch POWER off, then use a 1/4 inch nut driver to remove the two nuts for the assembly mounting studs. Carefully lift the assembly up and back so the cover can be removed. Be careful to not unplug P2025 from the Mother board connector. (If this connector is unplugged, it may be necessary to free the Frequency Standard assembly and move it forward so the connector P2025 can be reinstalled.)

2. Remove the cover and reconnect any cables that had to be removed in order to gain access to the circuit board. Switch POWER on.

3. Connect Channel 1 of a dual channel test oscilloscope to TP1044 and Channel 2 to TP2046 (Figure 6-26). Set the deflection sensitivity to 2 V/div, Time/Div to 20 ns, and trigger the display on Channel 1 signal.

4. Adjust R2042 so the falling edge of the signal at TP1044, lags the falling edge of the signal at TP2046 by

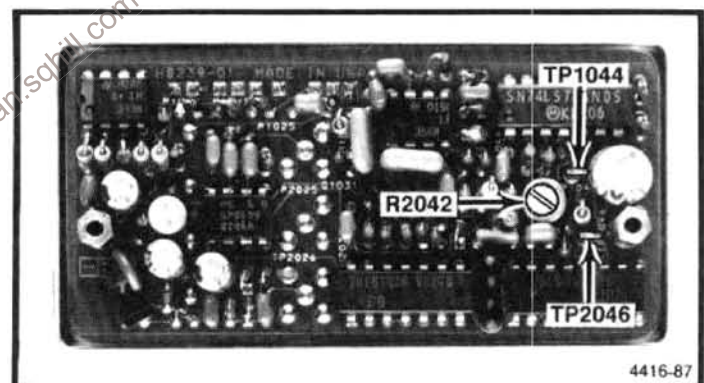


Figure 6-26. Test points and adjustments inside the Reference Lock module.

65 ns (Figure 6-27). This is to prevent U2046A from pretriggering when the input signal is some multiple of 1 MHz.

5. Check the operation to ensure the error message no longer exists and the instrument operation is normal. Re-install the cover and the assembly and again verify that the instrument operates satisfactory.

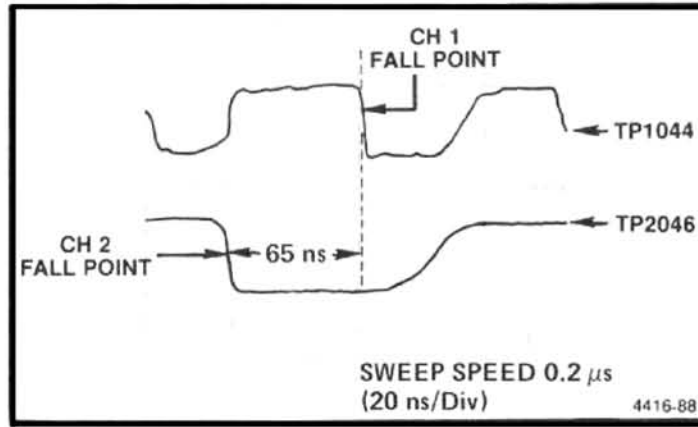


Figure 6-27. Typical display showing the delay through U2046A on the Reference Lock.

494P MICROCOMPUTER SYSTEM MAINTENANCE

INTRODUCTION

Several maintenance aids are built into the 494P microcomputer system. These are microcomputer operating test modes that demonstrate correct performance or indicate the location of a problem, if any.

The switch bank that sets up two of these test modes is described first. This is followed by instructions for the three test modes.

In the first test mode, the microcomputer executes a self-test that verifies, as much as possible, correct operation. RAM, ROM, and interface adapters are checked. Any failure found is indicated.

The second test mode hardwires the microprocessor to execute an instruction that toggles the address bus. This mode requires less of the system to run, so it may be used to troubleshoot problems that disable the first test mode.

The third test mode addresses communication between the microcomputer and the rest of the instrument. The microcomputer exercises the instrument bus to help isolate problems that, although they do not show up in the first test mode, they prevent normal instrument operation because of a breakdown in communication.

This maintenance procedure concludes with some notes on operation of several versions of instrument firmware.

INSTRUMENT TEST MODES

Memory Board Option Switch

S1038 on the Memory board informs the microcomputer at power up whether to configure itself to exercise test modes or to enable instrument modifications. Figure 6-28 shows the correct setting of the individual switches in the S1038 switch bank for normal operation.

The microcomputer reads these switches only at power-up. For a change in a switch position to take effect, the switch must be changed before the instrument is powered up.

Power-Up Self-Test Mode

The microcomputer automatically enters a self-test mode when power is switched on. S1038 chooses between two methods. Most of the power-up self-test is performed with switch 7 open; the first method. If any parts of the test fail, the results are displayed on the crt. With switch 7 open, the instrument continues operating as normally as possible after the self-test is completed.

With switch 7 closed, the instrument will not operate normally. The microcomputer performs the following steps in the order given. If a problem is found, the test is stopped and the source of the problem is indicated by a blinking LED on the Processor board. If no problem is found, this self-test takes two minutes to complete.

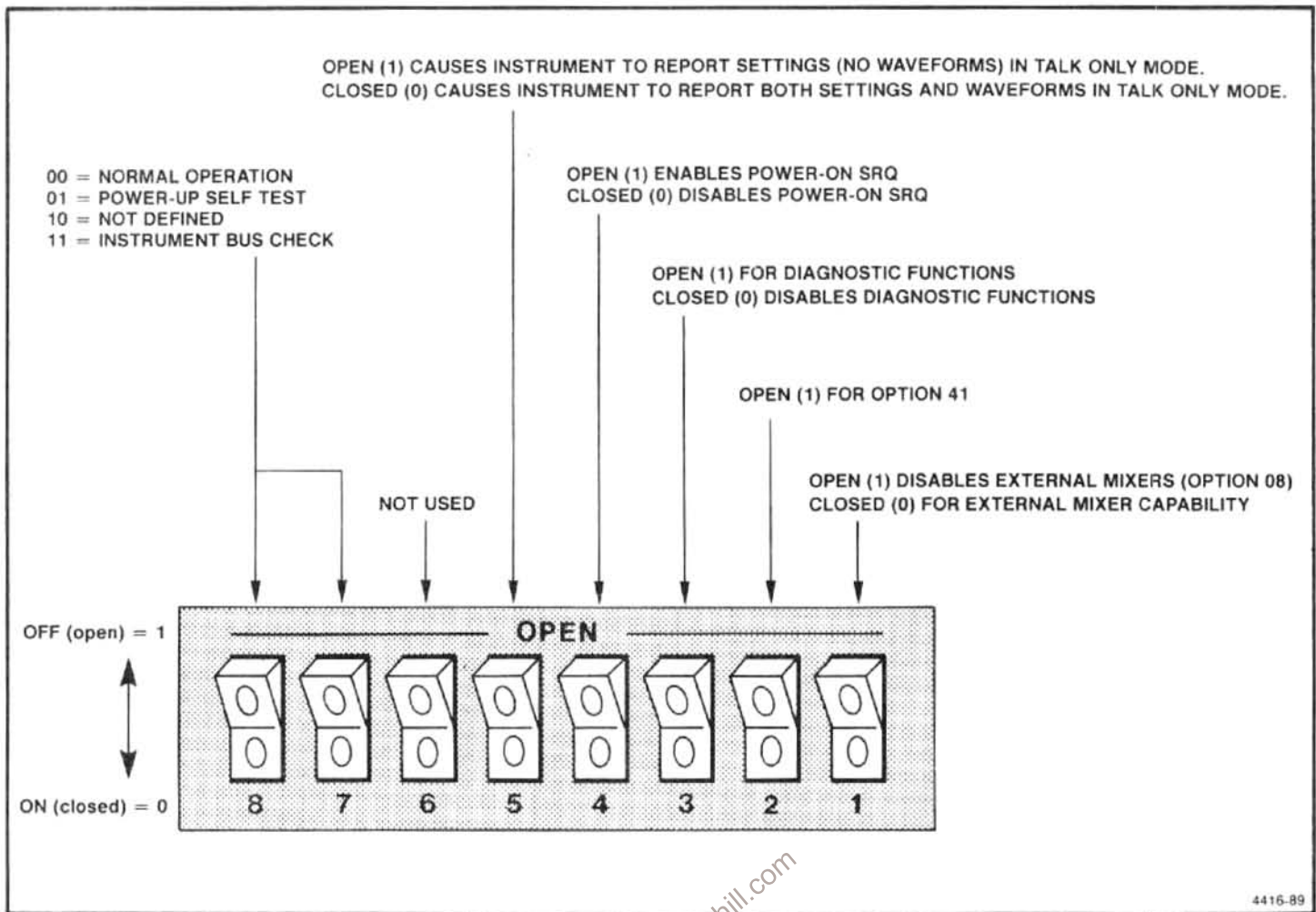


Figure 6-28. Option switch bank S1038 on the Memory board.

Addresses are specified as hexadecimal numbers in this description.

1. At power-up, the microcomputer vectors to the self-test in the ROM at the top of address space U1014 on the Memory board. The microcomputer first verifies the check sum of U1014. If the correct check sum for the ROM is not obtained when the test is run, the routine halts and blinks the ROM 9 LED, DS1049.

This step uses only U1014 and no other memory, and works the same in both self-test modes. If the test does not blink the LED and does not proceed, U1014 is probably at fault. Consider first, however, that the correct ROM must be installed, both phases of the clock on the Processor board must be present, the clock on the Processor board must be present, and the microcomputer system (exclusive of the instrument bus or GPIB) must be operating correctly. If in doubt about the 6802 microprocessor, its bus, or the microcomputer bus, skip to the instructions under Microcomputer Test Mode later in this section to exercise the microcomputer in a more simple manner.

2. The microcomputer next checks part of the instrument bus PIA, U2010, on the Processor board. The microcomputer first writes to the A control register and then reads back from the register. Next, it repeats these operations with the A data direction register. If either of these attempts fail, the routine stops and lights the bus LED, DS1046. This step works the same in both self-test modes. Following this step the message "PROCESSOR SYSTEM TEST, PLEASE WAIT" appears on the crt.

3. The microcomputer now checks the condition of RAM. This test contains three parts, the first part performs a quick test of all RAM addresses in volatile RAM (RAMs 1, 2, 3, and 4). This step does not rely on the RAM being good to execute. The microcomputer loads the bit pattern 01010101 into a RAM location, reads the location, and compares what is returned to what was stored. The microcomputer then repeats this test with the pattern 10101010.

If switch 7 is closed and an error is found on the Memory board, the microcomputer notes the failed RAM identification and sends the information to the crt to be displayed. If

switch 7 is open, it stops the test and pulses the RAM LED, DS1048, a number of times corresponding to the number of the RAM that failed the test (refer to Table 6-8).

**Table 6-8
RAM TEST**

RAM Identification	RAM Socket	DS1048 Pulses
1	U1026	1
2	U1031	2
3	U2026	3
4	U2021	4
5	U2044	5
6	U2037	6
7	U2032	7

The second part of the test is a one-minute test of all RAM (volatile and non-volatile — RAMs 1-7). The test (The Moving Inversions Test) consists of a dynamic test of all address and data functions. This test application depends on the top few bytes of RAM 7 being good. The test is performed with switch 7 open and pulses the LEDs.

Finally, another one-minute test similar to the one performed in the first part is done, with switch 7 open. In this test the memory contents are allowed to "soak" for thirty seconds before being read back and compared to what should be there.

4. The microcomputer proceeds to check sum all the ROMs. A check sum is stored in the header of each ROM. This is compared to a check sum formed by the successive 16-bit spiral sum of each byte in the ROM, starting at the third location in the ROM. The identification in the seventh byte of each ROM indicates where in the system the ROM is expected to be installed. A check is made to be sure that the ROMs are installed in the proper locations. If a ROM is installed in the wrong socket, a ROM error will result.

This step starts by looking at the part number suffix and its complement, which are stored in the fifth and sixth bytes, respectively. If these two bytes are not true complements, it is assumed that no ROM is installed at this location.

If switch 7 is closed and a bad ROM is found because of either a bad check sum or a placement error, a message is printed on the crt. Missing ROMs are not reported. If switch 7 is open, the test halts and the bad ROM is identified by pulsing ROM LED DS1047, N + 1 times, where N is the identification number of the ROM in error (e.g., a bad ROM #3

will cause four pulses; refer to Table 6-9). Missing ROMs are reported by pulsing the OK LED described in part 6.

**Table 6-9
ROM TEST
(GPIB Board Version 670-8431-00)**

ROM Identification	ROM Socket	DS1047 Board	Pulses
0	U2015	A54 Memory	1
1	U1012	A56 GPIB	2
2	U1018	A56 GPIB	3
3	U1022	A56 GPIB	4
4	U1024 ^a	A56 GPIB	5
5	U2013 ^b	A56 GPIB	6
6	U2018 ^c	A56 GPIB	7
7	U2022 ^d	A56 GPIB	8
8	U1021	A54 Memory	9
9	U1014	A54 Memory	10

^aROM #4 was U2013 on GPIB board version 670-7896-00.
^bROM #5 was U2018 on GPIB board version 670-7896-00.
^cROM #6 was U2022 on GPIB board version 670-7896-00.
^dROM #7 was not installed on GPIB board version 670-7896-00.

5. The microcomputer next tests timer IC U1016 on the Processor board. U1016 is initialized so that timer 1 will time delays, with 1 ms accuracy, and timer 3 will time delays with 8 ms accuracy. Timer 1 is then set for a 170 ms delay, and the microcomputer software delay is 169 ms. The microcomputer then checks to see if timer 1 has timed out yet. If timer 1 has not timed out, the microcomputer waits 2 ms and checks it again. Timer 1 should now be timed out. An early or late interrupt from the timer returns an error. Timer 3 is tested similarly with a 680 ms delay, checked at 672 ms and 688 ms.

If switch 7 is closed and there is a failure, a failed timer test is reported on the crt. If switch 7 is open and there is a failure, the test halts and timer LED DS1044 is lit.

This step is executed only if switch 7 is open. The microcomputer resets the GPIA, U2036, on the GPIB board and checks to see that the GPIA is not addressed to talk or listen. The GPIA is set to the listen-only mode and checked to see that it is addressed to listen. The GPIA is then set to the talk-only mode and checked to see that it is addressed to talk. If any part of this step fails, the test stops and GPIB LED DS1045 is lit.

If switch 7 is closed, the remainder of the power-up sequence is executed when the testing is completed. This puts

the instrument into the normal operating condition. When switch 7 is open and the test completes successfully, the last thing the microcomputer does is light OK LED DS1043 to indicate that the processor check is successfully complete, with no errors detected. The LED is lit continuously if no empty ROM sockets are found, or pulsed according to the number of empty ROM sockets found. If the LED blinks more times than is indicated by the number of missing ROMs, a ROM (or ROMs) failed to respond in part 4. Look for a possible problem on the chip-select line or on the MSB (bit 7) data line.

If the microcomputer seems to be good, but does not control the instrument, skip to the Instrument Bus Check Mode later in this section. There the microcomputer communication with the rest of the instrument is exercised.

Microcomputer Test Mode

Select the microcomputer test mode by moving jumper P1026 on the Processor board to the TEST position. This hardwires the 6802 data lines to hexadecimal 5F. As a result, the 6802 continuously executes a CLR B instruction, repetitively cycling through all of its address space. The spectrum analyzer will not function in this mode. It sets up a known pattern on the microcomputer address, data, and control lines and at the output of address decoders. This allows qualified service personnel to correct problems that prevent the microcomputer from running its self-test check.

Microcomputer Bus. As the microcomputer cycles through its address space, it toggles the address lines. The MSB, A15, has a period of approximately 1540 ms. The period of A14 through A0 is divided by two from the line above down to the LSB, A0, with a period of approximately 4.7 μs. High-order lines A15 through A12 are shown in Figure 6-29. Ignore the narrow pulses that may be evident during the low portion of each cycle.

The data lines on the microprocessor side of U1026 on the Processor board are static; D7 and D5 are low, the others are high. In the TEST position, P1026 disables U1026. On the other side of this buffer, the data lines are being driven by the various memory devices on the bus as they are addressed.

Examining the data lines can locate shorted or open lines; i.e., lines inactive at high, low, or in-between states or changing in unison, usually to indeterminate logic levels of +1 V to +2 V. A problem related to a particular device may be evident only while that device is addressed. Compare a problem that occurs only during a portion of the A15 cycle to the address decoder outputs in Figure 6-30.

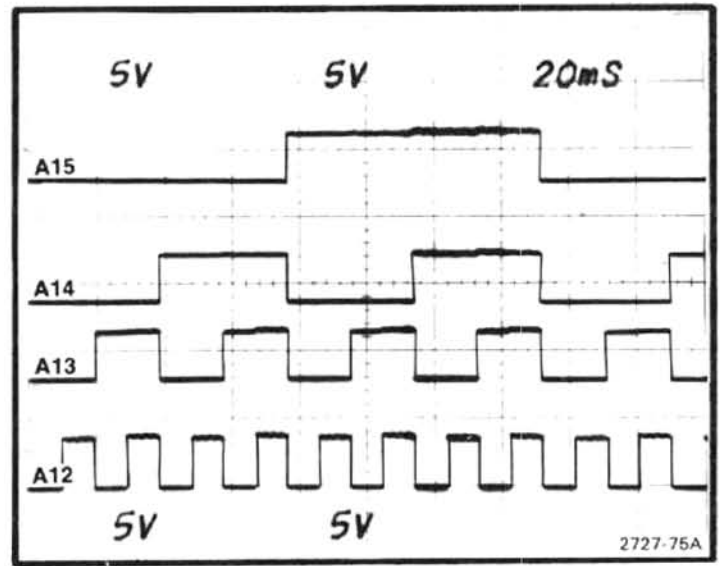


Figure 6-29. A15 through A12 in microcomputer test mode.

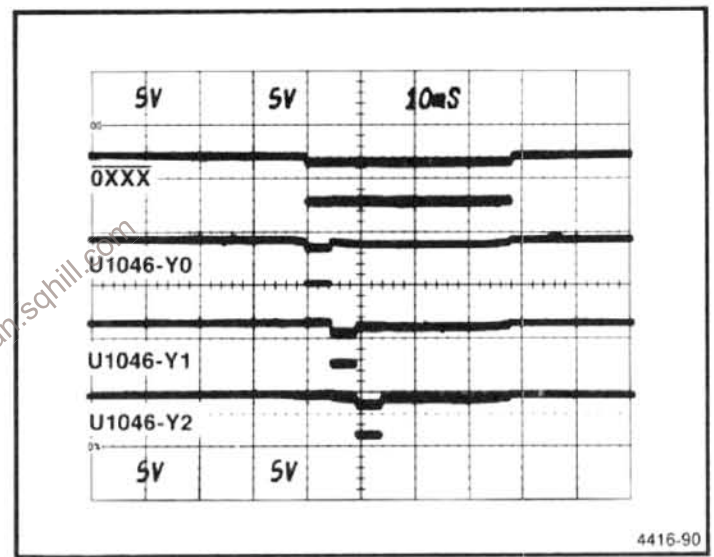


Figure 6-30. 0XXX and Y0 through Y2 of address decoder U1046 on the Memory board.

Memory Address Decoder. Address decoder U1046 on the Memory board sets its outputs low in turn to access a block of memory space. In Figure 6-30 the Y0 through Y2 outputs are compared to 0XXX. The other outputs follow in sequence with similar pulse widths. The self-test LEDs connected to the decoder outputs blink in sequence as the microcomputer cycles through its address space.

A portion of one address block decoded by U1046 is further decoded by U1041. Figure 6-31 shows the 38xx line on top and below it.

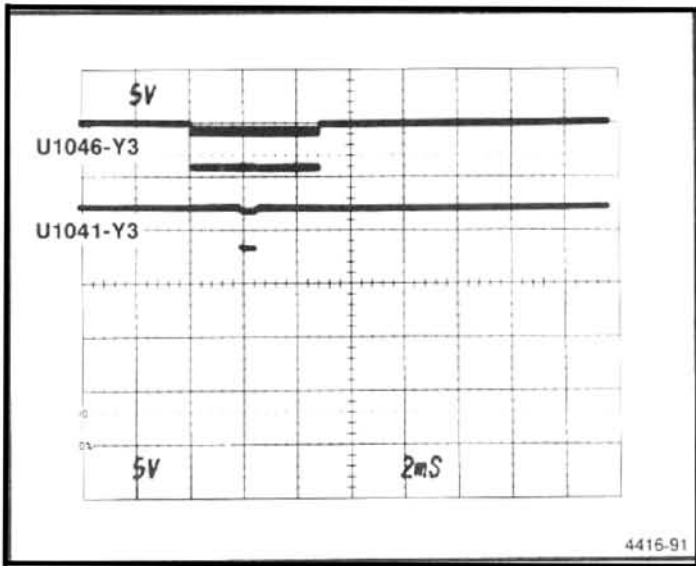


Figure 6-31. $\overline{3800}$ and Y3 of address decoder U1041 on the Memory board.

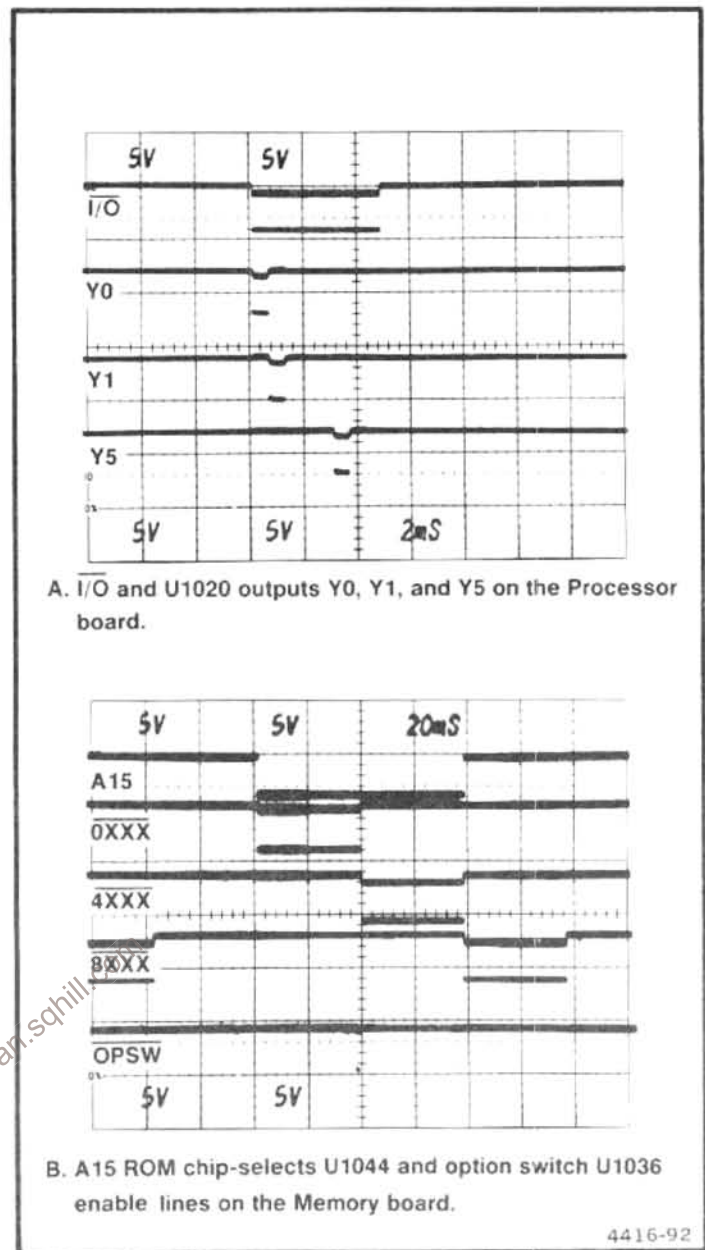
Ignore the narrow pulses evident during the time each output is asserted. The pulses result from address lines toggling between microcomputer cycles.

Address decoder U1046 on the Memory board sets its outputs low to access blocks of RAM addresses. These outputs are shown in relation to A15 in Figure 6-29. The ROM, U1044, chip-select lines and option switch register, U1036, enable lines are also shown decoded on the Memory board as shown in part B of Figure 6-32.

Processor Address Decoders. Address decoder U1020 on the Processor board decodes several chip-selects. Y0, Y1, and Y5 are shown in relation to the $\overline{I/O}$ line in part A of Figure 6-32.

GPIB Board Address Decoders. Address decoder U1032 on the GPIB board sets its outputs low in sequence while the 494P is operating in the microcomputer test mode. Y2, Y4, and Y6 are shown in relation to $\overline{I/O}$ in Figure 6-33. The ROM chip-enable lines are asserted by U1032. U1032 decodes data lines, not address lines, so it cannot be monitored in this mode.

Clocks and Control Lines. The 6802 clock lines are complementary, nonoverlapping square waves with periods of approximately $1.17 \mu s$. VMA, RESET, NMI, and R/W should be high (logic one). IRQ may be either high or low, depending on how assemblies on the instrument bus powered up.



A. $\overline{I/O}$ and U1020 outputs Y0, Y1, and Y5 on the Processor board.

B. A15 ROM chip-selects U1044 and option switch U1036 enable lines on the Memory board.

Figure 6-32. Address decoder U1020 on the Processor board and U1036 on the Memory board.

Instrument Bus Check Mode

If the microcomputer performs the power-up self-test, but fails to properly control the instrument, the instrument bus check may uncover the problem. Select the instrument bus check mode by setting the option switch as shown in Figure 6-28. The microcomputer continuously writes to the instrument bus to exercise it in a repetitive manner, so the instrument does not operate normally.

The pattern on the instrument bus toggles DATA VALID and POLL and exercises the address and data lines at sepa-

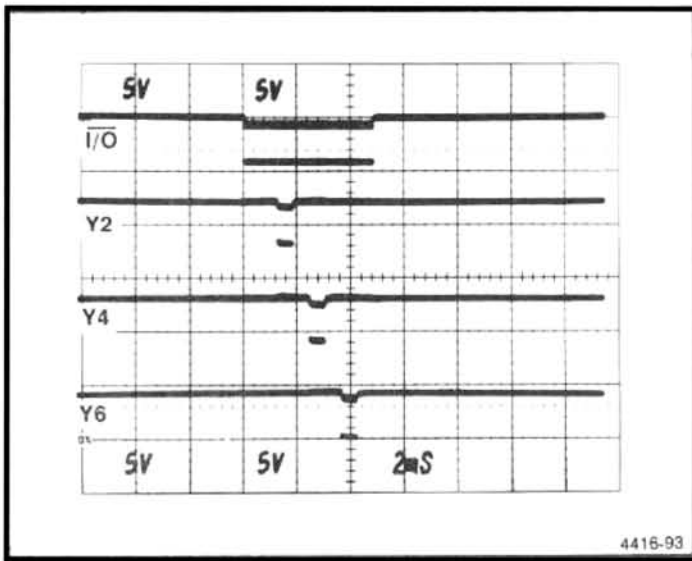


Figure 6-33. $\overline{I/O}$ and Y2 through Y4 of address decoder U1032 on the GPIB board.

rate times. The address lines change when DATA VALID is low and the data lines change when DATA VALID is high. There may be an exception on DB4 through DB0. If an assembly on the bus is requesting service because of the way it powered up, these lines may continue to change after DATA VALID goes low. In this case, an assembly or assemblies may respond to the high state of POLL and the changing state of AB7 and attempt to report status.

The pattern for the upper address and data lines is shown in Figure 6-34. Each lower order line changes at a rate that is twice the next higher line, resulting in 128 cycles on the LSB lines. The initial pulse on the upper four data lines is not part of the divide-by-two pattern and is not repeated on the lower four data lines. It is possible to discover open or shorted lines by comparing the lines to those in Figure 6-34, checking that they divide-by-two. Look for lines that stay high or low, change together or at wrong times in the pattern, or go to indeterminate logic levels (1 to 2 V).

TROUBLESHOOTING ON THE INSTRUMENT BUS

Instrument Bus Data Transfers

There are two 494P commands and queries provided to aid troubleshooting of circuit functions that are interfaced to the instrument bus. These functions are configured by data sent from the microcomputer or respond with data for the microcomputer. In either case, the data is transferred over the instrument bus. The ADDR command and ADDR? query

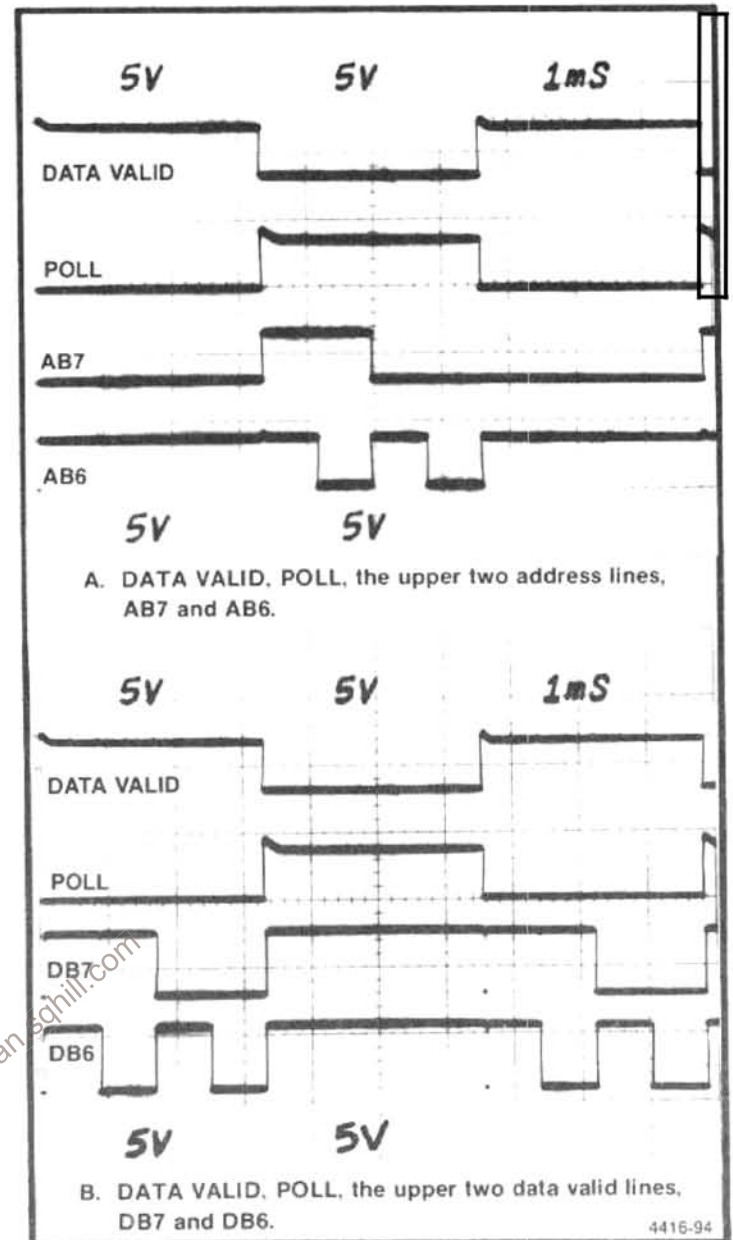
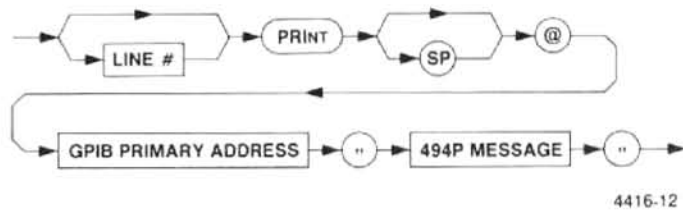


Figure 6-34. Instrument bus check.

set and return the address for the DATA command. The DATA command and DATA? query set and return data on the 494P instrument bus.

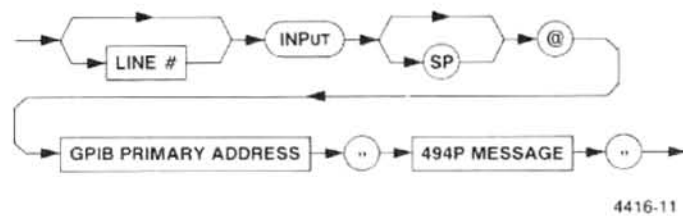
Because the DATA command can change the status of internal functions, its use may prevent normal 494P operation.

Using a 4050-Series controller, these commands and queries are transmitted to the 494P with the PRINT statement.



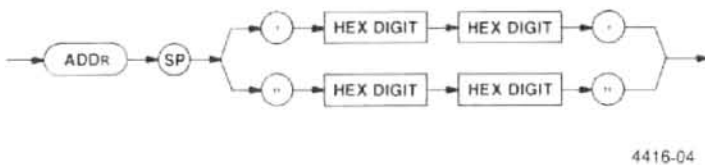
For the GPIB PRIMARY ADDRESS, enter the decimal equivalent of the 494P rear-panel GPIB ADDRESS switch settings.

The 494P response to a query is input with the INPUT statement.



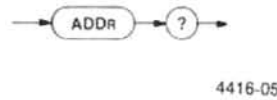
A string variable is formed by adding a dollar sign (\$) to a variable name such as A or X1, making A\$ or X1\$.

ADDR (instrument bus address) Command



HEX DIGIT—A character in the sequence 0 through 9 and A through F that represents a hexadecimal digit. The two digits (in order) form a number to represent a location on the instrument bus used by following DATA commands. If a character is not a hexadecimal digit or part of a pair of digits, it is not used to execute the ADDR command, and an error is reported.

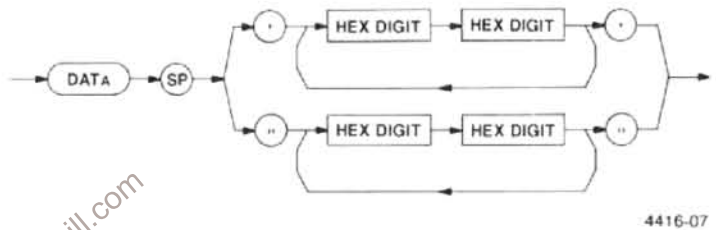
ADDR (instrument bus address) Query



Response to ADDR Query

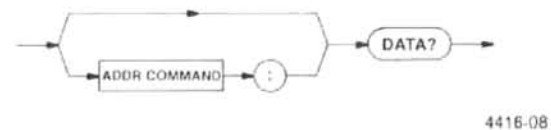


DATA (instrument bus data) Command



HEX DIGITS—As with ADDR, a pair of digits forms a hexadecimal number. The number is a data value to be sent on the instrument bus to the location specified by the last ADDR command. This allows internal 494P parameters to be set for service; these parameters control functions by setting the status or mode of 494P circuit assemblies. Up to 16 pairs of characters are accepted. If a character is not a hexadecimal digit or part of a pair of digits, the data byte formed by the pair is not executed and an error is reported. Also, an error is reported when data is sent to an invalid address.

DATA (instrument bus data) Query

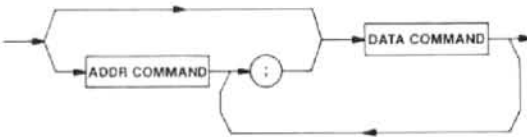


Response to DATA Query



4416-09

Combined ADDR Command and DATA Command



4416-10

The address command may precede a data command or query to identify the instrument bus location as part of the same message.

Errors related to these commands are 41, invalid DATA or ADDR argument contents, and 42, DATA direction not compatible with ADDR direction.

Instrument Bus Registers

Registers provide the link between the instrument bus and microcomputer controlled functions. The registers are defined here in the same order as they appear in the Diagrams section. The definitions are provided to help in constructing DATA commands and interpreting responses to DATA queries.

The data is presented here as binary. In some cases the data occupies the entire register width, as does a value in digital storage, for instance. In other cases, a single bit or group of bits in the register conveys a code. The upper five bits in the sweep rate and mode register indicate the sweep time/division, for instance. The meaning of the data is not fully defined here; refer to the description of the circuit module in Section 7 for details.

To use the binary data and codes presented here with the DATA command and query statements, you must convert binary to hexadecimal. The binary code number 01001011 is used as an example in the following steps.

1. Group the lower four bits and the upper four bits (break the data byte in half).

$$01001011 = 0100 \ 1011$$

2. Convert each group of four bits to a hexadecimal digit. Hexadecimal digits range from 0 to F in the sequence 0123456789ABCDEF.

$$0100 = 4$$

$$1011 = B \text{ (i.e., } 8+0+2+1=11, \text{ which is hexadecimal B)}$$

3. Group the two hexadecimal digits together, keeping their respective places.

4 and B make the two-digit hexadecimal number 4B

The information in Table 6-10 is separated by registers. The following information is related to the table information by leading alpha designators.

A. Variable Resolution (refer to diagram 20)

The microcomputer writes to two variable resolution registers. The data MSB steers the other bits that are defined into the desired register. When DB7 equals 1, it steers DB0 through DB2 to select the resolution bandwidth. When DB7 equals 0, it steers DB6 through DB0 to select the amount of gain added in the VR section and the band leveling gain (gain adjustment related to front-end response in each band). These two functions are addressed and set together by the same data byte.

B. Log and Video Amplifier (refer to diagram 23)

There are two registers that receive data from the microcomputer. One register controls video offset (78) and the other controls the display modes and the vertical scale factor (79).

C. Video Processor (refer to diagram 24)

Register 7C controls out-of-band clamping, video filtering, and leveling.

D. Digital Storage, Vertical (refer to diagram 25)

Registers 7A and FA on the Vertical Digital Storage board transfer display data to and from the microcomputer for 494P GPIB operations. Register 7B controls digital storage functions.

E. Z-Axis & RF Interface (refer to diagram 28)

Register 4F on the Z-Axis & RF Interface board enables Z-axis and RF attenuator control. Register CF reports power supply status.

F. Crt Readout (refer to diagram 30)

Register 5F controls crt readout and data steering. Register 2F accepts data from the microcomputer.

G. Sweep (refer to diagram 31)

The microcomputer writes to registers 0F and 1F to control sweep rate, mode, holdoff, interrupts, and triggering.

H. Span Attenuator (refer to diagram 32)

Registers 75 and 76 control the span attenuator.

I. 1st LO Driver (refer to diagram 33)

Register 72 controls functions on the 1st LO Driver board. Register 7E is added to make the PEAKing control programmable.

J. Preselector Driver (refer to diagram 34)

Register 77 controls functions on the Preselector Driver. The single bit DB3 responds on the data bus to indicate that the board is installed when the microcomputer performs a read at F7.

K. Center Frequency Control (refer to diagram 35)

Register 70 is provided for control functions and register 71 is provided for data values for center frequency DAC(s). A read, F0, returns the results of a comparison of the DAC output voltage and a memory voltage.

L. Auxiliary Synthesizer Control (refer to diagram 37)

Register 7D accepts data to set the synthesizer chip, U4041, to output 200 MHz to 220 MHz in 400 kHz steps. Values of R, A, and N are given to determine the output frequency as given by the formula

$$f_{out} = (1/R)(NP + A)$$

where R, the reference division ratio, is set at 5 and P is the prescale value of 32. N values needed are 31 through 34, while A ranges from 0 to 31. (Table 6-12 shows the f_{out} results for given N and A values.)

M. Phase Lock (refer to diagram 39)

Register 73 accepts data to preload the $\div N$ counter and control the synthesizer. Successive reads from register F3 obtain status and counter outputs. After resetting the counter output register selector, three read cycles return status bits and counter bits in the most significant byte and remaining counter bits in following bytes.

N. Front Panel (refer to diagram 43)

Reading from F4 accesses the keyboard encoder and the CENTER FREQUENCY knob encoder.

Table 6-10
INSTRUMENT BUS REGISTERS

Data Bits								Description
7	6	5	4	3	2	1	0	
A. Variable Resolution (3F)								
								Resolution Bandwidth
1	x	x	x	x	0	0	1	1 MHz Resolution Bandwidth
1	x	x	x	x	0	1	0	100 kHz Resolution Bandwidth
1	x	x	x	x	0	1	1	10 kHz Resolution Bandwidth
1	x	x	x	x	1	0	0	1 kHz Resolution Bandwidth
1	x	x	x	x	1	0	1	100 Hz Resolution Bandwidth
1	x	x	x	x	1	1	0	30 Hz Resolution Bandwidth
								Gain, Leveling
0	0	0	0	0	x	x	x	Band 1 Leveling
0	0	1	0	0	x	x	x	Band 2 Leveling
0	0	0	1	0	x	x	x	Band 3 Leveling
0	0	1	1	0	x	x	x	Band 4 Leveling
0	0	0	0	1	x	x	x	Band 5 Leveling
0	0	1	0	1	x	x	x	Band 6 Leveling
0	0	0	1	1	x	x	x	Band 7 Leveling
0	0	1	1	1	x	x	x	Band 8 Leveling
0	1	0	0	0	x	x	x	Band 9 Leveling
0	1	1	0	0	x	x	x	Band 10 Leveling
0	x	x	x	x	0	0	0	0 dB Gain
0	x	x	x	x	0	0	1	10 dB Gain
0	x	x	x	x	1	0	0	20 dB Gain
0	x	x	x	x	1	0	1	30 dB Gain
0	x	x	x	x	1	1	1	40 dB Gain
B. Log & Video Amplifier								
								Video Offset (78)
								LSB = 1/4 dB
								Total range = 63.75 dB
								Modes and Scale Factor (79)
1	x	x	x	x	x	x	x	Pulse stretcher on
0	x	x	x	x	x	x	x	Pulse stretcher off
x	1	x	x	x	x	x	x	Identify offset on
x	0	x	x	x	x	x	x	Identify offset off
x	x	0	1	x	x	x	x	Lin
x	x	1	0	x	x	x	x	Log
x	x	0	0	x	x	x	x	Full-screen deflection
								Log vertical scale factor in dB/div

Table 6-10 (cont)

Data Bits								Description
7	6	5	4	3	2	1	0	
C. Video Processor (7C)								
0	1	1	x	x	x	x	x	Out-of-band clamp = no clamp
0	0	1	x	x	x	x	x	Out-of-band clamp = clamp upper 5 div
1	1	1	x	x	x	x	x	Out-of-band clamp = clamp lower div
0	1	0	x	x	x	x	x	Out-of-band clamp = clamp lower 5 div
x	x	x	0	0	0	0	x	Video filter off
x	x	x	0	0	0	1	x	Video filter 30 kHz
x	x	x	1	0	0	1	x	Video filter 3 kHz
x	x	x	1	1	0	1	x	Video filter 300 Hz
x	x	x	0	0	1	1	x	Video filter 30 Hz
x	x	x	1	0	1	1	x	Video filter 3 Hz
x	x	x	1	1	1	1	x	Video filter 0.3 Hz
x	x	x	x	x	x	x	1	Base-line leveling on
x	x	x	x	x	x	x	0	Base-line leveling off

D. Digital Storage

								Input (7A)
							DB7-DB0	Data values for digital storage. A write to 7B clears the address counter so values are stored for points on the display starting at the left and proceeding to the right in order.
								Output (FA)
							DB7-DB0	Data values from digital storage. A write to 7B initializes output to begin at the left of the trace and proceed to the right.
								Control (7B)
x	x	x	x	x	x	x	x	Run storage acquisition
0	x	x	x	x	x	x	x	Halt storage acquisition
x	1	1	x	x	x	x	x	Peak/average cursor in knob position
x	1	0	x	x	x	x	x	Peak/average cursor in PEAK position
x	0	1	x	x	x	x	x	Peak/average cursor in AVERAGE position
x	x	x	1	x	x	x	x	MAX HOLD on
x	x	x	0	x	x	x	x	MAX HOLD off
x	x	x	x	1	x	x	x	B – SAVE A on
x	x	x	x	0	x	x	x	B – SAVE A off
x	x	x	x	x	1	x	x	VIEW B on
x	x	x	x	x	0	x	x	VIEW B off
x	x	x	x	x	x	1	x	VIEW A on
x	x	x	x	x	x	0	x	VIEW A off
x	x	x	x	x	x	x	1	SAVE A on
x	x	x	x	x	x	x	0	SAVE A off

Table 6-10 (cont)

Data Bits								Description
7	6	5	4	3	2	1	0	
E. Z-Axis & RF Interface								
								Z-Axis & RF Attenuator (4F)
1	x	x	x	x	x	x	x	Baseline clipper on
0	x	x	x	x	x	x	x	Baseline clipper off
x	1	x	x	x	1	x	1	0 dB RF attenuation
x	1	x	x	x	1	x	0	10 dB RF attenuation
x	0	x	x	x	1	x	1	20 dB RF attenuation
x	1	x	x	x	0	x	1	30 dB RF attenuation
x	1	x	x	x	0	x	0	40 dB RF attenuation
x	0	x	x	x	0	x	1	50 dB RF attenuation
x	0	x	x	x	0	x	0	60 dB RF attenuation
x	x	1	x	x	x	x	x	829 MHz 2nd converter
x	x	0	x	x	x	x	x	2 GHz 2nd converter
x	x	x	1	x	x	x	x	EXT MIXER
x	x	x	0	x	x	x	x	RF INPUT
x	x	x	x	0	x	x	x	100 ms to switch attenuator
								Power Supplies Status (CF)
x	x	x	x	x	x	1	x	Fault
x	x	x	x	x	x	0	x	Supplies okay
F. Crt Readout								
								Crt Control (5F)
1	x	x	x	x	x	x	x	Spectrum chop enable
0	x	x	x	x	x	x	x	Spectrum chop disable
x	1	x	x	x	x	x	x	32 characters/line
x	0	x	x	x	x	x	x	40 characters/line
x	x	1	x	x	x	x	x	2 lines
x	x	0	x	x	x	x	x	16 lines
x	x	x	x	1	x	x	x	Max span dot on
x	x	x	x	0	x	x	x	Max span dot off
x	x	x	x	x	x	1	x	Address 2F contains an address
x	x	x	x	x	x	0	x	Address 2F contains data
x	x	x	x	x	x	x	1	Readout enabled
x	x	x	x	x	x	x	0	Readout disabled to load readout
								A8 (address bit 8)
								A9 (address bit 9)
								Address/Data (2F)
								If DB1 in 5F = 1 — A7, A6 of address. With A8 and A9 in 5F, they specify the line number (0-F).
								If DB1 in 5F = 1 — A5-A0 of address. This specifies the character position in a line.
								1 = Character is a space
								0 = Character is not a space
								If DB1 in 5F = 0 — 1 = Skip a line
								0 = Don't skip a line
								If DB1 in 5F = 0 — Character code (lower 6 bits of ASCII)

Table 6-10 (cont)

Data Bits								Description
7	6	5	4	3	2	1	0	
G. Sweep								
								Sweep Rate and Mode (0F)
1	1	0	1	1	x	x	x	20 μ s Time/Div
1	0	1	1	1	x	x	x	50 μ s Time/Div
1	0	0	1	1	x	x	x	100 μ s Time/Div
0	1	0	1	1	x	x	x	200 μ s Time/Div
0	0	1	1	1	x	x	x	500 μ s Time/Div
0	0	0	1	1	x	x	x	1 ms Time/Div
1	1	0	0	1	x	x	x	2 ms Time/Div
1	0	1	0	1	x	x	x	5 ms Time/Div
1	0	0	0	1	x	x	x	10 ms Time/Div
0	1	0	0	1	x	x	x	20 ms Time/Div
0	0	1	0	1	x	x	x	50 ms Time/Div
0	0	0	0	1	x	x	x	100 ms Time/Div
1	1	0	0	0	x	x	x	200 ms Time/Div
1	0	1	0	0	x	x	x	500 ms Time/Div
1	0	0	0	0	x	x	x	1 s Time/Div
0	1	0	0	0	x	x	x	2 s Time/Div
0	0	1	0	0	x	x	x	5 s Time/Div
0	0	0	0	0	x	x	x	10 s Time/Div
1	1	1	1	1	x	x	x	Manual
0	1	1	1	1	x	x	x	External
x	x	x	x	x	1	x	x	Sets single-sweep mode
x	x	x	x	x	x	1	x	Internal reference shut down
x	x	x	x	x	x	0	x	Internal reference on
x	x	x	x	x	x	x	1	Sets trigger in single-sweep mode
								Holdoff, Interrupt, Trigger (IF)
1	x	x	x	x	x	x	x	Enables end-of-sweep interrupt
x	0	0	x	x	x	x	x	Short sweep holdoff
x	0	1	x	x	x	x	x	Medium sweep holdoff
x	1	0	x	x	x	x	x	Long sweep holdoff
x	x	x	0	0	x	x	x	Free run trigger mode
x	x	x	0	1	x	x	x	Internal trigger mode
x	x	x	1	0	x	x	x	External trigger mode
x	x	x	1	1	x	x	x	Line trigger mode
x	x	x	x	x	1	x	x	Disable SWPGATE
x	x	x	x	x	0	x	x	Enable SWPGATE
x	x	x	x	x	x	1	x	Disable trigger
x	x	x	x	x	x	0	x	Enable trigger
x	x	x	x	x	x	x	1	Aborts sweep

Table 6-10 (cont)

Data Bits								Description
7	6	5	4	3	2	1	0	
H. Span Attenuator								
								Span Magnitude (75)
								Lower 8 bits of 10-bit attenuation code (000 is max attenuation)
								Span Magnitude and Attenuator (76)
								Gain of U3032 is +1
								Gain of U3032 is -1
								X1.0 sweep decade attenuator
								X0.1 sweep decade attenuator
								X0.01 sweep decade attenuator
								1st LO main coil output select and calibration
								1st LO FM coil output select and calibration
								2nd LO output select and calibration
								For future use
								Upper two bits of attenuation code
1	x	x	x	x	x	x	x	
0	x	x	x	x	x	x	x	
x	0	0	x	x	x	x	x	
x	0	1	x	x	x	x	x	
x	1	0	x	x	x	x	x	
x	x	x	0	0	x	x	x	
x	x	x	0	1	x	x	x	
x	x	x	1	0	x	x	x	
								DB7-DB0
								DB2
								DB1, DB0
I. 1st LO Driver								
								1st LO Driver Functions (72)
								Normal span mode
								Max span mode
								Connect sweep voltage to driver
								Disconnect sweep voltage to driver
								Driver off (for degauss)
								Driver on
								Filter on at driver output (for unphase-locked narrow spans)
								Filter off at driver output
								External mixer disconnected
								External mixer connected (connected in bands 1-5 if external mixer selected; always connected in higher bands)
								Internal mixer bias for Band 1
								Internal mixer bias for Band 2
								Internal mixer bias for Band 3
								Internal mixer bias for Band 4
								Internal mixer bias for Band 5
								No internal mixer bias selected
								PEAKing Control (7E)
								Steers DB4-DB0 to upper latch
								Steers DB5-DB0 to lower latch
								1 sent to DB4 of upper latch disables front-panel PEAKing control; DB3-DB0 of upper latch and DB5-DB0 of lower latch form 10-bit input to DAC for programmable peaking voltage
0	x	x	x	x	x	x	x	
x	0	x	x	x	x	x	x	
								DB5-DB0

Table 6-10 (cont)

Data Bits								Description
7	6	5	4	3	2	1	0	
J. Preselector Driver (77)								
0	1	x	x	x	x	x	x	– Conversion, 829 MHz offset
1	0	x	x	x	x	x	x	+ Conversion, 829 MHz offset
0	0	x	x	x	x	x	x	829 MHz IF not used
x	x	1	x	x	x	x	x	Driver output filter on (for narrow spans)
x	x	0	x	x	x	x	x	Driver output filter off
x	x	x	1	x	x	x	x	Preselector switch
x	x	x	0	x	x	x	x	LPF switch
x	x	x	x	1	x	x	x	1st LO FM coil not swept
x	x	x	x	0	x	x	x	1st LO FM coil swept
x	x	x	x	x	1	x	x	Driver on
x	x	x	x	x	0	x	x	Driver off (for degauss)
x	x	x	x	x	x	x	1	3rd harmonic 1st LO conversion
x	x	x	x	x	x	x	0	1st harmonic 1st LO conversion
K. CENTER FREQUENCY Control								
								Control (70)
1	x	x	x	x	x	x	x	1st LO storage gate open
0	x	x	x	x	x	x	x	1st LO storage gate closed
x	0	x	x	x	x	x	x	Steers DAC data to 1st LO high byte
x	x	0	x	x	x	x	x	Steers DAC data to 1st LO mid byte
x	x	x	0	x	x	x	x	Steers DAC data to 1st LO low byte
x	x	x	x	1	x	x	x	2nd LO storage gate open
x	x	x	x	0	x	x	x	2nd LO storage gate closed
x	x	x	x	x	0	x	x	Steers DAC data to 2nd LO high byte
x	x	x	x	x	x	0	x	Steers DAC data to 2nd LO mid byte
x	x	x	x	x	x	x	0	Steers DAC data to 2nd LO low byte
								DAC Data (71)
						DB7-DB0		Data for center frequency DAC(s) steered by control register
								Center Frequency Control Read (F0)
						DB7		1st LO DAC stored voltage comparator
						DB0		2nd LO DAC stored voltage comparator

Table 6-10 (cont)

Data Bits								Description
7	6	5	4	3	2	1	0	
L. Auxiliary Synthesizer Control (7D)								
								DB7-DB4 Synthesizer chip data (D3-D0)
								DB2-DB0 Synthesizer chip addresses (A2-A0)
x	x	x	x	1	x	x	x	VCO enable
x	x	x	x	0	x	x	x	VCO disable
0	1	0	1	x	1	0	1	This section sets R, the reference divider to 5 yielding a 200 kHz reference frequency.
0	0	0	0	x	1	1	0	
0	0	0	0	x	1	1	1	
A	A	A	A	x	0	0	0	This section sets the value of A from 0 to 31. LSB
0	0	0	A	x	0	0	1	
N	N	N	N	x	0	1	0	This section sets N from 31 to 34. 31=1111 32=0000 33=0001 34=0010 01 10 10 10
0	0	N	N	x	0	1	1	
0	0	0	0	x	1	0	0	
M. Phase Lock Control								
								Write (73)
1	x	x	x	x	x	x	x	Clocks data on DB0 into a latch
x	x	1	x	x	x	x	x	Clears the counters
x	x	x	1	x	x	x	x	Transfers DB0 serial data to control latch outputs
x	x	x	x	1	x	x	x	Resets the counter output register selector
x	x	x	x	x	x	1	x	Transfers DB0 serial data to synthesizer N latches
								DB6 Gate mode latch
								DB2 NVRAM switch latch
								DB0 Serial data for control of synthesizer N latches
								Read (F3)—Most Significant Byte
1	x	x	x	x	x	x	x	Error voltage below a preset amount
x	1	x	x	x	x	x	x	Error voltage above a preset amount
x	x	1	x	x	x	x	x	Valid count is in counters
								DB4-DB0 Upper five bits of counter output; the remaining 16 bits are in the following two bytes
N. Front Panel								
								Reading Data From Switch Encoders (F4)
1	x	x	x	x	x	x	x	CENTER FREQUENCY down
0	x	x	x	x	x	x	x	CENTER FREQUENCY up
								DB6-DB0 Switch codes (see Figure 7-33 in Section 7)

Front-Panel Registers

Writing to register 74 loads data into shift registers that drive all the lights on the front panel, including the one for the crt graticule. Four 8-bit shift registers store the data, requiring eight writes of four bits each time (one bit for each register) to update the front-panel lights. Table 6-11 shows the order that data is entered to control the lights. A 0 turns on the light (except in the case of the crt graticule), and a 1 turns off the light.

**Table 6-11
FRONT-PANEL REGISTERS
Writing Data to Shift Registers for Lights (74)^a**

Write Number	DB5	DB4	DB2	DB1	DB0
1	not used	MAX HOLD	ZERO SPAN	GRAT ILLUM	COUNTER
2	not used	BASELINE CLIP	REMOTE	FINE	LIN
3	not used	ADDRESSED	10 dB/DIV	READY	WIDE
4	not used	READOUT	20 dB/DIV	LINE TRIG	NARROW
5	STORE SETTINGS	SHIFT	IDENT	SINGLE SWEEP	B—SAVE A
6	HELP	AUTO PEAK	MIN NOISE	FREE RUN TRIG	VIEW B
7	COUNT→CF	MAX SPAN	AUTO RESOLN	INT TRIG	VIEW A
8	Δ F	PULSE STRETCHER	UNCAL	EXT TRIG	SAVE A

^aDB3= 1—initializes encoder at power up.

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Table 6-12
AUXILIARY SYNTHESIZER TABLE OF VALUES

N Value	A Value	F _{out} Result
31	8	200.0 MHz
31	9	200.2 MHz
31	10	200.4 MHz
31	11	200.6 MHz
31	12	200.8 MHz
31	13	201.0 MHz
31	14	201.2 MHz
31	15	201.4 MHz
31	16	201.6 MHz
31	17	201.8 MHz
31	18	202.0 MHz
31	19	202.2 MHz
31	20	202.4 MHz
31	21	202.6 MHz
31	22	202.8 MHz
31	23	203.0 MHz
31	24	203.2 MHz
31	25	203.4 MHz
31	26	203.6 MHz
31	27	203.8 MHz
31	28	204.0 MHz
31	29	204.2 MHz
31	30	204.4 MHz
31	31	204.6 MHz
32	0	204.8 MHz
32	1	205.0 MHz
32	2	205.2 MHz
32	3	205.4 MHz
32	4	205.6 MHz
32	5	205.8 MHz
32	6	206.0 MHz
32	7	206.2 MHz
32	8	206.4 MHz
32	9	206.6 MHz
32	10	206.8 MHz
32	11	207.0 MHz
32	12	207.2 MHz
32	13	207.4 MHz
32	14	207.6 MHz
32	15	207.8 MHz
32	16	208.0 MHz
32	17	208.2 MHz
32	18	208.4 MHz
32	19	208.6 MHz
32	20	208.8 MHz
32	21	209.0 MHz
32	22	209.2 MHz
32	23	209.4 MHz
32	24	209.6 MHz
32	25	209.8 MHz

Table 6-12 (cont)
AUXILIARY SYNTHESIZER TABLE OF VALUES

N Value	A Value	F _{out} Result
32	26	210.0 MHz
32	27	210.2 MHz
32	28	210.4 MHz
32	29	210.6 MHz
32	30	210.8 MHz
32	31	211.0 MHz
33	0	211.2 MHz
33	1	211.4 MHz
33	2	211.6 MHz
33	3	211.8 MHz
33	4	212.0 MHz
33	5	212.2 MHz
33	6	212.4 MHz
33	7	212.6 MHz
33	8	212.8 MHz
33	9	213.0 MHz
33	10	213.2 MHz
33	11	213.4 MHz
33	12	213.6 MHz
33	13	213.8 MHz
33	14	214.0 MHz
33	15	214.2 MHz
33	16	214.4 MHz
33	17	214.6 MHz
33	18	214.8 MHz
33	19	215.0 MHz
33	20	215.2 MHz
33	21	215.4 MHz
33	22	215.6 MHz
33	23	215.8 MHz
33	24	216.0 MHz
33	25	216.2 MHz
33	26	216.4 MHz
33	27	216.6 MHz
33	28	216.8 MHz
33	29	217.0 MHz
33	30	217.2 MHz
33	31	217.4 MHz
34	0	217.6 MHz
34	1	217.8 MHz
34	2	218.0 MHz
34	3	218.2 MHz
34	4	218.4 MHz
34	5	218.6 MHz
34	6	218.8 MHz
34	7	219.0 MHz
34	8	219.2 MHz
34	9	219.4 MHz
34	10	219.6 MHz
34	11	219.8 MHz
34	12	220.0 MHz

PROGRAM FOR MOVING STORED DATA FROM THE 494P TO TAPE AND RETURNING IT TO NON-VOLATILE MEMORY

If either the Memory or GPIB boards are removed from the instrument, data stored in non-volatile memory will be lost because the back-up battery on the GPIB board is disconnected. The following program will move this data to a tape and replace the data by using a Tektronix 4050-Series Computer connected over the GPIB bus to the 494P.

```

100  PAGE
110  PRINT "ANALYZER ADDRESS IS: ";
120  INPUT A1
125  PRINT
130  PRINT @A1:"RQS OFF"
140  PRINT "SAVE NON-VOLATILE MEMORY ON TAPE? ";
150  INPUT B$
160  B$=SEG(B$,1,1)
170  IF B$<>"N" THEN 2000
175  PRINT
180  GO TO 1000

1000  REM THIS ROUTINE MOVES DATA FROM THE TAPE TO THE ANALYZER
1010  PRINT "DISPLAYS AND SETTINGS ARE ON THE FOLLOWING DATA FILES"
1020  PRINT " (2560 X 9 FOR DISPLAYS, 768 X 10 FOR SETTINGS )"
1030  PRINT
1040  TLIST
1050  PRINT
1060  PRINT "ENTER NUMBER OF FIRST DATA FILE: ";
1070  INPUT T1
1080  PAGE
1090  GOSUB 9000
1100  PRINT "REWRITE OVER ALL DISPLAYS AND SETTINGS (0), "
1110  PRINT "OR WRITE ONLY IN BLANK ..... MEMORY (1): ";
1120  INPUT Y$
1130  IF Y$="0" OR Y$="1" THEN 1160
1140  PRINT ""1" OR "2", PLEASE: ";
1150  GO TO 1120
1160  Y=VAL(Y$)
1170  HOME
1180  DELETE I$
1190  DIM I$(512)
1200  PRINT @A1:"SET?"
1210  INPUT @A1:I$
1220  W1=0
1230  PRINT @A1:"BVIEW OFF"
1240  PRINT
1250  PRINT
1260  FOR I=1 TO 9
1270  GOSUB 8000
1280  GOSUB 6000
1290  IF Z=0 THEN 1320
1300  PRINT W1;"= WAVEFORM FROM DATA FILE ";T1
1310  GO TO 1330
1320  PRINT W1;"= ..... NOT WRITTEN. ";T1;" FILE NOT USED."
1330  W1=W1+1

```

```

1340 T1=T1+1
1350 NEXT I
1360 FIND T1
1370 S1=0
1380 PRINT
1390 PRINT
1400 PRINT
1410 FOR I=1 TO 10
1420 GOSUB 5000
1430 IF Z=0 THEN 1460
1440 PRINT S1;"= SETTINGS FROM DATA FILE ";T1
1450 GO TO 1470
1460 PRINT S1;"= ..... NOT WRITTEN. ";T1;" FILE NOT USED."
1470 S1=S1+1
1480 T1=T1+1
1490 NEXT I
1500 PRINT @A1:I$
1510 PRINT
1520 PRINT
1530 PRINT
1540 PRINT
1550 PRINT "**** FINISHED ****"
1560 END

2000 REM THIS ROUTINE MOVES DATA FROM THE ANALYZER TO THE TAPE
2010 DELETE I$
2020 DIM I$(512)
2030 PRINT @A1:"SET?"
2040 INPUT @A1:I$
2050 PAGE
2060 TLIST
2070 PRINT
2080 PRINT "ENTER NUMBER OF LAST TAPE FILE: ";
2090 INPUT T1
2100 FIND T1
2110 PAGE
2120 GOSUB 9000
2130 HOME
2140 MARK 9,2500
2150 FIND T1
2160 PRINT
2170 PRINT
2180 PRINT @A1:"BVIEW OFF"
2190 W1=0
2200 FOR I=1 TO 9
2210 GOSUB 3000
2220 GOSUB 7000
2230 IF Z=0 THEN 2260
2240 PRINT W1;"= WAVEFORM SENT TO FILE ";T1
2250 GO TO 2270
2260 PRINT W1;"= ..... SKIPPED OVER. ";T1;" FILE NOT USED."
2270 W1=W1+1
2280 T1=T1+1
2290 NEXT I
2300 PRINT @A1:I$

```


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```
2310 REM SETTINGS ARE SENT TO TAPE
2320 FIND T1
2330 MARK 10,512
2340 FIND T1
2350 S1=0
2360 PRINT
2370 PRINT
2380 PRINT
2390 FOR I=1 TO 10
2400 GOSUB 4000
2410 IF Z=0 THEN 2440
2420 PRINT S1;"= SETTINGS SENT TO FILE ";T1
2430 GO TO 2450
2440 PRINT S1;"= ..... SKIPPED OVER. ";T1;" FILE NOT USED."
2450 S1=S1+1
2460 T1=T1+1
2470 NEXT I
2480 PRINT @A1:I$
2490 PRINT
2500 PRINT
2510 PRINT "**** FINISHED ****"
2520 END
```

```
3000 REM ACQUIRE WAVEFORM AND SETTINGS.
3010 REM X9 IS 500-POINT WAVEFORM, L$ IS LOWER READOUT,
3020 REM M$ IS UPPER READOUT, AND E$ IS AN ERROR MESSAGE.
3030 DELETE E$,H$,L$,M$,X9
3040 Z=0
3050 DIM H$(1100)
3060 DIM X9(500)
3070 DIM L$(50)
3080 DIM M$(50)
3090 PRINT @A1:"SAVEA OFF;DRECAL A: ",W1
3100 PRINT @A1:"ERR?"
3110 INPUT @A1:E$
3120 E$=SEG(E$,5,2)
3130 IF E$<>"62" THEN 3190
3140 V=0
3150 X9=0
3160 M$=""
3170 L$=""
3180 GO TO 3330
3190 V=1 3200 PRINT @A1:"UPRDO?"
3210 INPUT @A1:M$
3220 PRINT @A1:"LORDO?"
3230 INPUT @A1:L$
3240 M$=SEG(M$,8,40)
3250 L$=SEG(L$,8,40)
3260 PRINT @37,0:44,255,255
3270 PRINT @A1:"WFM WFID:A, ENCDG:BIN;CUR?"
3280 INPUT %A1:H$
3290 WBYTE @65:
3300 RBYTE P9,R8,R9,X9,C9
3310 WBYTE @95:
3320 Z=1
3330 RETURN
```

```

4000 REM REMOVE NON-VOLATILE SETTINGS (S$) FROM ANALYZER
4010 Z=0
4020 DELETE S$
4030 DIM S$(512)
4040 PRINT @A1:"RECALL ";S1
4050 PRINT @A1:"ERR?"
4060 INPUT @A1:E$
4070 E$=SEG(E$,5,2)
4080 IF E$<>"62" THEN 4120
4090 V1=0
4100 S$=""
4110 GO TO 4170
4120 PRINT @A1:"SET?"
4130 INPUT @A1:S$
4140 PRINT @A1:"RQS OFF"
4150 V1=1
4160 Z=1
4170 FIND T1
4180 PRINT @33:V1,S$
4190 RETURN

5000 REM RETRIEVE TAPED SETTINGS (S$) AND SEND TO NVRAM LOCATIONS (S1)
5010 Z=0
5020 DELETE S$
5030 DIM S$(512)
5040 FIND T1
5050 INPUT @33:V1,S$
5060 IF V1=0 THEN 5150
5070 IF Y=0 THEN 5120
5080 PRINT @A1:"RECALL ";S1;"RQS OFF;WAIT;ERR?"
5090 INPUT @A1:E$
5100 E$=SEG(E$,5,2)
5110 IF E$<>"62" THEN 5150
5120 PRINT @A1:S$
5130 PRINT @A1:"STORE ";S1;"RQS OFF"
5140 Z=1
5150 RETURN

6000 REM SEND WAVEFORM (X9) & READOUTS (M$,L$) TO NVRAM LOCATION (W1).
6010 Z=0
6020 IF V=0 THEN 6180
6030 IF Y=0 THEN 6080
6040 PRINT @A1:"SAVEA OFF;DRECAL A: ";W1;"ERR?"
6050 INPUT @A1:E$
6060 E$=SEG(E$,5,2)
6070 IF E$<>"62" THEN 6180
6080 PRINT @A1:"WAIT;TRI?"
6090 INPUT @A1:H$
6100 PRINT @A1:"RDOUT ";M$;" "
6110 PRINT @A1:"RDOUT ";L$;" "
6120 PRINT @A1:"WFM WFID:A,ENCDG:BIN;SIG;SAVEA ON"
6130 WBYTE @33:64,X9,-1
6140 WBYTE @63:
6150 PRINT @A1:"DSTORE A: ",W1

```

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6160 PRINT @A1:H$
6170 Z=1
6180 RETURN

7000 REM STORE READOUTS (M$,L$), AND WAVEFORMS (X9) ON TAPE FILE (T1).
7010 FIND T1
7020 M$=M$
7030 L$=L$
7040 PRINT @33:V
7050 PRINT @33:M$
7060 PRINT @33:L$
7070 PRINT @33:X9;
7080 RETURN

8000 REM RETRIEVES READOUTS (M$, L$), AND WAVEFORM (X9)
8010 REM FROM THE SELECTED TAPE FILE.
8020 FIND T1
8030 DELETE X9
8040 DELETE M$
8050 DELETE L$
8060 DIM X9(500)
8070 DIM M$(50)
8080 DIM L$(50)
8090 INPUT @33:V
8100 INPUT @33:M$
8110 INPUT @33:L$
8120 INPUT @33:X9
8130 RETURN

9000 REM THIS ROUTINE SHOWS THE CONTENTS OF NVRAM DISPLAYS AND SETTINGS
9010 PRINT "NON-VOLATILE DISPLAY MEMORY"
9020 PRINT "-----"
9030 PRINT @A1:"RQS OFF"
9040 DELETE S$
9050 DIM S$(512)
9060 PRINT @A1:"SET?"
9070 INPUT @A1:S$
9080 W1=0
9090 FOR I=1 TO 9
9100 PRINT @A1:"SAVEA OFF;DRECAL A: ";W1
9110 PRINT @A1:"ERR?"
9120 INPUT @A1:E$
9130 E$=SEG(E$,5,2)
9140 IF E$="62" THEN 9170
9150 PRINT W1;"= WAVEFORM"
9160 GO TO 9180
9170 PRINT W1;"= ..... "
9180 W1=W1+1
9190 NEXT I
9200 REM NOTE: "RECALL" MAY RECALL A RQS-ON STATE, SO THIS MUST BE
9210 REM TURNED OFF AGAIN BY A "RQS OFF" STATEMENT.
9220 PRINT
9230 PRINT "NON-VOLATILE SETTINGS MEMORY"
9240 PRINT "-----"

```

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```
9250 S1=0
9260 FOR I=1 TO 10
9270 PRINT @A1:"RECALL ";S1;"RQS OFF;WAIT"
9280 PRINT @A1:"ERR?"
9290 INPUT @A1:E$
9300 E$=SEG(E$,5,2)
9310 IF E$="62" THEN 9340
9320 PRINT S1;"= SETTINGS"
9330 GO TO 9350
9340 PRINT S1;"= ..... "
9350 S1=S1+1
9360 NEXT I
9370 PRINT
9380 PRINT @A1:S$
9390 RETURN
```

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THEORY OF OPERATION

This section of the manual describes the circuitry in the 494/494P Spectrum Analyzer. The section begins with a general or functional description of the major circuit blocks and systems that make up the 494/494P. This is followed by a more detailed description of the circuitry within each block or section, for example; the display section.

The number in the diamond that is adjacent to the section title refers to the corresponding schematic diagram number. Note that these same numbers are included on diagrams to designate the interconnection between circuits, or, in the case of block diagrams, to the more detailed diagram of that block. Schematic diagrams of the circuits are part of Volume 2, section 10.

FUNCTIONAL AND GENERAL DESCRIPTION

What It Does

The 494/494P Spectrum Analyzer accepts an electrical signal as its input and displays the signal's frequency components on a crt. Signals can be applied directly to the RF INPUT or, if the analyzer is equipped for external mixer operation, to an external mixer, which extends the measurement range of the 494/494P.

The display of the frequency components of the input signal appears on the crt as a graph where the horizontal axis is frequency and the vertical axis is amplitude. The display can be plotted, if desired, by connecting a chart recorder through rear-panel connectors. If the instrument is programmable, the display can also be transmitted digitally via the IEEE 488 bus to a GPIB plotter.

Manual operation of the 494/494P Spectrum Analyzer is accomplished with front-panel controls and switches. The 494P (programmable version) can also be operated via the IEEE 488 bus using a straightforward language format.

How It Works

A functional block diagram, located at the front of the Diagrams section in Volume 2, shows how the major sections in the instrument relate and the paths of most major signals. Refer to the diagram while reading this general description.

The 494/494P operates as a swept, narrow-band receiver. As it sweeps or spans a range of frequencies, it moves the crt beam horizontally. When a frequency component of an input signal is detected the beam is deflected

vertically as a function of input power at that frequency. The center frequency of each span is set by the CENTER FREQUENCY control or FREQUENCY entry via a Data Entry keyboard. The frequency range of each span is set by the FREQ SPAN/DIV control or settings. The power level, represented by the top of the screen, is set by either the REFERENCE LEVEL control or the Data Entry keyboard.

First, Second, and Third Converters

In the 494/494P Spectrum Analyzer, this swept-frequency analysis is achieved by means of a triple-conversion superheterodyne technique. Each of three frequency converters consist of a mixer, a local oscillator, and appropriate filters. Only one frequency is converted in each mixer to pass through band-pass filters to the detector. This frequency can be changed by changing the frequency of the local oscillators in any one of the converters.

The first converter, usually referred to as the front end, converts the input signal frequency to an intermediate frequency (IF) of either 829 MHz or 2072 MHz, depending on which band is in use. The internal mixer converts signals from 10 kHz to 21 GHz, and external mixers may be used for signals in the millimeter wavelengths. When the internal mixer is used, a preselector or low-pass filter is inserted in the signal path to reduce unwanted signals or images and spurious responses from cluttering the display.

One of two second converters is selected automatically for each band so the input frequency range does not overlap the first IF frequency. Each second converter has its own local oscillator (LO), mixer, and filters. Both down-convert the signal to 110 MHz which is sent to the third converter.

The third converter amplifies the 110 MHz IF signal and converts it to the final intermediate frequency of 10 MHz. The third converter passes the signal to the main IF section for processing and detection.

IF Section

In this section the signal is processed for frequency resolution. Three functions are performed here:

1. Weak signals can be amplified, by switchable amplifiers, so the vertical window (dynamic display range) is shifted up or down. The REFERENCE LEVEL selects the gain and input RF attenuation to frame this window between the top of the display screen or reference level, in dBm or volts, and the bottom of the display.

2. The signal is processed through one of several 10 MHz band-pass filters that can be selected by the RESOLUTION BANDWIDTH control. In the auto mode the microcomputer will select the best combination of bandwidth and sweep time for the selected span, unless overridden by the operator.

3. The signal is amplified by a logarithmic then detected. The output from this detector is a voltage that corresponds to the signal strength, in decibels, which is sent to the vertical channel of the display section to drive the vertical axis of the crt and display the strength of the signal.

Display Section

The display section drives the X, Y, and Z axis of the crt display. Vertical deflection of the beam is increased as the output of the amplitude detector increases. The horizontal position of a signal is controlled by the frequency control section and corresponds to the frequency analyzed at that instant. As the 494/494P spans from low to high frequencies during its analysis, the beam is swept from left to right. When the analyzer tunes through a signal frequency, a vertical deflection shows the strength of the signal. This signal is therefore displayed at a position on the span that corresponds to its frequency, or, the display is one of amplitude as a function of frequency.

The video amplifier scales the output of the detector for vertical deflection in dB/div or performs a log/linear conversion, depending on the vertical display mode. The video processor filters the video if either the wide or narrow filter is selected.

The display section also drives the crt readout to show control settings. This readout is based on data from the

microcomputer which is reading the settings of the front panel controls or data on the GPIB bus.

The sweep is usually fast enough so the display is flicker-free, but at times the sweep must be slowed below the flicker rate. With digital storage the display can be recorded and refreshed at a flicker-free rate. The 494P can read-out the display data, from digital storage, through the IEEE 488 interface.

Frequency Control Section

The 494/494P sweeps through a frequency range that is centered about a frequency set by the frequency control section. The CENTER FREQUENCY control sets the center frequency of either the 1st or 2nd local oscillator.

The output of a sweep generator is scaled by a span attenuator to sweep a range or span of frequencies either side of center. The output of the span attenuator drives the 1st LO for wide spans and the 2nd LO for narrow spans. The output sweep also deflects the crt beam across the horizontal axis as the local oscillators are swept so the display is a spectrum of frequency versus power.

The frequency control section also tunes the preselector so it tracks the signal frequency being detected over the 1.7 to 21 GHz range.

Microwave Counter and Phase Lock Section

The microwave Counter, Harmonic Mixer, and Auxiliary Synthesizer comprise the nucleus of the frequency control hardware. Both the 1st LO and 2nd LO frequencies are controlled via the firmware based control loop. Data from the Counter, is used as feedback to control the oscillator frequency. Accurate signal frequency measurement is also possible by counting the frequency of the 3rd IF.

The Phase Lock system stabilizes the 1st LO frequency to minimize FM'ing or display jitter and increase resolution.

Digital Control Section

Operational modes and internal functions of the 494/494P analyzer are selected and controlled directly from the front panel or remotely controlled from an external controller through a IEEE 488 connector. This connector interfaces to an instrument microcomputer through a General Purpose Interface Bus (GPIB). The modes and functions that are selected are processed and activated by the instrument master microcomputer which talks and listens to all circuits over the instrument bus.

Front panel control and selector data is processed by a front panel CPU that interfaces with the master micro-computer over the instrument bus. The master micro-computer receives and sends all of its information over the instrument bus to the internal circuits. It communicates with the outside world through the GPIB to the IEEE Std 488 connector or through the Accessories Interface to the Accessories connector located on the rear panel. Control language corresponds to front-panel nomenclature of the 494/494P Spectrum Analyzer.

Power Supply Section

The power supply section provides regulated dc power and forced air cooling for all circuits within the instrument. The switching supply is capable of providing regulated voltages over wide input line frequency and voltage ranges. The cooling system consists of an intake on the bottom of the case, air passages within the instrument, a fan, and a rear panel exhaust. Air is routed to all section of the instrument in proportion to the heat generated by circuits within that section. Internal temperature variation is small so as to provide reliable operation.

Other Sections

Signal, power, and control lines between circuit boards and assemblies interconnect through a common Mother board. Most circuit board assemblies plug onto the the top

side of the Mother board, assemblies or modules, such as oscillators, of the RF deck, plug through cables and connectors to the bottom side of the Mother board.

Timer (Running time indicator)

An electromechanical timer (M1019) is installed on the Z-Axis board. This timer is calibrated for a duration of 5000 operating hours. Current through the timer causes a copper band to progress along a scale to indicate operating hours.

For Further Information

The circuits that make up the different sections of the 494/494P are described under headings that correspond to those shown in the Functional Block diagram. Detailed block diagrams of these main sections follow the Functional Block diagram. All diagrams are located in the Diagrams section of Volume 2. Detailed block diagrams and circuit schematics of each circuit board and assembly within a section follow the breakdown of the sections.

Circuit theory of operation is described under the Detailed Description that follows. Adjacent to each schematic is a detailed block diagram and a parts location illustration with look-up tables. The parts location illustration and look-up tables should aid in finding components on either the schematic or parts location illustration.

DETAILED DESCRIPTION

The following description is arranged by sections or systems; such as 1st Converter, 2nd Converter, etc., followed by circuit analysis of the circuits within that section. Each system/section is introduced with a description of the system using the system block diagram found in the Diagrams

section of the manual. This is followed by a description of each circuit board or major circuit within the system. Adjacent to the title of each section or part is the diagrams number.

1ST CONVERTER ASSEMBLIES



The 1st Converter consists of the following assemblies: The 0-60 dB Step Attenuator, the Filter Select switch, a 2 GHz Limiter and 1.8 GHz Low-Pass Filter, a 1.7 to 21 GHz Preselector, the Mixer, the 1st LO and Power Divider, Transfer Switch, 2.072 GHz Directional Filter, Diplexer and two 4.5 GHz Low-Pass Filters. External circuits that control or drive the assemblies within the 1st Converter are: the Preselector Driver, 1st LO Driver, Microwave Counter and Phase Lock system, and the RF Interface board.

The 1st Converter converts the incoming RF signals to the 1st IF. Incoming signals are applied through a calibrated 0-60 dB decade attenuator to a filter select switch. Signals within band 1 (10 kHz-1.8 GHz) are routed through a limiter and 1.8 GHz low-pass filter to the mixer, signals within bands 2 through 5 (1.8-21 GHz) are routed through a tunable preselector to the mixer. The RF signals are mixed with the output from a tunable (2.072-6.329 GHz) local oscillator to generate modulation products at the intermediate frequency in use.

The output of the 1st mixer is applied, through Transfer Switch S13, to a directional filter which separates intermediate frequencies 2.072 GHz and 829 MHz for the 2072 MHz 2nd Converter or 829 MHz 2nd Converter. The 2072 MHz IF is applied through a 4.5 GHz low-pass filter to the 2072 MHz 2nd Converter to reject the re-entrant modes of the directional and four cavity band-pass filters. The 829 MHz IF is fed through a diplexer and a 4.5 GHz low-pass filter before it is applied to the 829 MHz IF stages. The 4.5 GHz filter is used to reject re-entrant modes of the 829 MHz band-pass filter internal to the 829 MHz 2nd Converter.

An EXTERNAL MIXER port permits an external mixer to be connected to the instrument to serve as the 1st IF source. The IF signals from external mixers are routed through the Transfer switch to the Directional Filter. This feature is primarily for use with waveguide mixers.

Two intermediate frequencies (2072 MHz and 829 MHz) are used in the analyzer to prevent baseline rise caused by local oscillator feedthrough and crossover of intermodulation products. The 2072 MHz IF is selected for bands 1 and 5, plus the waveguide bands. 829 MHz IF is selected for bands 2-4.

RF Interface Circuits



The RF interface circuits receive instruction from the microcomputer and produce control voltages that drive the RF Attenuator, the Transfer Switch, and the IF Select.

These circuits are located on the Z-Axis board and their operation is described under the Z-Axis board part of the Display section.

RF Signal Path



The 0-60 dB Step Attenuator consists of 10 dB, 20 dB, and 30 dB sections which are controlled by relays that are actuated by voltages from the RF Interface circuit.

Coaxial relays S11 and S12 select either the low-pass filter (FL10) and limiter or the Preselector and 3 dB attenuator (AT11) for the RF signal path. The relay coils are driven by circuitry on the Preselector Driver board. The low-pass filter path is used for band 1, band 2 through 5 (signals with frequencies 1.7 to 21 GHz) are routed through the Preselector.

The 2 GHz Limiter operates from 100 kHz to 2 GHz. It has a linear two-port transfer characteristic of unity (-1 dB) until the input exceeds +5 dBm. Above this point, the internal detector diodes conduct, reflecting part of the RF input energy back to the source. As the input level rises, the Limiter reflects more signal, limiting the amount that can pass through the mixer, thus protecting the mixer from burnout.

The 1.8 GHz low-pass filter (FL10) strips the incoming signal of any frequencies above 1.8 GHz and passes the signal below 1.8 GHz to the output segment of selector switch S11.

The Preselector is a 1.7-18 GHz YIG filter that provides high selectivity and image-frequency rejection. Tuning current, which is near 500 mA at 21 GHz, is provided by the Preselector Driver circuits. The Preselector operates on bands 2, 3, 4, and 5. The signal from the Preselector passes through a 3 dB attenuator to the output section of the Filter Selector switch. The Preselector is sensitive to output load impedance so an attenuator is used to help isolate this loading.

1st Mixer

The 1st Mixer is a single balanced design. This has less conversion loss, in comparison to an unbalanced mixer, and this design also cancels local oscillator feedthrough to the RF port. The local oscillator input is split through a broadband multi-section coupler whose outputs are equal in power but 90° out of phase. An additional 90° phase shift is cascaded with the appropriate signal to create a 180° phase difference that is applied across a pair of series-con-

nected Schottky diodes. The result is that the diodes are alternately switched on and off as the local oscillator cycles.

The node between the two diodes is isolated from the 1st LO input by about 30 dB so the RF input is applied to this node. The blocking capacitor at the input connector permits broadband signal application from the RF port, while blocking the dc diode bias to the RF port and the analyzer input. Dc bias for the mixer is via the Transfer Switch, Directional Filter, Diplexer, and 4.5 GHz Filter through the 829 MHz IF circuits. Bias return is through assembly A11 to ground. Bias is supplied from the 1st LO Driver board.

Not counting the IF filtering circuitry, the fundamental conversion loss of the 1st Converter is about 14 dB; third harmonic conversion loss is about 24 dB. The Schottky diodes are mounted in a sub-assembly of the mixer so they can be easily replaced.

1st Local Oscillator

The 1st LO is a YIG (Yttrium-Iron-Garnet) oscillator that has a tuning range of 2.072 to 6.35 GHz. The oscillator assembly includes the interface circuit board that couples operating and tuning voltages from the 1st LO Driver, Span Attenuator, and Error Amplifier circuits to the oscillator.

The +15 V₁ voltage provides operating bias for the oscillator. The supply is protected and decoupled by VR1010, C1016, and R1011. The second supply, +15 V₂, is for future applications. VR1018 and VR1019 clamp transient voltages from the tune voltage coil. It also protects the driving circuits from the transients induced when degaussing.

Relay K1015 is closed when the FM coil is used to sweep the oscillator. C1012 and C1014 are connected across the tune coil to lower the noise bandwidth of the main coil driving circuit while the FM coil is in operation. The heater provides temperature stability.

Power Divider (A13)

The Power Divider splits the output of the 1st LO (YIG oscillator) to isolate the 1st Mixer from the 1st LO OUTPUT

front panel connector. The unit is essentially two multi-section directional couplers that are multi-port cascaded to produce two ports having equal power. The isolation between output ports is 15 dB or more at the operating frequency. The Power Divider also provides an improved load to the local oscillator.

Transfer Switch

The Transfer Switch is a three-port coaxial switch that permits application of 1st IF signals from inside or outside the analyzer. This allows the use of an external mixer by bypassing the 1st Converter circuitry. The function is controlled by circuitry on the RF Interface board. It is automatically actuated when waveguide bands are selected or the front panel EXT MIXER push button is pressed.

Directional Filter

The Directional Filter (FL16) couples the 2072 MHz signal to the 2nd Converter via low-pass and band-pass filters, FL11 and FL14. As mixing products pass through FL16, they induce a selected current into a one-wavelength distributed ring, which couples the 2072 MHz IF signal out to the low-pass filter FL11. The remainder of the IM products pass on through, since the ring is excited only with 2072 MHz signals. The bandwidth of this unit is approximately 45 MHz. The unfiltered signals are passed on to the Diplexer.

2072 MHz IF Filters

The 2072 MHz signal, from the Directional Filter, passes through a low-pass filter (FL11) which rejects all signals above 4.5 MHz. The signal is then sent through a 15 MHz band-pass filter (FL14) which rejects IM products either side of the 2072 MHz IF.

Diplexer and Filter

The Diplexer (A14) passes the 829 MHz IF signal from the mixer output through a low-pass filter (FL15) to the 2nd Converter. The Diplexer and directional filter provide a broadband impedance match to the 1st Mixer IF port. This match contributes to the overall flatness and frequency response of the analyzer.

2ND CONVERTER CIRCUITS



Two 2nd Converter systems are used in the 494/494P Spectrum Analyzer. One converts 2072 MHz to 110 MHz and the other converts 829 MHz to 110 MHz. The operation of either converter is a function of the selected frequency band. The IF selection for each band is shown in Table 7-1 along with the center frequency range and the local oscillator frequency range. Two 2nd IF's are used by the analyzer for the following reasons:

1. If a frequency band were to include the first intermediate frequency within its range, it is possible for some input signals to pass through the Preselector and the 1st Converter (without conversion), into the 2nd Converter at the 1st intermediate frequency. The resultant spurious signal will cause the baseline level on the screen to rise and obscure real signals. By the use of two 2nd converters, the analyzer can overlap frequency bands so they do not include the first intermediate frequency, and avoid this problem.
2. With two IF'S, IF feedthrough in band 2 and higher order spurs in bands 3 and 4 can be eliminated.
3. Because of the limited tuning range of the 719 MHz LO, the lower IF cannot be used above band 4.

The 2072 MHz 2nd Converter mixes the 2072 MHz from the 1st Converter with the output from a 2182 MHz phase-locked 2nd local oscillator. This local oscillator is swept and tuned over a 4 MHz range. The 2072 MHz input IF signal is

passed through a four-cavity band-pass filter (FL14) to allow only the 2072 MHz 1st IF signal to pass through and prevent other signals, generated within the 2nd Converter, from getting back to the 1st Converter. A diode mixer combines the 2072 MHz IF input and the local oscillator signals to generate the 110 MHz IF output which then passes through a 110 MHz low-pass filter to reject any higher order signals from the mixer.

The 829 MHz 2nd Converter uses a phase-locked voltage controlled oscillator to produce the 719 MHz signal that is mixed with the 829 MHz first IF signal. The swept 2182 MHz 2nd Local Oscillator is used as a reference for the phase locked oscillator. The 719 MHz oscillator can be disabled upon command from the microcomputer in the IF selection process. The phase lock circuit maintains a constant relationship between the two local oscillators as the 719 MHz oscillator is swept and tuned over a 1.33 MHz range. A four section coaxial band-pass filter is used before the mixer to exclude any RF signals other than the desired 829 MHz. Again, a diode mixer is used to mix the 829 MHz input and local oscillator signals to produce the 110 MHz second IF output.

Selection between the two IF signals also takes place within the 829 MHz converter system. Under command of the microcomputer (by way of the RF Interface circuits) a diode selector switching network connects one of the two 110 MHz second IF signals to the output for application to the 3rd Converter.

Table 7-1
2ND CONVERTER IF SELECTION

Frequency Band	Center Frequency Range	2nd Local Oscillator Frequency (MHz) Range	Converter System IF
1	0-1.8 GHz	2182 ± 2.25	2072 MHz
2	1.7-5.5 GHz	719 ± 0.75	829 MHz
3	3.0-7.1 GHz	719 ± 0.75	829 MHz
4	5.4-18.0 GHz	719 ± 0.75	829 MHz
5	15.0-21.0 GHz	2182 ± 2.25	2072 MHz
6	18.0-26 GHz	2182 ± 2.25	2072 MHz
7	26-40.0 GHz	2182 ± 2.25	2072 MHz
8	40.0-60.0 GHz	2182 ± 2.25	2072 MHz
9	50.0-0.0 GHz	2182 ± 2.25	2072 MHz
10	75-40.0 GHz	2182 ± 2.25	2072 MHz
11	110-220 GHz	2182 ± 2.25	2072 MHz
12	170-325 GHz	2182 ± 2.25	2072 MHz

2072 MHz 2ND CONVERTER



The 2072 MHz 2nd Converter converts the 2072 MHz signal output from the 1st Converter to 110 MHz for eventual application to the 3rd Converter. The assembly consists of a low-loss, narrow band, four-cavity filter, connected, through an external cable, to a low conversion loss narrow band diode mixer, a 110 MHz low-pass filter, and a mixer biasing circuit that will disable the mixer when directed by the microcomputer.

Four-Cavity Filter

The four-cavity (band-pass) filter, which is depicted on Diagrams 11, 12, and 13, is designed to pass only the 2072 MHz IF signal to the mixer and to reflect any other frequencies back to the 1st Converter for termination. In addition, the filter keeps the converter LO and mixer products from entering the 1st Converter.

This filter has a 1 dB bandwidth of 15 MHz and an insertion loss of 1.2 dB. Each end resonator is capacity coupled to external circuits through a coupling hat plugged into a 3 millimeter connector. Intercavity coupling is provided by

coupling loops that protrude from the machined filter top. The resonant frequency of each cavity is determined primarily by the depth of a gap in the underside of the filter top, and is fine tuned with a tuning screw on the side of each cavity. All of the tight machining tolerances are confined to the top. Thus, the main cavity milling need not be a high precision part. When properly tuned, using a network analyzer, the filter return loss is greater than 25 dB from either end (in a 50 Ω system). Figure 7-1 shows a cross sectional view of the filter; Figure 7-2 shows the equivalent electrical circuit.

Mixer Circuit

The mixer circuit in the 2072 MHz 2nd Converter is of the single-balanced, two diode type. It consists of the mixer, an operational amplifier bias circuit, a delay line, and a low-pass filter. In operation, both diodes of the mixer are turned on and off by the output signal from the 2182 MHz 2nd Local Oscillator through coaxial connector P183. Although the diodes are connected for opposite polarity, both are turned on at the same time because of the 180° phase shift delay line in the input line to the upper deck. Note that the diodes are matched and must be replaced as a pair if one fails.

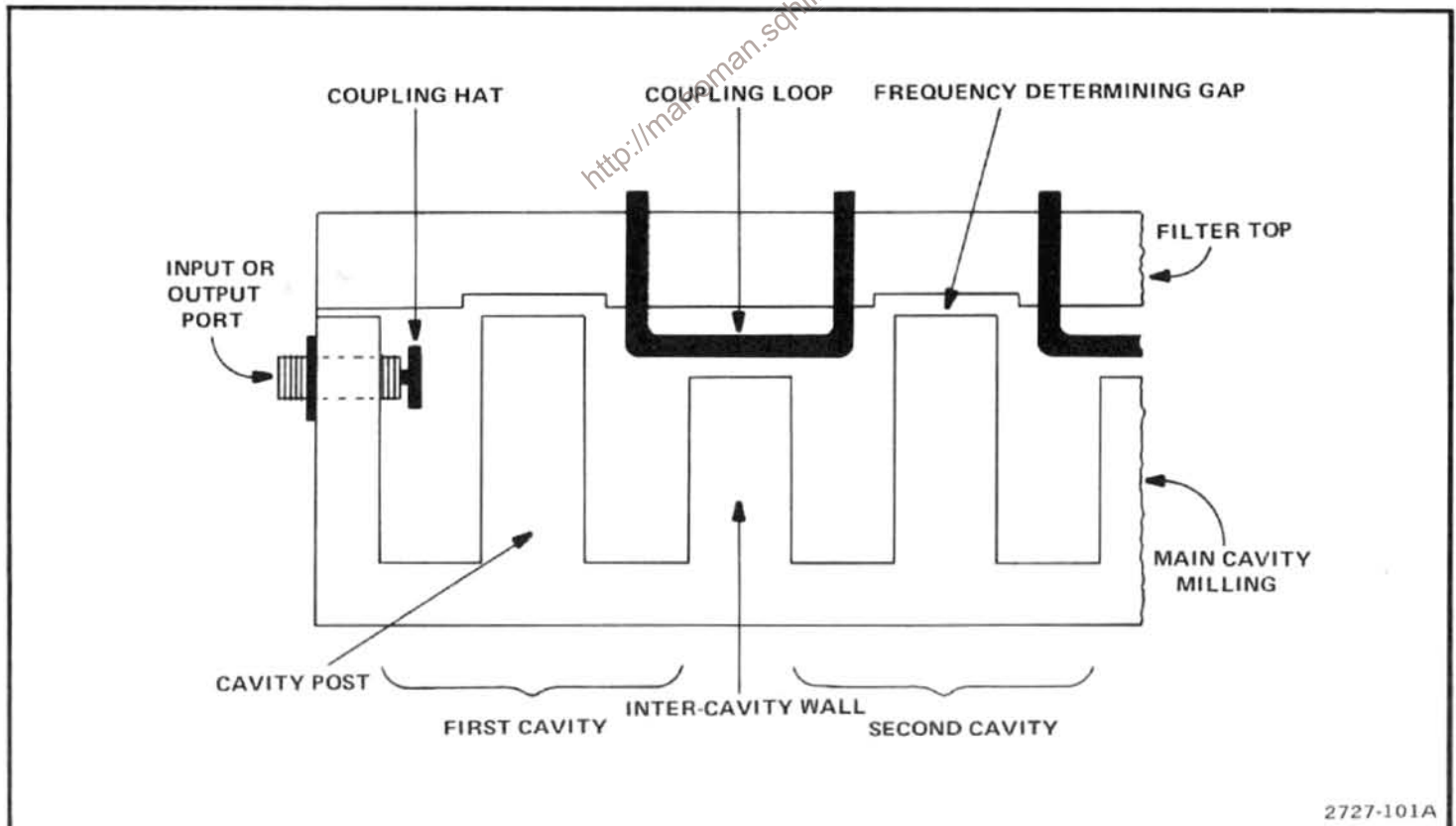


Figure 7-1. Cross section of a four-cavity filter.

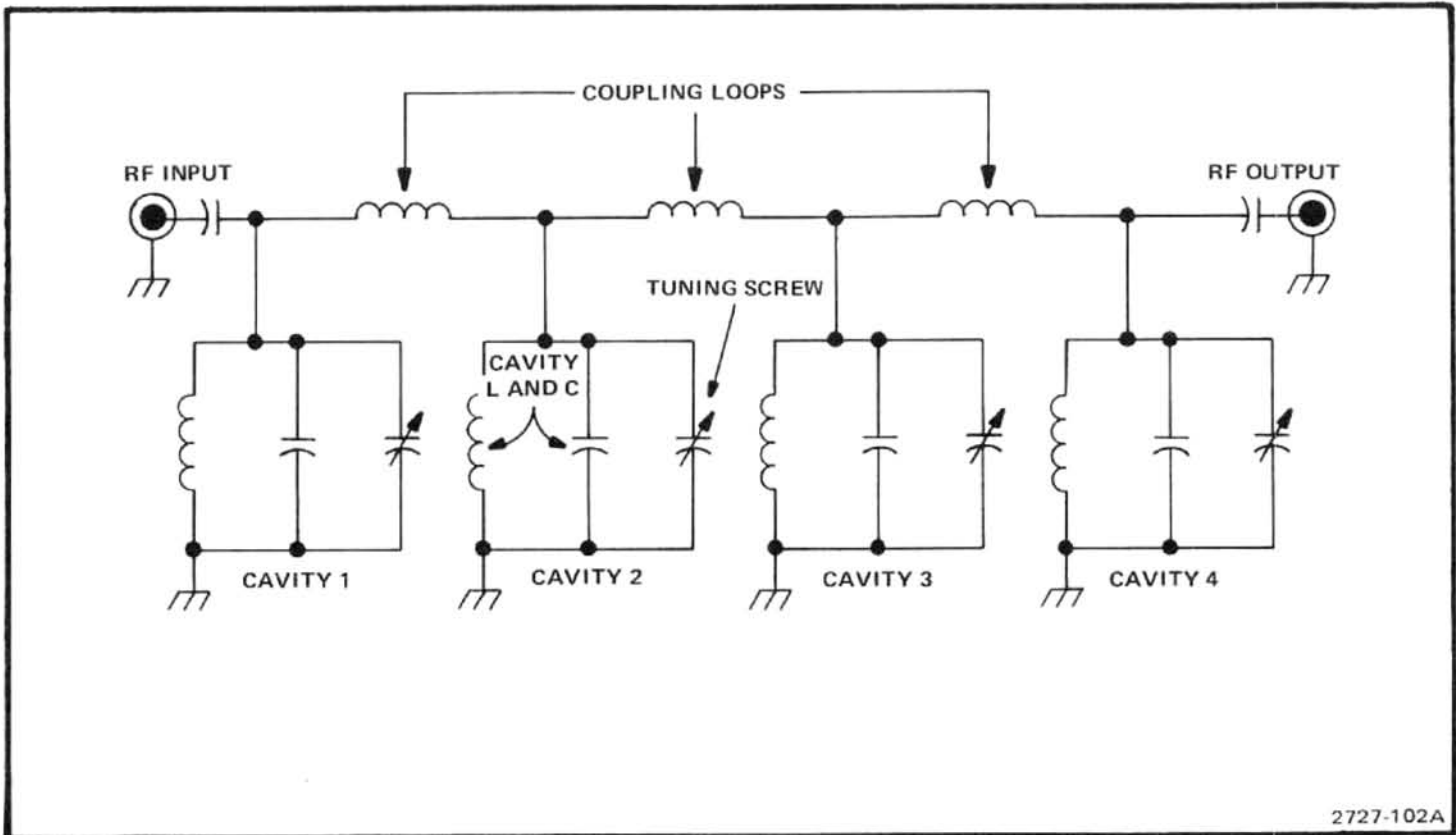


Figure 7-2. Equivalent circuit of the four-cavity filter.

2072 MHz RF from the four-cavity filter (FL14) enters the mixer, where it is switched on and off at a 2182 MHz rate by the mixer diodes. Conduction of the diodes is controlled by the much stronger 2182 MHz LO signal. Several mixing products result; one, the difference frequency of 110 MHz is separated from the others by a low-pass filter for use as the IF output.

The two inductors and one capacitor, at the output of the mixer, form a low-pass filter that passes 110 MHz unattenuated to the 829 MHz 2nd Converter, via coaxial connector P182. Capacitors, at each of the three inputs to the mixer, keep the diode bias from being impressed upon the RF and local oscillator lines.

The bias circuit, which consists of operational amplifier U1014 and the associated components, establishes the bias for the mixer diodes and also provides the means for effectively switching the mixer off (under control of the micro-computer). When the mixer is active, each diode has approximately 2 mA of forward bias. For this condition, the IF SELECT signal from the Z Axis/RF Interface circuits (applied through feedthrough capacitor C182) is low. This causes the output from U1014A to be at +14 V and the output from U1014B to be -14 V. Diodes CR1014 and CR1018 are thereby reverse-biased. Thus, the series resistances of potentiometer R1019 plus resistor R1014, and

potentiometer R1010 plus resistor R1017, provide forward bias to the diodes. The potentiometers are set to balance the bias levels.

In operation where the mixer is not active, the IF SELECT signal is high. This reverses the states of the U1014 outputs and forward-biases diodes CR1014 and CR1018. With these diodes conducting, resistors R1014, R1016, R1017, and R1018 form two voltage dividers that set the reverse bias, to the mixer diodes, at 5 V. This effectively turns the mixer off and attenuates the 110 MHz signal by about 55 dB.

Precision External Cables

The external cable that connects the four-cavity filter output to the mixer circuit and the external cable that connects the 2nd local oscillator to the mixer circuit are both critical length cables.

The Four-Cavity Filter-to-Mixer Input Cable (W140). Several products and harmonics of the local oscillator and RF input frequencies will exit the mixer via the RF input port of the mixer. The image (RF input minus the 2nd LO) and the sum (RF input plus the 2nd LO) are two significant products. There is enough energy in these two signals to warrant efforts to recover that energy.

Only the RF signal at 2072 MHz can pass through the four-cavity filter. Thus, any other signal frequency that is applied to the filter (that is, signals exiting the mixer via the RF port) is reflected back to the mixer by the filter. If the cable between the filter and the mixer is the correct length, the most significant reflected signals (that is, the image and the sum) can be returned to the mixer in phase and converted into additional energy at the intermediate frequency. This technique is called "image enhancement mixing" and typically improves conversion loss by approximately 3 dB at the design frequencies.

The image frequency, in this instance, is very near the RF frequency. A very sharp cut-off filter is required to pass the RF, yet reflect the image. The four-cavity filter performs this function.

The 2nd Local Oscillator-to-Mixer LO Input Cable (W222). The image and sum products are also present at the LO port of the mixer. These signals leave the mixer via the cable to the 2nd LO and are reflected back to the mixer by the LO. The oscillator resonator appears highly reflective to the image and sum signals because it is tuned to the LO frequency. Again, the length of the cable from the LO to the mixer LO port is adjusted so the image and sum signals are reflected back to the mixer, in the proper phase, for re-conversion to supply additional energy at the IF frequency.

2182 MHz PHASE LOCKED 2ND LO



General Description

The 2182 MHz phase locked 2nd LO assembly contains a tunable microwave oscillator, frequency reference, and phase lock circuitry within a two-section housing. Microwave circuitry is packaged within the machined aluminum portion of the housing. Low frequency phase lock circuitry is within the mu-metal compartment.

In the microwave or LO portion of the assembly, the 2182 MHz Microstrip Oscillator generates 2182 MHz for the 2nd converters and the 2nd LO internal reference circuitry. The 2200 MHz Reference circuit receives a 100 MHz drive signal from the 3rd converter crystal oscillator and produces 100 MHz harmonics. The 22nd harmonic or 2200 MHz is mixed with 2182 MHz from the microstrip oscillator in the 2200 MHz Reference Mixer circuit. The difference frequency of 18 MHz is then fed to the phase lock side of the module.

A phase/frequency detector, on the 16–20 MHz Phase Lock circuit board, compares the 18 MHz difference frequency with a signal from a linearized varactor tuned, 18 MHz voltage controlled oscillator. The detector output tunes the 2182 MHz Microstrip Oscillator such that the dif-

ference frequency exactly matches the frequency of the 18 MHz reference VCO.

Sweep and tune signals from the Span Attenuator and Center Frequency Control circuits tune the 18 MHz VCO. The output voltage from the phase/frequency detector forces the Microstrip Oscillator to tune the same amount.

2182 MHz Microstrip Oscillator



This oscillator consists of a printed half wavelength resonator driven by a common-emitter feedback amplifier (Q1021). The base of Q1021 is capacitively tapped into the resonator. The resonator serves as a tuned phase inverter and impedance transformer, connected between the base and collector of Q1021. Part of the base feedback capacitance is provided by a bendable tab (C1021). This allows fine adjustment of the total feedback. This feedback RF signal is detected, by the base-emitter junction of Q1021, to produce a change in bias voltage that is related to the amount of feedback. The base voltage can be monitored at TP1015 with a high impedance voltmeter without significantly disturbing the oscillator.

The dc collector voltage and current for Q1021 is regulated by an active feedback circuit containing transistor Q2021. Voltage at the junction of R2023 and L2023 is a function of Q1021 collector current. This voltage is sensed by Q2021, which alters the base current to Q1021 thereby regulating the collector current and maintaining +10 V dc on the resonator. Decoupling and control of bias loop dynamics are provided by C2104. Resistor R2016 swamps the negative base resistance of Q1021 to provide stabilization. Resistor R2015 protects the base-emitter junction of Q1021 from excessive reverse bias in the event the +12 V supply fails.

The oscillator is tuned by varactor diode CR1028, connected to one end of the resonator. Decoupling for the varactor is provided by the low-pass elements in the tune line. Bendable tab C1022 can be used to fine tune the oscillator center frequency.

Three output taps are coupled to the resonator through printed capacitors under the resonator. One output supplies 2182 MHz through a 6 dB attenuator to the Harmonic Mixer in the 829 MHz 2nd Converter. The other two output taps couple LO power through 6 dB attenuators to buffer amplifiers Q1031 and Q1011. The amplifiers provide approximately +10 dBm to the 2072 MHz 2nd Converter and +8 dBm to the Reference Mixer.

Since the two buffers are nearly identical, only the 2nd Converter buffer is described. Gain is provided by a single

common-emitter transistor (Q1011). Printed elements provide input and output impedance matching. Out-of-band damping is provided by R1011 in series with a 1/4 wavelength shorted stub. Dc is blocked by C1014 and C1011. A 1/4 wavelength open stub is used at the output to reflect one of the 2nd Converter's image frequencies at 4254 MHz (the other buffer does not use nor need this stub). Collector bias for Q1011 is provided through R1012, L1011, the 1/4 wavelength shorted stub, and R1011. The 1/4 wavelength shorted stub is grounded through C2011 (C2011, C1013, and L1011 are also used for decoupling). Collector voltage is determined by divider R1013 and R2013; this controls the dc feedback to the collector-base junction of Q1011. The bias network is decoupled from the RF path by L1014. Diode CR2013 protects the base of Q1011 from excessive reverse bias if the +12 V supply fails.

2200 MHz Reference Board

This circuit generates harmonics of the 100 MHz input. The 22nd harmonic or 2200 MHz is used by the Reference Mixer. The input 100 MHz signal is applied through a matching network (consisting of L1034, L1025, C1036, C1029, and C1025) to a differential amplifier (Q1024 and Q2024). The emitters of this amplifier are ac coupled through C2026, reducing low frequency gain and ensuring balanced operation. A snap-off diode (CR2014) is driven by the amplifier, via transformer T2015, to generate multiple harmonics of the 100 MHz signal including the 2200 MHz reference. The output passes through a 3 dB attenuator, for isolation, to the Reference Mixer circuit.

2200 MHz Reference Mixer

Signals from the 2200 MHz Reference circuit are filtered by a printed 2200 MHz bandpass filter. Diodes CR1011 and CR1012 are the switching elements of a single-balanced mixer. The microstrip oscillator output is applied to CR1011 and through a half wavelength delay line to CR1012. The delay line shifts the oscillator signal 180° so both diodes switch together. Mixing the 2200 MHz with the oscillator 2182 MHz signal produces the difference frequency of 18 MHz. This 18 MHz signal is fed through a 37 MHz low-pass filter to the 16-20 MHz phase lock circuit. The low-pass filter prevents unwanted products, such as 82 MHz (product of 2100 MHz and 2182 MHz), from passing into the phase lock circuit.

16-20 MHz Phaselock Board

This board contains regulated power supplies, a 16-20 MHz (18 MHz nominal) voltage controlled oscillator with linearizing circuitry, and a phase/frequency detector circuit. Its main function is control of the 2182 MHz Microstrip Oscillator. The entire circuit board is housed in a magnetic shield to reduce spurious effects of external ac fields. All power supply and control inputs enter the circuit board via

feedthrough capacitors in the housing wall. All connections with the microwave circuitry are through feedthrough capacitors C2200-C2204, in the floor of the housing.

The +15, -15, and +9 V supply inputs are re-regulated down to +12, -12, and +5.2 V by regulators using quiet operational amplifiers. IC U2025 provides a stable -6.2 V reference that is filtered by R2018 and C2015 and amplified by U2016B to produce the -12 V supply. IC U2016B uses emitter-follower Q2024 to increase the current capability of the supply. Resistor R2013 ensures sufficient base drive, while collector resistor R2025 reduces power dissipation in Q2024. Diode CR2019 protects the base-emitter junction during power supply shutdown. Feedback resistors R2016 and R2017 set the gain of U2016B and control the -12, +12, and +5.2 supply voltages. The -12 V supply is applied to inverting amplifier U2016A to produce the +12 V supply, and inverting amplifier U1017 to produce the +5.2 V supply. The output circuitry for the +12 V and +5.2 V supplies are similar to the -12 V supply.

Differential amplifier U2072A accepts the 2nd LO sweep voltages. One input senses the sweep voltage while the other input senses the ground potential at the Sweep board. Sweep sensitivity is adjusted by selecting resistor R2070. In wide spans, the sweep signal passes through parallel resistors R2082 and R2083. In narrow spans, R2082 may be switched out by Q2084, which reduces the sweep sensitivity by a factor of ten. When the TTL signal to Q2076 is high, Q2076 is turned off, R2086 holds the gate of Q2084 at -15 V, Q2084 is turned off, and R2082 is switched out. This reduces the sweep sensitivity. When the TTL signal is low, Q2076 saturates with the collector slightly above 0 V, Q2084 turns on, and full sweep sensitivity is restored.

Amplifier U2072B accepts the 2nd LO tune voltage. the Tune board senses the ground potential of the 16-20 MHz Phase Lock board and floats the tune voltage. Tune sensitivity is adjusted by selecting resistor R2072.

The sweep and tune signals combine at the summing node input of a non-linear shaping amplifier. The non-linearity of the shaping amplifier compensates for the non-linear tuning of the reference oscillator varactor to give a linear tuning characteristic from 16 to 20 MHz. The shaping function is produced by a resistor-diode array in the feedback loop of inverting amplifier U1073A.

All of the amplifier's feedback is through R1072 when the output swings to the negative limit. As the output voltage swings less negative, it sequentially passes the tap-point voltages of a series of voltage dividers connected between 0 V (the summing node at pin 12) and a negative reference set by Q1047. If the output becomes positive with respect to a given divider tap, a corresponding diode in U2059 for-

ward biases and connects the output to the tap, which creates additional feedback through one leg of the divider to the summing node. This causes R2051, then R2052, then R2053 (as so on through R2056) to be connected in parallel with R1072 as the amplifier output becomes less negative. This progressively increases the feedback, which causes the gain of U1073A to decrease.

Another series of dividers connected between the amplifier's output and a negative voltage reference causes the diodes in U1059 to sequentially conduct as the output becomes more positive. Resistors R2060, then R2061, then R2062 (as so on through R2065) are sequentially added in parallel with the existing feedback. Soft diode turn-on characteristics and a large number of breakpoints result in smooth gain changes. The non-linear amplifier's voltage-gain characteristic is controlled by the shaper reference voltage, which is set by R2049. Altering R2049 will make the breakpoints either closer together or further apart; in practice, this resistor is selected to correct the tolerance variations of the 18 MHz VCO varactor.

The forward drop of the shaper diodes gives U1073A an offset voltage. Temperature correction diodes CR1086, CR1087, and CR1088 correct this offset over a wide temperature range by summing a correction voltage through R1074. These diodes also compensate for the lack of series diode drop across R1072 and eliminate offsets at the summing input of U1073B. Selecting R1070 provides fine adjustment of the VCO's center frequency. IC U1073B is an inverting amplifier that increases the shaper output voltage swing to a level that can control the varactor of the 18 MHz VCO.

A differential amplifier with well-defined limiting characteristics is used for the 18 MHz VCO. Emitter degeneration is used to control loop gain. Transistors Q2096 and Q2087 form the differential pair of transistors, with the emitters coupled through C2091. Transformer T2092 provides ac feedback for the collector-base junction of Q2096 and also creates the majority of the resonator inductance. The total resonator inductance may be adjusted by trying different combinations of connections between taps on inductor T1091 and transformer T2092. These taps allow coarse adjustment of the VCO center frequency. The capacitor of the resonator is varactor CR1089. Capacitor C1088 completes the resonator ac path and acts as a dc block, which allows a bias voltage to be impressed on the varactor. Resistor R2092 and capacitor C2090 damp the Q2096 collector, which prevents high-frequency instability in the oscillator. Transistor Q2087 provides a buffered oscillator output.

A discrete two-stage amplifier provides an unsaturated voltage gain of approximately 43 dB for the 18 MHz signal from the 2200 MHz Reference Mixer board. Transistor Q1041 is the common-emitter first stage while Q1042 and

Q1043 form the differential second stage. The differential stage limits the output swing to 0.8 V to prevent over-driving the following ECL circuitry. Dc bias is maintained by Q1041, which has dc collector-base feedback via R1046 and the R1043/R1048 voltage divider. Transistor Q1043 receives its base bias through R1042. Each transistor operates with 5 mA of quiescent current.

ECL line receivers U2041D and U2041B amplify and buffer the 18 MHz signals from the Reference Mixer and the VCO, respectively. These two signals are then applied to the phase/frequency detector for comparison.

A pair of ECL D-type flip-flops, U2031A and U2031B, comprise the phase/frequency detector. The flip-flops drive a common reset line with a wired-AND output. The clock input of U2031B is driven with the signal from the 18 MHz VCO, and the clock input of U2031A is driven with the signal from the 18 MHz signal from the Reference Mixer.

Both flip-flops are configured to reset together whenever both are set. If they are clocked with signals that exactly match in frequency and phase, then both flip-flops set simultaneously and then almost immediately reset. If the Reference Mixer signal has a slight phase lead, U2031A will remain set longer than U2031B. If the Reference Mixer signal has a slight phase lag, U2031B will set first and remain set the longest. The signal that has the phase lead will cause the associated flip-flop to be set a greater percentage of time than the lagging flip-flop. If there is a frequency difference between the two inputs, the flip-flop with the higher input frequency will be set more of the time than the other flip-flop. The ratio between the filtered output signals of the two flip-flops indicates whether the Reference Mixer signal leads, lags, or differs in frequency from the 18 MHz VCO signal.

The outputs of the flip-flops are low-pass filtered by C1031 and C1028 and applied to differential amplifier U1031. U1031 compares the outputs of the flip-flops and produces an output that controls the tuning of the 2182 MHz microstrip oscillator. The phase-lock loop bandwidth is controlled by R1026, C1029, R1027, and C1026. The gain slope breaks to -12 dB/octave for frequencies below 16 kHz. Resistors R1033 and R1034 divide and offset the output of U1031 so the tune voltage ranges between 0 and -12.5 V.

The output of divider R1033/R1034 is applied to the varactor of the 2182 MHz microstrip oscillator (2nd LO). This closes the phase-lock loop, tuning the 2nd LO so that it closely tracks the 18 MHz VCO. When the 18 MHz VCO is tuned, U1031 simultaneously tunes the microstrip oscillator an equal amount. Within the loop bandwidth, the 2nd LO performance is determined by the 18 MHz VCO instead of

the microstrip oscillator, giving a significant improvement in frequency stability and reduction of phase noise.

829 MHz 2ND CONVERTER

15 16
If Section 15

The 829 MHz 2nd Converter down-converts the 829 MHz signal from the 1st Converter to 110 MHz for application to the 3rd Converter and provides the switching capability for the microcomputer controlled selection of either the 2072 or the 829 MHz converter system. The converter circuits consist basically of an input diplexer, an amplifier, a band-pass filter, a mixer, and a diode switch.

829 MHz Diplexer Circuit

15

The diplexer passes signals at 829 MHz with minimum attenuation (approximately 1 dB) and has a pass-band of approximately 200 MHz. All frequencies outside the pass-band, from approximately 50 kHz to 2 GHz, are terminated in 50 Ω loads with a match of at least 10 dB. Figure 7-3 shows a simplified schematic of the diplexer.

At 829 MHz, the series resonators provide a low impedance path from input to output. (Note on Diagram 15 that the input is from the 1st Converter through coaxial connector P231.) Ideally, signal loss across the 50 Ω resistors is zero because of the low impedance path around these resistors. The parallel resonator appears as an open circuit at 829 MHz.

At frequencies above or below the pass-band, the series resonators appear as large reactances, shifting the primary signal flow through the 50 Ω resistors. The out-of-band impedance of the parallel resonator is now small compared to 50 Ω. Thus, the resistors are essentially grounded at one end, terminating both the input and output ports. A wide bandwidth is used to minimize loss in the resonators and eliminate adjustments. Relative bandwidths of the series and parallel resonators are optimized to provide reasonable match at the band edges.

As shown in Diagram 15, the diplexer contains components not shown in Figure 7-3. Two pairs of 100 Ω resistors (R1012/R1015 and R1011/R1012) are used in parallel to form each 50 Ω termination. This reduces load inductance. A small capacitor is connected across each load (C1010 and C1013) to improve impedance match at frequencies above the pass-band. The inductor in the parallel resonator is a printed length of transmission line that is tapped to establish the correct bandwidth. One end of this inductor is grounded through four capacitors (C1017, C1016, C1019, and C1018) so that dc bias from the 1st Local Oscillator Driver can be introduced to the mixer through the diplexer. Four capacitors are used in parallel to minimize inductance variations

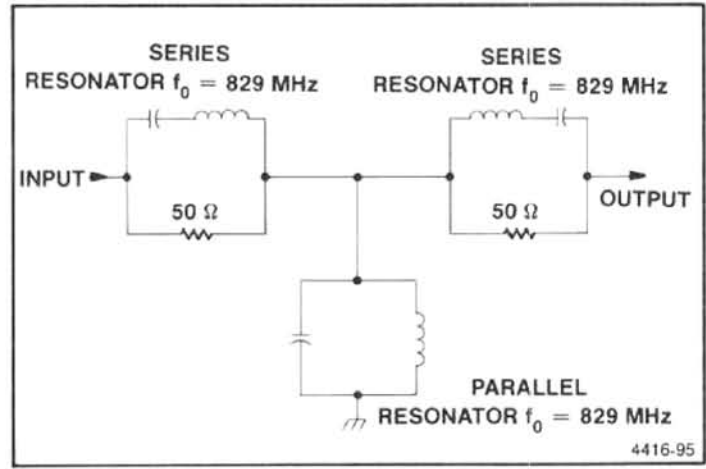


Figure 7-3. Simplified diagram of the diplexer.

and circuit Q degradation. A low-pass filter is included in the bias line to keep noise from the 1st Converter.

The diplexer is followed in the signal path by a printed circuit five-element low-pass filter that consists of three shunt capacitors and two series inductors. Cutoff frequency for this filter is approximately 1.2 GHz.

829 MHz Amplifier Circuit

15

The 829 MHz Amplifier provides approximately 18 dB of signal gain at 829 MHz and consists of two nearly identical amplifier stages in cascade (Q1017 and Q1025), plus a 3 dB attenuator. The overall noise figure is approximately 2.8 dB. The gain stages are designed as general purpose, unconditionally stable amplifiers for use in a 50 Ω system. Operation of a stage is covered by describing the ac and dc signal paths separately. Figures 7-4 and 7-5 are simplified diagrams of the ac and dc signal paths.

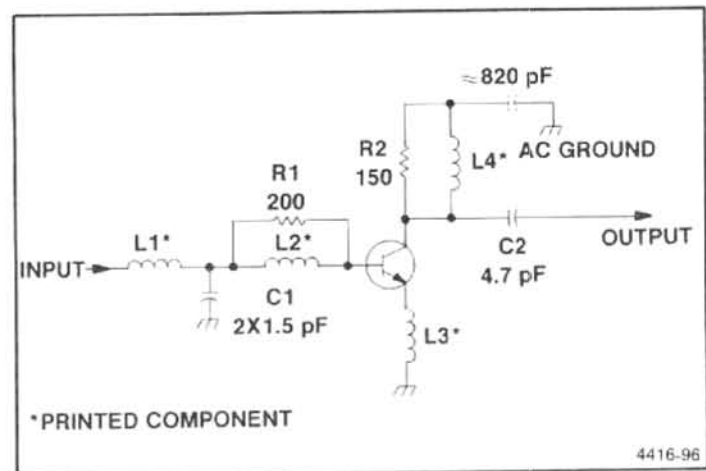


Figure 7-4. Equivalent ac circuit of an amplifier stage in the 829 MHz 2nd converter.

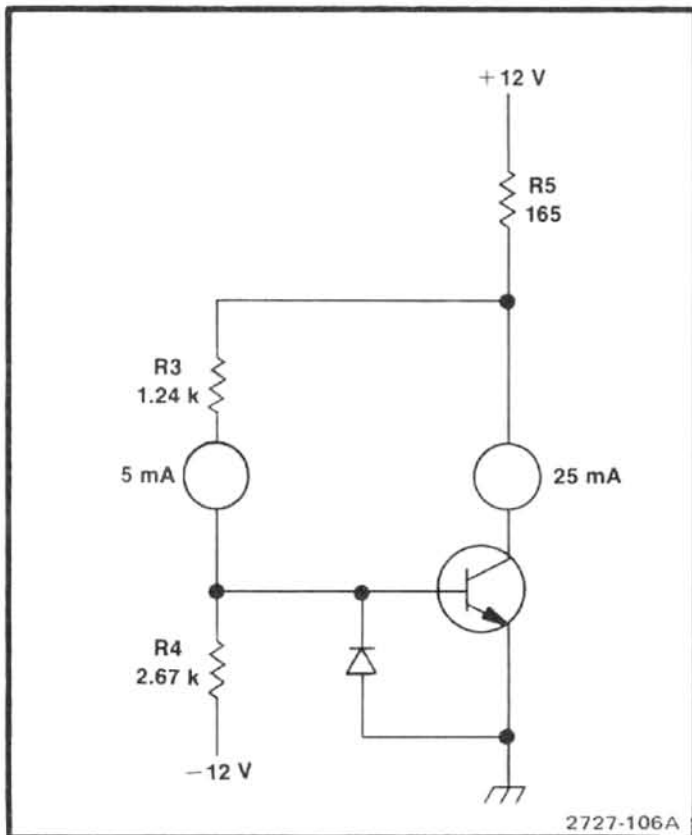


Figure 7-5. Simplified diagram of the dc path in an amplifier stage.

In the ac circuit (Figure 7-4) capacitor C1 and printed circuit inductors L1 and L2 form the input matching network. (In the first stage, inductor L1 is actually the series inductance of dc blocking capacitor C1016.) The collector circuit is matched to $50\ \Omega$ by inductor L4 and capacitor C2. Gain is primarily controlled by printed circuit emitter inductor L3. High frequency stability is enhanced by resistors R1 and R2. That is, at frequencies well above 829 MHz, resistor R1 ensures low common-base gain and resistor R2 helps to dampen the collector circuit.

In the dc circuit (Figure 7-5) negative feedback through the voltage divider, consisting of resistors R3 and R4, sets the collector voltage as a fixed proportion of the $-12\ \text{V}$ reference supply. Collector current is determined by resistor R5. Current requirements for the first stage is less than the requirements for the second because the first stage requires less intermodulation distortion performance. Reverse breakdown of the base-emitter junction can degrade the transistor performance, so a diode base clamp is provided in each circuit (CR1013 and CR1022) to protect the transistor if the $+12\ \text{V}$ supply should fail.

Not shown in Figures 7-4 and 7-5 are inductor L1014 and a capacitor C1014 in the base circuit for Q1017 and L1021, C1023 for Q1025 plus a capacitor in the collector

circuits (C1013 for Q1017; C1027 for Q1025). These decouple the signal path from the bias network.

The 3 dB attenuator (R1026, R1027, R1025, and R1029) helps maintain a wideband $50\ \Omega$ interface between the second amplifier stage and the 829 MHz bandpass filter. A test point (J1029) at the output of the attenuator is used to verify amplifier performance and to aid in adjustment of the following 829 MHz band-pass filter. From the attenuator, the signal is applied to the 829 MHz 2nd Converter Mixer circuit.

829 MHz Mixer Circuits



Frequency conversion from 829 MHz to 110 MHz occurs on the 829 MHz 2nd Converter board. The board contains a coaxial band-pass filter, a 1.3 GHz low-pass filter, a 3 dB attenuator, and a two-diode, single-balanced mixer with associated frequency duplexing circuitry.

829 MHz 1st IF signals, from the 829 MHz Amplifier, enters the converter through an 829 MHz band-pass filter. The filter blocks unwanted inputs, primarily the 609 MHz image signal. A 1.3 GHz printed element low-pass filter blocks high frequency signals that would otherwise be admitted at the re-entrant frequencies of the band-pass in excess of 2 GHz. The function of the 1.3 GHz low-pass filter is shared by the 1.2 GHz low-pass filter, located on the 829 MHz Diplexer board. A 3 dB attenuator on the 829 MHz Amplifier board and one following the 1.3 GHz low-pass filter help ensure consistent $50\ \Omega$ interfaces for the 829 MHz band-pass filter.

The 829 MHz band-pass filter consists of four, quarter-wave, coaxial type resonators, mounted on the 829 MHz 2nd Converter board. The end resonators are tapped near their grounded end to facilitate the filter's input and output coupling. Inter-resonator coupling is provided by printed "through-the-board" capacitors that connect between the resonators at their high impedance end. A bendable tab is located at the high impedance end of each resonator for fine adjustment of resonant frequency. The bendable tab acts as a small, variable capacitance from the end of the resonator to ground, making fine adjustments of resonant frequency possible. When properly tuned, the filter presents an input return loss of at least 12 dB at 829 MHz and an insertion loss of about 2 dB.

829 MHz enters the mixer diodes through a 450 MHz high-pass filter. The high-pass filter blocks the lower IF signals generated within the mixer. The mixer diodes are transformer driven by a large amplitude ($+12\ \text{dBm}$) 719 MHz from the local oscillator. This large signal drives the diodes in and out of conduction and switches the smaller 829 MHz signal on and off, at a 719 MHz rate, to generate several IM products. Only the difference frequency of 110 MHz is allowed to leave the mixer by way of a 300 MHz low-pass

filter which blocks LO, RF, and higher frequency products. The sum product of 1548 MHz, is reflected back to the mixer by the 829 MHz band-pass filter, in-phase with LO harmonics, to increase the energy of the 110 MHz signal. A printed delay line, between the 829 MHz band-pass and 1.3 GHz low-pass filters, controls the phase delay. The net result of this "image enhancement" is low conversion loss and good inter-modulation distortion performance. The 3 dB attenuator reduces the image enhancement affect and permits the use of non-critical line lengths and filter characteristics. Overall conversion loss, from 829 MHz to 110 MHz, is about 8.5 dB, including 2 dB from the 829 MHz band-pass filter and 3 dB from the attenuator.

110 MHz IF Select Circuits 

The 110 MHz IF Select circuits select the 110 MHz IF signal from either the 829 MHz 2nd Converter or the 2072 MHz 2nd Converter for transmission to the 110 MHz IF Amplifier. The 110 MHz IF signal, from the 829 MHz Converter, is applied directly to the select switch circuit. The 110 MHz IF signal, from the 2072 MHz converter, is applied (via coaxial connector P233) through a controlled amplifier to the select switch circuit. The switch circuit diodes are CR2011, CR2012, CR2013, and CR1015.

When the IF SELECT line to the 829 MHz 2nd Converter (via feedthrough C236) is low, series diode switch CR2011 is turned on. This steers the 110 MHz IF signal, from the 829 MHz 2nd Converter, to the output port. At the same time shunt diodes CR2012, CR2013, and CR1015 turn on and Q1011 turns off to isolate the output port from any spurious signals from the 2072 MHz 2nd Converter.

When the IF SELECT line goes high, amplifier Q1011 turns on and shunt diodes CR2012, CR2013, and CR1015 turn off to allow the 110 MHz IF signal, from the 2072 MHz 2nd Converter, to be applied to the output port. Series diode CR2011 also turns off to prevent signal loss into the inactive 829 MHz 2nd Converter. Isolation for the 829 MHz 2nd Converter is not critical, when the 829 MHz Converter is inactive, because the 719 MHz LO is also turned off by the state of the IF SELECT line. The switch and amplifier logic is summarized in Table 7-2.

As described above, diodes are used as the basic switch elements. When forward biased, with current of several milliamps, the diodes present only a few ohms of series resistance to RF signals. When reverse biased, the diodes present essentially an open circuit. The control signal from switch driver Q2015 is connected in a series path through the four diodes (CR2011, CR2012, CR2013, and CR1015) and inductors L2011, L2013, and L2019 so only a small current is required to forward bias all four diodes. This bias current is also used to turn off Q1011.

**Table 7-2
SWITCH AND AMPLIFIER SELECTION SUMMARY**

IF Select Line	Series Switch	Shunt Amplifier	110 MHz IF Source
High	On	Off	829 MHz 2nd Conv.
Low	Off	On	2072 MHz 2nd Conv.

Diodes CR2012 and CR2013 are incorporated into a pi-type matching network, consisting of inductors L2011, L2013, and capacitor C2012, so both switches shunt the signal at moderately high impedance points. In addition, when the switch diodes are turned on, parallel resonance, between inductor L2011 and capacitor C2012, presents virtually an open circuit to signals passed by switch diode CR2011. Switch diode CR2013 is located at the high impedance node created by series resonant inductor L2019 and capacitor C2017. Diode CR1015 directly shunts the output from Q1011.

Transistor Q1011 operates as a common-emitter amplifier for the 110 MHz IF signal from the 2072 MHz 2nd Converter. Its gain and impedance match are controlled primarily by feedback resistors R1011 and R1012. Resistors R1013 and R1018 attenuate the output by approximately 6 dB for enhanced control of match and stability characteristics. Dc collector current from Q1011 develops a voltage across resistor R1017. Bias control transistor Q1012 then compares this voltage with the fixed voltage of the voltage divider, R1015 and R1016. Any variation in the collector current of Q1011 is sensed by Q1012 and offset by a resulting change in the Q1011 base current. Collector current for Q1011 is set, in this manner, at approximately 15 mA.

When the control current from Q2015, through the switching diodes, develops a voltage across R1017 that exceeds the control limits of Q1012, it effectively removes the base-bias from Q1011 and turns Q1011 off. Negative current, supplied through resistor R1014, ensures that Q1011 is turned off by the loss of positive base drive. Diode CR1011 protects the base of Q1011 from excessive reverse bias. Voltage across R1017 is approximately 3.4 V when Q1011 is turned on and approximately 4.4 V when it is off. Overall gain is approximately 12.8 dB when the amplifier is turned on.

From the diode switch circuit, the 110 MHz IF signal is transmitted via coaxial connector P232 to the 110 MHz IF Amplifier.

829 MHz 2nd Converter, LO Section 16

The 829 MHz 2nd Converter LO generates the 719 MHz frequency that is mixed with the 829 MHz IF to produce the 110 MHz IF signal. In the following description, the circuits are referred to as the 719 MHz LO. The 719 MHz LO consists of a phase lock loop, a 719 MHz output circuit, and a 2nd LO front panel output circuit. Refer to Diagram 16 while reading the following description.

Phase Lock Circuit 16

The phase lock circuit receives reference frequency inputs and uses phase/frequency detection techniques to use those signals in controlling the output frequency of the 719 MHz oscillator. The circuit consists of a voltage controlled oscillator (VCO), a phase/frequency detector, a harmonic mixer, and various amplification stages and power splitters. When the 719 MHz LO is enabled, the 2182 MHz LO output frequency is used as a swept reference to derive the 719 MHz frequency. The VCO is controlled so that the third harmonic of its output frequency is a constant difference from the 2182 MHz reference. This control is accomplished by the phase lock loop. Refer to Figure 7-6 for a simplified block diagram.

In the phase lock loop, the harmonic mixer generates a frequency that is the difference between the swept

2182 MHz input reference and the third harmonic of the VCO output frequency. Ideally, this difference is 25 MHz, which in turn, is compared with the 25 MHz that is divided down from the 100 MHz oscillator output supplied from the 3rd Converter. This comparison is done by the phase/frequency detector whose output is a correction voltage that drives the VCO and shifts the oscillator frequency in the direction to hold the nominal output frequency at 719 MHz. This completes the loop that causes the VCO to track the 2182 MHz reference.

Because the 3rd harmonic of 719 MHz is locked to the 2182 MHz reference, the tuning range of the 719 MHz oscillator is only one third of the tuning range of the reference. Since the range is 4 MHz, the range of the 719 MHz oscillator is 719 ± 1.33 MHz.

The 719 MHz VCO (Q2014) uses a Colpitts configuration, with a printed circuit quarter-wavelength transmission line resonator, to achieve high spectral purity and good thermal stability. Correction voltage is applied to varactor diode CR1011 (which is connected at the midpoint of the transmission line resonator) to vary the resonant frequency of the transmission line over a 1.5 MHz range. A tunable transmission line (also printed) adjacent to the printed resonator compensates for variations in component tolerances and resonator dimensions. This adjustable transmission line is cut, at factory calibration, to the correct length for proper VCO operation. A scale with minor divisions every 2 MHz is

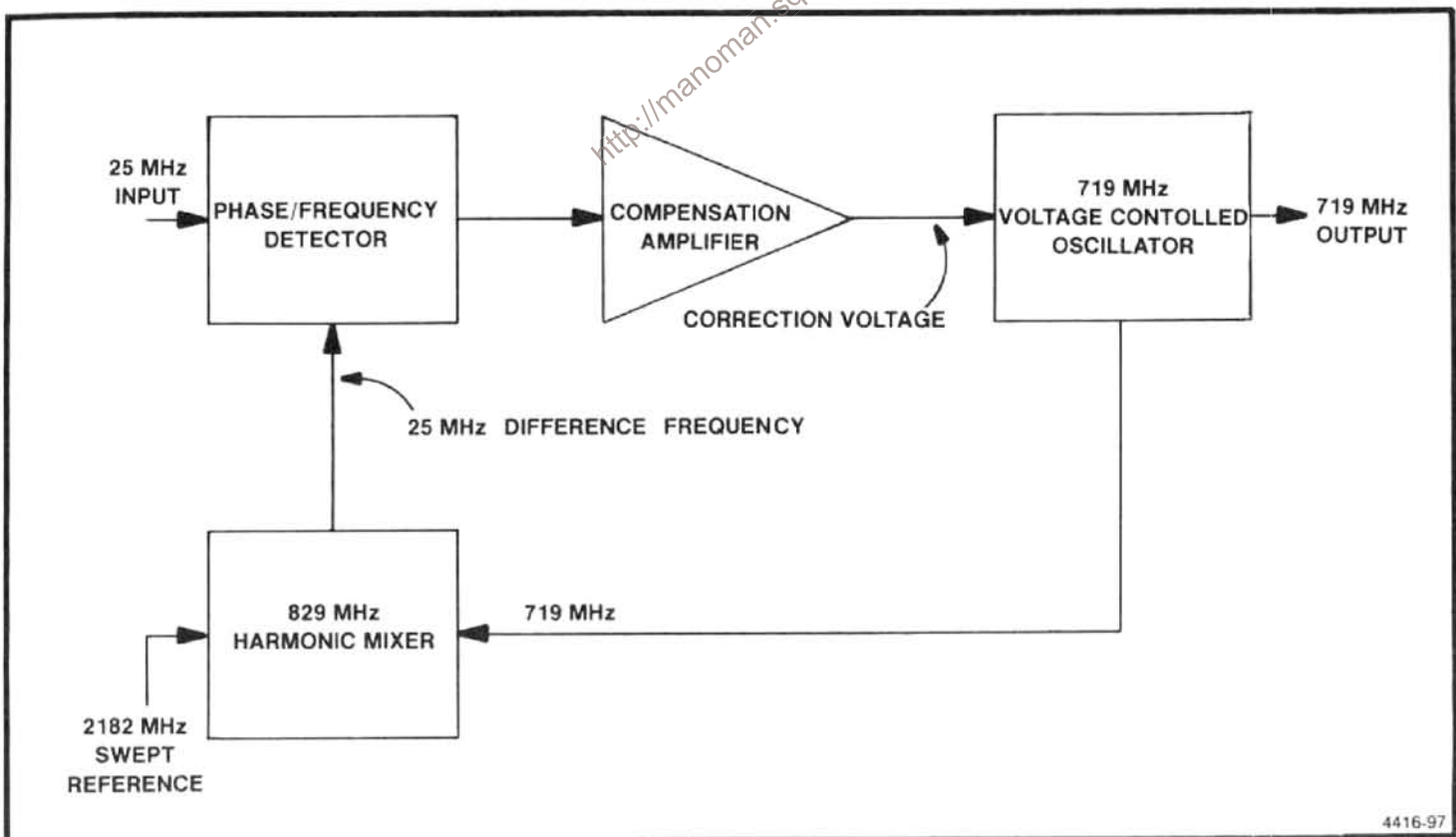


Figure 7-6. Simplified block diagram of the phase lock loop in the 829 MHz 2nd converter.

printed next to the adjustable line to aid in calibration. The output from the oscillator is extracted near one end of the quarter-wavelength line through two printed inductors and applied to output amplifiers through a power splitter.

The 719 MHz VCO is enabled or disabled, under micro-processor control, dependent upon the frequency band being analyzed, by the IF SELECT line. When this line is low, Q2017 is cut off, which turns Q2016 off. This, in turn, cuts off transistor Q3015 (which is the current source for oscillator transistor Q2014), thus disabling the 719 MHz oscillator.

From the oscillator, the +6 dBm 719 MHz output signal is applied, through a power divider consisting of resistors R1021, R1022, and R1020, to isolation amplifier Q1021. From the other side of this power divider, the signal is applied to an output amplifier (Q2021) for transmission to the 829 MHz 2nd Converter Mixer circuit. A second isolation amplifier (Q3021), identical in configuration, provides isolation between the 719 MHz oscillator output and any undesired Harmonic Mixer products.

The 829 MHz Harmonic Mixer produces not only the required 25 MHz difference frequency, but also many higher order IM products. Two of these frequencies, 744 MHz and 694 MHz, are 25 MHz from the 719 MHz oscillator frequency. The isolation amplifiers, Q1021 and Q3021, provide sufficient attenuation in the reverse direction to prevent these products from getting into the 829 MHz mixer to produce spurious signals.

To provide maximum reverse attenuation in each amplifier circuit, external RF feedback is kept to a minimum. An output matching LC network, consisting of capacitor C1025 plus a printed inductor for Q1021, and capacitor C3021 plus a printed inductor for Q3021, presents an optimum load impedance to the collector of each transistor to allow maximum power transfer to the attenuator that precedes the harmonic mixer. An input LC matching network consisting of capacitors C1023, C1022, plus a printed inductor for Q1021 and capacitors C3023, C3022, plus a printed inductor for Q3021, establishes the 50 Ω input impedance to each transistor.

A 3 dB attenuator consisting of resistors R3021, R3022, R2021, and R3023, at the output of isolation amplifier Q3021, provides a non-reflective source impedance to the mixer. Without the attenuator, mixer conversion loss could vary from unit to unit.

The 829 MHz Harmonic Mixer, consisting of diode CR2021, inductor L2014, and a half-wavelength (at 2182 MHz) transmission line, produces the difference fre-

quency between the third harmonic of the 719 MHz oscillator frequency (nominally 2157 MHz) and the 2182 MHz reference frequency. Note that the 2182 MHz signal is supplied from the 2182 MHz 2nd Local Oscillator through coaxial connector P237 and the power divider, consisting of resistors R1021, R1023, and R1022, to a half wavelength transmission line. The VCO input to the mixer switches diode CR2021 at a 719 MHz rate. The 2182 MHz reference acts as the RF and is applied to the diode from the transmission line. The resultant 25 MHz intermediate frequency is diplexed from the mixer through the 100 MHz low-pass filter consisting of capacitor C3014 and inductor L3014. (Diode CR2021 is mounted in printed circuit board cut-outs to relieve any necessity of bending the diode leads. Lead bending may fracture the diode case.) Inductor L2014 provides a bias return path to allow the diode to switch at a 719 MHz rate.

From the 829 MHz Harmonic Mixer, the signal is applied through the above mentioned low-pass filter to cascaded amplifiers U1053 and U1044B. These amplifiers boost the -32 dBm mixer output signal to a level appropriate to drive the phase/frequency detector. IC amplifier (U1053) contains two differential amplifiers in cascade; amplifier IC U1044 contains only one differential amplifier and acts as a buffer. When the loop is first acquiring lock, such as at power-on, the nominal 25 MHz IF may be as high as 34 MHz. Two stages of amplification are necessary to ensure enough gain for the phase/frequency detector to drive the IF back to 25 MHz; the buffer is necessary to provide ECL levels to the detector.

The second input to the phase/frequency detector is the 100 MHz signal, from the reference oscillator in the 3rd Converter, via two amplifier stages, U1022A and U1022B, and a $\div 4$ circuit, U1036A and U1036B. The 100 MHz signal is divided down to a 25 MHz reference for application to the phase/frequency detector. Two stages of amplification are used to isolate the 100 MHz reference bus from signals generated in the local oscillator section of the 2nd Converter. This stable 25 MHz reference signal is used to lock the difference frequency from the Harmonic Mixer to 25 MHz.

The phase/frequency detector output is a voltage that is proportional to the phase difference between the 25 MHz reference and the IF signal from the 829 MHz Harmonic Mixer. This correction voltage is then applied to the 719 MHz VCO to lock it to the reference.

The detector circuit consists of two D-type flip-flops, U2047A and U2047B, and a differential amplifier stage used as a NAND-gate (U1044A). The 25 MHz reference signal, from the frequency divider, is applied to the clock input of flip-flop U2047A; the nominal 25 MHz signal from the 829 MHz Harmonic Mixer is applied to the clock input of flip-flop U2047B. The rising edge of the input signal to each flip-

flop causes the Q(bar) outputs to return to the low level only after both flip-flops have been clocked.

If the frequency out of the 829 MHz Harmonic Mixer is below 25 MHz, or if its phase lags that of the 25 MHz reference, the \bar{Q} output of flip-flop U2047A will remain high longer than the \bar{Q} output of U2047B. If the frequency out of the Harmonic Mixer is above 25 MHz, or if its phase leads, the opposite will occur. When the two flip-flops are clocked at the same frequency and phase, the two outputs will be high for the same amount of time. The \bar{Q} outputs are applied to a compensation or differential amplifier U3053, that determines which output is high for the longer time.

Compensation amplifier U3053 provides part of the loop gain to ensure that the 719 MHz oscillator will track the sweep of the 2182 MHz reference oscillator. The compensation amplifier also limits the loop bandwidth to 100 kHz to make certain that the loop will not oscillate. Note the differential inputs to the amplifier each include a low-pass RC filter to attenuate the undesired high frequency clock pulses from the phase/frequency detector.

The nominal swing of the U3053 output is from +12 to -12 V. Since the compensation amplifier is capable of considerably more output than is needed to control the oscillator, a voltage divider is used to limit the output and reduce amplifier related noise. This voltage divider, consisting of resistors R2053, R2054, R3051, and R3052, reduces the possible ± 12 V swing to +5 V to +12 V, as required by varactor diode CR1011. Nominal voltage swing in a locked condition is +6.75 to +7.5 V. Thus, dependent upon whether the Harmonic Mixer frequency is above or below 25 MHz, the correction voltage swing, applied to diode CR1011, is more than nominal to correct the oscillator frequency.

Front Panel 2nd Local Oscillator Output Circuit

A portion of each 2nd LO output signal is sent to the front panel 2nd LO OUT connector. This output provides signal for external accessory equipment, such as a tracking generator. Each local oscillator (719 MHz and 2182 MHz) output is applied through power dividers to a power combiner for application to the 2nd LO OUT connector.

The 719 MHz oscillator frequency is applied from a power splitter (R3027, R3028, R3029) through a 1 GHz low-pass filter (C3025, C2024, C1023, C1021, and three printed inductors), to the power combiner (R2024, R2025, R2026), and the front panel 2nd LO OUTPUT. The 2182 MHz oscillator signal is applied through a power splitter (R1021, R1022, R1023), a 2.2 GHz band-pass filter (consisting of coupled quarter wavelength printed lines) to the power divider (R2024, R2025, R2026) and the front panel 2nd LO OUTPUT.

Both 2nd local oscillator signals, 2182 MHz and 719 MHz, are present at the front panel when the 829 MHz 2nd Converter is selected.

719 MHz Output Circuit

The 719 MHz 2nd Local Oscillator signal is applied is applied through divider resistors R2021, R2023, and R2024 to isolation amplifier Q2021. Q2021 boosts the signal level from about 0 dBm to +12 dBm to drive the 829 MHz mixer. The output of the amplifier includes a 3 dB attenuator (consisting of resistors R2027, R2028, and R2029), to ensure a 50 Ω non-reflective source impedance. The signal level at test point J2026 is typically -6 dBm.

110 MHz IF AMPLIFIER, 3RD CONVERTER, 100 MHz REFERENCE, AND REFERENCE LOCK



The 110 MHz IF Amplifier and 3rd Converter down converts the 110 MHz output signal from the 2nd Converter to 10 MHz for the Variable Resolution circuits. A 100 MHz crystal controlled local oscillator is phase locked to either a precise internal 10 MHz reference or an external 1, 2, 5, or 10 MHz reference. This 100 MHz is applied to the mixer and, through output amplifiers, to many other circuits throughout the instrument as a reference signal. It is also available for external use at the front-panel CAL OUT connector.

The 110 MHz signal is amplified in a three-stage gain block and applied to a three-section band-pass filter. This filter uses helical resonators and has a nominal bandwidth of 1 MHz. From the band-pass filter, the signal is applied to the converter, which consists of a mixer, an oscillator, and various output amplifiers.

110 MHz IF AMPLIFIER



Initial gain for the analyzer is provided by the 110 MHz IF Amplifier. This gain compensates for conversion losses in the three mixers. Typical gain for the amplifier is 21 dB. The amplifier consists of three stages of amplification and an attenuator. The first two mixers in the RF system offer no high-frequency gain; therefore, it is important that this amplifier exhibit low noise characteristics. It must also be relatively free from third-order intermodulation distortion.

Signal input is applied through an impedance matching band-pass filter (L2044 and C325) to a parallel tuned circuit. The signal is injected into the parallel-tuned circuit through a tap in the inductor and taken out at the high impedance side through variable capacitor C2047. Inductive input provides for conversion to high impedance within the tuned circuit; the extra capacitor on the output provides for conversion back to 50 Ω nominal. The primary tuning capacitor, C325, adjusts the resonant point; the output capacitor, C2047, is adjusted in combination with C325 for good impedance match at 110 MHz. This is done with a return loss bridge. The nominal return loss is 35 dB. The Q of the input filter is approximately 20.

From the input filter, the signal is applied to Q4053, which is the first stage of amplification. This is a broad-band feedback amplifier to provide good input and output impedance and controlled gain. All feedback is through reactive components (transformer T3054), not resistive components. Thus, the impedance and gain can be controlled without significant noise problems.

The second amplifier stage, Q4037, is essentially the same as the first, with only minor bias differences. Gain through each of these stages is approximately 9 dB. The output is applied through a 3 dB attenuator, to preserve the impedance figure, to the bridged "T" adjustable attenuator. The 3 dB attenuator consists of resistors R2039, R2038, and R2043.

From the 3 dB attenuator, the signal is capacitively coupled through C2037 to the adjustable attenuator. This attenuator uses two PIN diodes, CR3030 and CR1029, in the mode when the resistance to RF signal flow is controlled by the current through the diodes. Refer to Figure 7-7 to aid in understanding the following description.

If resistor R1 in Figure 7-7 were set to infinite resistance and resistor R2 were set to zero resistance, the RF signal path would be through R2 to ground, to produce infinite signal attenuation. If resistor R1 were set to zero resistance and resistor R2 were set to infinite resistance, the RF signal path would be through R1 to the load, to produce almost no attenuation. This, basically, is how the adjustable attenuator operates, except that resistors R1 and R2 are actually PIN diodes and the RF path resistance through these diodes is controlled by the current through the diodes in an inverse proportion (higher current results in less resistance to RF).

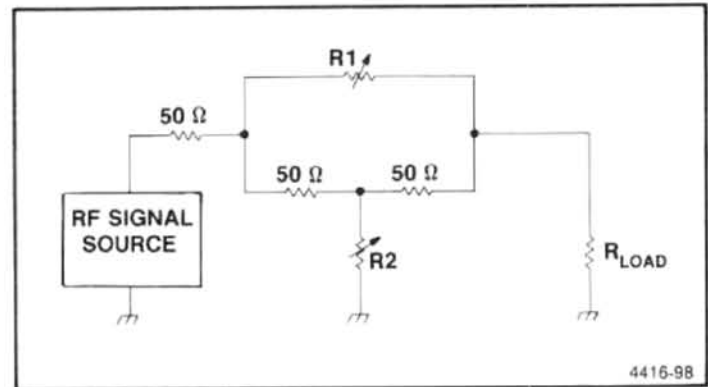


Figure 7-7. Bridged "T" attenuator equivalent circuit.

Resistors R3035 and R2030 on the 110 MHz Amplifier board, A32A1, establish a constant current of approximately 2 mA from the 15 V supply to the diodes. This current is divided according to the bias on the diodes. The bias, in turn, is established by gain adjustment R1015, from the +15 V supply. If R1015 is set low (near ground), diode CR3030 is reverse biased and the 2 mA flows through diode CR1029. This routes the RF signal through resistors R2032 and R3029 and capacitor C2029, with the impedance characteristics of CR1029 added for maximum attenuation.

If R1015 is set higher (nearer +15 V), diode CR3030 is forward biased and starts to conduct. Since the 2 mA supply current is relatively constant, this subtracts from the current through CR1029. Thus, the impedance of the diodes is relatively constant, which results in a good impedance match over a broad range. The RF signal path is determined by the exact amount of current through CR3030; part of the RF signal path is through CR3030 to the output amplifier and part is through R2032 and diode CR1029 to ground. This results in reduced signal attenuation.

If R1015 is set to the positive limit, the entire 2 mA flows through CR3030. This routes the RF signal through CR3030 (which exhibits little resistance with high current) to the output amplifier with almost no attenuation. (The insertion loss is approximately 1 dB.)

From the adjustable attenuator, the signal is applied to the final amplifier Q3018. This stage is a broad-band feedback amplifier that supplies relatively substantial output current and exhibits good intermodulation distortion performance. This is provided primarily through the large current capacity, by negative feedback through resistor R3014, and emitter degeneration through resistor R4029. These resistors are sized to provide a reasonably good impedance match at 110 MHz. Nominal gain of the stage is 13 dB.

With Gain potentiometer R1015 set for maximum gain (least attenuation), the gain of the 110 MHz IF Amplifier is approximately 26 dB to 27 dB. R1015 is normally adjusted for total gain of 21 dB.

The output signal from the 110 MHz IF Amplifier is applied through the 110 MHz band-pass filter, FL36, to the 3rd Converter.

110 MHz BAND-PASS FILTER



The 110 MHz band-pass filter is a three-section filter using helical resonators, which determine the widest resolution bandwidth of the analyzer. The filter provides image rejection to prevent the mixer from producing 10 MHz outputs from input signals of 90 MHz, and it also limits the noise spectrum that appears at the 10 MHz IF circuits to those frequencies at which signals also appear.

Though the filter is a sealed unit, in the interest of system understanding, the following brief description is provided.

The filter consists of three small encapsulated helical resonators that are tuned with multi-turn trimmer capacitors. For purposes of impedance matching, the filter is symmetrical. The end resonators are connected to external circuits by 10 pF capacitors attached to taps on the coils. Coupling between resonators is accomplished through holes in the resonator cans.

Adjustment of the filter for minimum attenuation is performed by setting the three trimmer capacitors. Insertion loss is approximately 4 dB to 4.5 dB. From the filter, the 110 MHz signal is applied to the 3rd Converter.

3rd CONVERTER



The 3rd Converter consists of a crystal and phase locked 100 MHz oscillator and mixer. It outputs the 3rd IF of 10 MHz, for the VR, and a stable 100 MHz reference for other circuits within the instrument.

100 MHz Oscillator



A Colpitts oscillator is formed by Q2038, L1041, C1038, and related components. Y3038 is a 100 MHz crystal that operates in a series resonant mode in the feedback loop of the oscillator. L3041, varactor diode CR3039, and Y3038 form a series resonator that is used to tune the oscillator approximately ± 1 kHz (the voltage on CR3039 is varied, which changes its capacitance). RPL GND is tied to ground in the Reference Lock module. RPL VOLTS TUNE varies from 0 V to +12 V to tune the oscillator to exactly 100 MHz. P2042 shorts across the tune circuit for adjustment purposes. The output of the oscillator is coupled through C2042 to differential amplifier Q2042/Q2041. The two separate outputs of approximately 2 V peak-to-peak amplitude go to three hybrids (mixer U3051, distribution amplifier U3031, and calibrator U2022) on the 3rd Converter board.

Mixer

At mixer U3051, 100 MHz enters on pin 2 and is amplified to drive a ring diode mixer. 110 MHz enters on pin 10 and is mixed with the 100 MHz to yield mixing products at 10 MHz and 90 MHz. The 10 MHz signal passes through a low-pass filter and is sent to the Variable Resolution Input circuit, while the unwanted 90 MHz signal is terminated in a 50 Ω resistance within the mixer.

Distribution Amplifier

U3031 distributes a 100 MHz signal to other modules in the instrument. The input level on pin 2 is typically 2 V peak-to-peak, while the output level is 0 dBm into a 50 Ω load.

Calibrator

U2022 and related components regulate a 100 MHz signal to -20 dBm for the front-panel CAL OUT connector, through coaxial connector J1011. VR1051 serves as an accurate 6.2 V reference, which is attenuated to approximately 1.2 V and applied to pin 6 of U2022. The 100 MHz signal enters pin 1 and passes through a variable attenuator pin diode. The signal is then amplified and passed through a low-pass filter to remove any harmonics. The signal then enters a peak detector and comparator where the peak amplitude of the 100 MHz signal is compared to the 1.2 V reference on pin 6. An operational amplifier then adjusts the attenuation level of the pin diode to maintain a constant signal level. The output of this operational amplifier can be measured on TP3011. A small portion of the 100 MHz signal is attenuated through R2011 to -20 dBm. R1021 and R1022 supply bias current to the peak detector circuits. The voltage on pins 7 and 8 should typically be +5 V.

C2023, C2011, and related components form a high-pass filter to allow harmonics of 100 MHz to pass through to the front panel. The final result is a calibrator signal rich in harmonics with an accurate 100 MHz amplitude.

REFERENCE LOCK



The Reference Lock module consists of a reference detector, frequency synchronizer, phase/frequency detector, and tune window detector. Either an internal 10 MHz reference or an external 1, 2, 5, or 10 MHz reference frequency is routed through the reference detector to the frequency synchronizer. The local oscillator's 100 MHz output is divided by 100 and applied to one input of a phase/frequency detector which compares it with the 1 MHz reference frequency. The resultant error signal is amplified by the tune amplifier and applied, as a corrective voltage, to the voltage controlled 3rd LO.

External Reference Detector

Buffer amplifier Q2014 converts External Reference signals, within the range of -15 dBm to $+15$ dBm, into TTL compatible level. When an external signal, within the level range, is applied, it triggers multivibrator U2046B. The output of U2046B enables external signal control NAND gate U2032D, and disables the internal signal control gate U2032A. It also disables the internal 10 MHz reference oscillator by turning Q1031 on, which biases Q1033 off, and removes the $+5$ V supply for the oscillator. The \bar{Q} output of U2046B is sent to the processor, on the EXT REF line, to indicate that an external reference frequency is in use. The microprocessor can also pull the INTERNAL SHUT-DOWN line down, during a diagnostic test, to turn the Internal Reference Oscillator off and check for loop unlock. U2032B is a wired-OR gate that gates, either, the 10 MHz from the internal gate U2032A, or the external reference from U2032D, to the frequency synchronizer U2046A.

Frequency Synchronizer

Multivibrator U2046A, synchronizes its 1 MHz output with any of the 1 MHz multiple input signals by edge-triggering the time-out period. The 1 MHz output frequency is set by the timing components R2039, C2038, and adjustment R2042. With a 10 MHz signal applied to U2046A, adjust-

ment R2042 is set for a $1 \mu\text{s}$ period, with 65 ns between the falling edge on TP2046 and the next falling edge on TP1044.

Phase/Frequency Detector

The 100 MHz, from the 3rd Local Oscillator, is divided by 100 and converted to a TTL level by prescaler U2020. The 1 MHz from U2020, is fed to the clock input of D-type flip-flop U1044A. The 1 MHz from U2046A, is applied to the clock input of D-type flip-flop U1044B. The two flip-flops and NAND gate U2032C, form the Phase/Frequency Detector. R1034, R1035, and C1037, along with its counterpart, on the output of U1044A, form a low-pass averaging filter for the outputs of the flip-flops. When the two input frequencies are equal and in phase, the composite output of the averaging filter is $+2.5$ Vdc.

Tune Amplifier

The FET input operational amplifier (U1034) takes the output of the phase/frequency detector, amplifies the error and supplies an appropriate tune voltage to the 100 MHz voltage controlled oscillator. The tune amplifier, with feedback components C1031, C1038, R1028, and R1029, determine the loop transfer characteristics. The loop dc gain is very high which takes advantage of the high accuracy of the internal or external references. The loop ac gain (determined by C1031) rolls off very quickly so any phase noise, on an external reference signal, is not amplified.

Lock Detector

U1012 is used as a tune volts window detector. R1013, R1012, and R1011 set the upper threshold at 11 Vdc, and the lower threshold at 2 Vdc. As long as the tune volts stays within these limits, a high output tells the processor that the 3rd LO loop is locked. A low output from U1012, indicates that the reference oscillator frequency is beyond the 3rd LO's tune range. This REF LOCK status line, along with the other two processor interface lines, is routed through the Sweep board for processor interrupt generation. The processor reads the lines and displays their status on the crt readout.

IF SECTION



The IF section receives the 10 MHz IF signal from the 3rd Converter, establishes the system resolution through selective filtering, levels the gain for all bands, and logarithmically amplifies and detects the signal to produce the video output to the Display section.

System bandwidth resolution is selectable, under microcomputer control, from 1 MHz to 100 Hz in decade steps plus 30 Hz. This selection is performed by the Variable Resolution circuits. Two sets of filters are used to establish the bandwidth. Band-pass filters are also included at the circuits input and output.

Significant gain is also provided by several stages of amplification within the Variable Resolution circuit block. Other gain steps, under microcomputer control, are also provided by switching gain blocks in or out of the signal path. These gain blocks when switched in combination, provide -10, +20, or +30 dB of additional gain.

Leveling, to compensate for front-end losses, is also included in the Variable Resolution circuit block. Because there are greater front-end losses in the higher frequency bands, band leveling amplification is required for these bands.

To calibrate the graticule in dB/division, a logarithmic amplification of the signal is required. This is performed by a seven stage amplifier that produces an output proportional to the logarithm of the input; thus, the screen displacement can be selectable as to amount of change per division, and can be proportional to the input level change. For example, in the 10 dB/div display mode, each division of displacement on the screen represents a signal level change of 10 dB regardless of whether it is at the top or bottom of the screen.

An area detector follows the logarithmic amplifier to produce a positive-going output signal that is applied to the display section as the VIDEO signal.

Variable Resolution Circuits



The Variable Resolution (VR) circuits establish the resolution bandwidth, under microcomputer control, and provides approximately 41 dB of system gain in band 1. The assembly consists of two sets of filters plus gain stages. Since the input to the VR circuits is nominally at -35 dBm and the Log Amplifier input requires +6 dBm for full screen,

the VR circuits must provide the gain difference. (In the 494/494P the VR supplies 30 dB of additional gain and 10 dB of gain reduction for all vertical display modes as well as 30 dB of additional gain for band leveling.)

Physically, the VR section consists of two sub-assemblies that plug onto the analyzer Mother board. The input circuits are in one sub-assembly and the output section and digital interface are in the other. Each of the sub-assemblies consists of boards that plug onto a four-layer VR Mother board with a ground plane on both outside layers. Only power supply and control voltages travel through the VR Mother board. All signal interconnection is via coaxial cable.

VR Input Circuit



The VR Input circuit receives the 35 dBm 10 MHz signal from the 3rd Mixer through J693. This signal is applied to a two-pole, 1.2 MHz bandpass filter, which augments the 1 MHz filter that precedes the 3rd Mixer and provides initial selectivity. This 1.2 MHz filter includes C1037 and C1031 and all of the components between. Filter tuning is provided by variable capacitors C1033 and C1026, Input Align.

From the filter, the signal is applied to broadband feedback amplifier Q1023, which is biased at a relatively substantial output current (approximately 50 mA) to exhibit good intermodulation distortion performance. This performance is provided primarily through the large current capacity by negative feedback through resistor R1025 and by emitter degeneration resistor R1023.

A 6 dB attenuator at the output of amplifier Q1023 provides a clean 50 Ω output to the 1st Filter Select circuit and reflects a 50 Ω termination back through the amplifier for proper termination of the 1.2 MHz band-pass filter. The output signal is transmitted via jumper B.

1st Filter Select Circuit



The 1st Filter Select circuit operates in conjunction with the 2nd Filter Select circuit to determine the overall system bandwidth through banks of switched filters that are selectable under the analyzer microcomputer control. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder IC U4035 (it provides a low signal on the appropriate output pin to enable the selected filter). Bandwidth selections are 1 MHz to 100 Hz in decade steps plus 30 Hz. The data bits select a filter bandwidth according to Table 7-3.

Table 7-3
BANDWIDTH SELECTION

DB0	DB1	DB2	Bandwidth
1	0	0	1 MHz
0	1	0	100 kHz
1	1	0	10 kHz
0	0	1	1 kHz
1	0	1	100 Hz
0	1	1	30 Hz

Filter selection is done by PIN diode switching. At the input and output of each filter is a series and a shunt diode. When a filter is selected, the series diodes are biased on and the shunt diodes are biased off. For the filters that are not selected (only one is on at a time), the diode conditions are opposite. Since the switching operation is the same for all filters, the description for the 100 kHz filter selection is applicable to all filters with the appropriate component designators.

With a content of 010 for the three data bits, line 2 from U4035 will be low. This turns on transistors Q3019 and Q3055, which operate as dc switches. With input switch Q3019 turned on, the current path is through R4012, L3012, CR3010, L3013, R3014, and Q3019. This current is determined by decoupling resistor R3014 and resistor R4012. The voltage drop across R3014 and R4012 is sufficient to turn CR3010 on and reverse-bias CR3012. The same operational situation exists for the filter output switch, Q3055. Resistors R3057 and R1067 establish the current to forward-bias CR3061 and reverse-bias CR3060.

Thus the signal from the input circuit, via jumper B, is applied through the selected filter and transmitted to the 10 dB Gain Steps circuit via jumper K. Nominal loss through the filter circuit is approximately 13 dB, with slight variations among the filters. The output level is nominally -32 dBm.

In the non-selected filter sections, the input and output switch transistors are turned off by the high outputs from decimal decoder U4035. The collectors are pulled toward -15 V by pulldown resistors, which forward-bias the shunt diodes (input: CR3014, CR3012, CR2013, CR2011, CR1013, and CR1011; output: CR3062, CR3060, CR2066, CR2055, CR1055, and CR4065). Since one filter is always selected, the voltage drop across the common input and output resistors (R4012 and R1067, respectively) back-bias the series diodes (input: CR3011, CR3010, CR2012, CR2010, and CR1010; output: CR4068, CR2062, CR2059, CR1059, and CR4064).

Design of the filter for each bandwidth is determined by the requirements of each band and ranges in complexity from no filter to an electronically switched dual-bandwidth filter, for the 100 Hz/30 Hz resolutions.

A filter is not used in the 1 MHz section, because this circuit section is preceded by two filters that accomplish the required function; the first is the 1 MHz filter between the 2nd and 3rd Converters, the second is the 1.2 MHz filter in the input circuit. Instead of a filter, a 6 dB attenuator is contained in the 1 MHz selection circuit. This attenuator provides initial leveling to compensate for the loss when a filter is used.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C3023 and C3035 provide for input and output adjustments. Impedance matching is accomplished at both input and output by series capacitors C3020 and C3048, respectively.

The 10 kHz filter uses a pair of two-pole monolithic crystal filters that are interconnected by variable shunt capacitor C2037. Input and output impedances are matched with broadband transformers T3026 and T3055. A 3 dB attenuator consisting of R2027, R2026, and R2028 is included at the filter input.

The 1 kHz resolution filter consists of a single two-pole monolithic crystal filter, matched to the 50Ω impedance with broadband transformers T2035 and T2055. A 2 dB attenuator consisting of R2024, R2023, and R2025 is also part of the filter.

The 100 Hz/30 Hz filter is an electronically switched filter that has a bandwidth of 100 Hz when its input and output ports are low (-15 V) and 30 Hz when high ($+15$ V dc). When 100 Hz is selected, output 5 (pin 6) of decoder U4035, outputs a low. This low turns transistor Q1020 on which forward biases CR1010 and back biases CR1011. This applies the IF to the input of the 100 Hz/30 Hz filter FL690. At the same time Q4050 is turned on which applies forward bias to CR4064 and back bias on CR4065. The output of FL690 is now connected to the input of the 10 dB Gain Step board through pin K.

When output 6 (pin 7) of decoder U4035 is high, Q1019 and Q1055 are off. This applies -15 V to the input and output ports of the 100 Hz/30 Hz filter FL690 so it is in the 100 Hz mode. When output 6 of U4035 is low, Q1019 and Q1020 are on as well as Q1055 and Q4050. This provides forward bias for CR1010 and CR4064. At the same time

Q1019 and Q1055 are turned off which applies +15 V to the input and output ports of FL690 switching it to its 30 Hz mode.

Diodes CR1017, CR1021 and CR1018, CR1022 provide limiter and clamping action at the filter input to remove RF excursions when the dc potential at the filter input and output switches.

10 dB Gain Steps Circuit

The 10 dB Gain Steps circuit provides 10 dB of signal gain when selected by the microcomputer. The circuit consists of three stages of amplification; one stage provides variable gain and the other two are fixed gain steps. The nominal input signal level from the 1st Filter Select circuit is -25 dBm for a resolution bandwidth of 100 kHz. (All levels listed in this description relate to the 100 kHz resolution.)

The input signal is applied through an impedance transformer, T4019, to the first amplifier stage consisting of a differential pair, Q3016 and Q2027, and an emitter follower output amplifier, Q1036. Negative feedback through R1031 and R2051 provide gain stabilization. An output resistor, R2035, increases the output impedance of the composite amplifier to approximately 50 Ω .

Gain of the input stage is fixed for all resolution bandwidths except 30 Hz. The gain for 30 Hz resolution is set to a precise level by activating Q2015. Transistor Q2015 is turned on when pin L goes low. This adds R2025 (30 Hz Level) across feedback resistor R2051. Adjustment R2025 can now set the gain of the stage.)

The output from the 1st stage is then applied to a common emitter stage (Q2043). Gain of this stage, when transistor Q4039 is turned on, is 10 dB. When the base of Q4039 is pulled low by data bit 0 from Q4035 on the VR #1 Mother board, A69A1, the transistor saturates and shunts the emitter load resistor R3048 with R3038 and 10 dB Gain adjustment R3035.

The output of Q2043 drives the input of the third amplifier stage. This stage operates the same as the first stage except for gain variation. Feedback resistor R1060 is shunted by PIN diode CR1053. As the current through the diode increases, the resistance decreases and the gain of the stage increases. Gain control of the stage is established by the setting of the front-panel AMPL CAL adjustment. Gain range is approximately 14 dB.

Output impedance of the stage is 50 Ω , set by resistor R1064. Nominal output level is -2 dBm for a full screen

display. This level may be as high as +8 dBm when MIN NOISE is active. A 10 dB gain is removed from the Log Amplifier to reduce the noise level and must be supplied by the VR section.

20 dB Gain Steps Circuit

The 20 dB Gain Steps circuit provides -6 dB, +4 dB, +14 dB, and +24 dB of gain in precise 10 dB steps. The nominal -2 dBm input is supplied through pin P from the 10 dB Gain Steps circuit. This signal is applied to a chain of three common emitter amplifiers, each using emitter degeneration. A change of the emitter resistance is used to change the amplifier gain under the direction of the microcomputer.

The nominal gain of the complete circuit is -10 dB, with Q2018, Q2042, and Q1062 biased off. This provides a nominal -12 dBm output. In this condition, control pins V and Y are high, causing switching transistors Q2018, Q2042, and Q1062 to be cut off.

Q2018 and Q2042 are turned on, when pin V is low, increasing the total gain of the first two amplifiers 20 dB. Potentiometer R2023 (20 dB Gain) is used to adjust the gain shift of the first stage (Q1025) while the gain shift of the second stage (Q1035) is fixed at +10 dB. This adjustment allows the gain shift to be set exactly to +20 dB.

When pin Y is low, Q1062 is saturated. This raises the gain of the third amplifier (Q1043) by 10 dB. Variable resistor R2060 allows the gain shift to be set exactly to +10 dB.

Gain of the 20 dB and 10 dB gain step circuits is controlled by data bits 0, 1, and 2. Data is latched on the output of decoder U3017, on the VR #2 Mother board and when the bits are high, turns on transistor Q4035, Q3035, and Q4037. The resultant low out, turns on the respective gain step circuit. Table 7-4 shows the state of bits 2, 1, and 0 and the gain shifts of amplifier stages Q2043, Q1025 plus Q1035, and Q1043.

The output signal from the 20 dB Gain Steps circuit is applied through an interconnect coaxial cable to the VR Band Leveling circuit.

Band Leveling Circuit

The two amplifiers, in the Variable Resolution Band Leveling circuit, correct gain variations through the front end. These band-to-band variations are due to the different modulation products out of the 1st Converter and losses through the Preselector.

Table 7-4
GAIN STEP COMBINATIONS

Required Gain Addition	Data Bits			10 dB Gain Step Circuit		20 dB Gain Step Circuit			
	2	1	1	Q2043	Pin N	Q1025 + Q1035	Pin V	Q1043	Pin Y
10 dB	0	0	1	10 dB	0	0 dB	1	0 dB	1
20 dB	1	0	0	0 dB	1	20 dB	0	0 dB	1
30 dB	1	0	1	10 dB	0	20 dB	0	0 dB	1
40 dB	1	1	1	10 dB	0	20 dB	0	10 dB	0

Nominal signal input level for band 1 at 100 kHz resolution, in the Min Distortion mode, is -12 dBm. This decreases some for the higher bands. The output level is about -2 dBm. This output level is kept constant by using the microcomputer to adjust the amplification through this circuit for each band.

The two amplifier stages on this board are similar to the 10 dB gain steps circuits. A stage consists of a three-transistor circuit using a differential pair connected to an emitter-follower. The gain is controlled by altering the feedback network.

The first stage (Q2015, Q2019, and Q1025) has a gain range of 13.5 dB by controlling the bias of PIN diode CR2021 in the feedback loop. Bias for this diode depends on a voltage divider network consisting of an array of variable resistors on the VR #2, Mother board A68A1 with the divider network selected by the microcomputer.

The second stage (Q1031, Q1033, and Q1041) is similar, except the gain change is a one step change of approximately 12.5 dB. This gain step occurs in the higher bands (4 through 11). If required, gain change is activated by the microcomputer through user-selected diodes and transistor Q2046.

The 494/494P is normally calibrated with the band 1 gain control resistor set for minimum gain. Gain is then added as required for the higher bands. Data bits 3 through 6 select gain for each band selection.

The output from this board is applied through connector EE to the 2nd Filter Select circuit.

Digital Control Circuits



The digital control circuits, on the VR #2, Mother board provide address and data decoding for resolution bandwidth, gain step selection, and band identification for the band leveling control.

Address and data valid lines from the analyzer address bus are applied to address decoder U4022. Data bit 7 is applied to the select input A, of the decoder, as a supplemental address bit. This bit is used to select either an address to latch data for the resolution bandwidth selection or an address to latch data for band identification and gain step selection.

Data from the analyzer data bus is applied to data latches U3010 and U3017. Note that only data bits 0, 1, and 2 are applied to latch U3010.

Latch U3010 stores the data that selects the filters in the 1st and 2nd Filter Select circuits. Outputs from pins 2, 19, and 16 of U3010 are applied to the decimal decoders in the filter select circuits through edge connector pins G, F, and E to control the filter selection.

Data that selects gain steps and identifies the selected frequency band for control of the band leveling function is latched on the output of U3017. Output on pins 2, 5, and 6 of U3017 (corresponding to data bits 0, 1, and 2) are applied through transistors Q4035, Q3035, and Q4037, respectively, to the gain switching circuits in the 10 dB and 20 dB Gain Step circuits.

The output on pins 15, 16, 19, and 12 of U3017 (corresponding to data bits 3, 4, 5, and 6) are applied to band decoder U3023, an open collector decoder. If band 1 is selected, pin 1 of U3023 goes low and if band 2 is selected pin 2 goes low, etc. This output in conjunction with a 7.5 V reference source (provided by operational amplifier U3038B and driver transistor Q3036) produces a voltage at the output of a operational amplifier, U3038A. This voltage is indicative of the gain that must be set for each band so the level remains constant at the output for all bands.

The output of U3038A is applied through edge connector pin BB to the gain control PIN diode in the Band Leveling circuit. For example; when band 1 is selected (U3023 pin 1 low), current through Band 1 Gain potentiometer, R2031, and the emitter of Q3036 sets the voltage through R2033 to the summing input of operational amplifier U3038A. The increased output of U3038A increases the current through band leveling PIN diode CR2021 and increases the gain of the stage according to the setting of Band 1 Gain potentiometer R2031. In similar fashion, the other potentiometers (R3034, R3030, R3019, R3022, R3024, R3026, R3032, R3029, and R3028) allow adjustment of the current for each of the other bands.

An additional diode may be added to each decoder output, for bands 4 through 10, to transmit the low, via edge connector pin DD, to the gain control transistor, in the Band Leveling circuit, and increase the gain more for these bands. These diodes are CR3022, CR3023, CR3024, CR3025, CR3031, CR3027, and CR3026. If needed these diodes are installed during instrument calibration.

+5 V Regulator Circuit



The +5 V regulator circuit, U3041, supplies a noise-free +5 V source for the VR system. This is required because of noise in the +5 V main supply.

2nd Filter Select Circuits



Circuits on the 2nd Filter Select board operate in conjunction with the circuits on the 1st Filter Select board to set the overall system bandwidth. Banks of filters are selected under the master microcomputer control. Data bits 0, 1, and 2, from the data bus, are applied to decimal decoder U3070 (which outputs a low on the appropriate output pin to enable the selected filter). Bandwidth selections are 1 MHz to 100 Hz in decade steps and 30 Hz.

Filter bandwidth selection is shown in Table 7-3. Filter selection is accomplished as previously described for the 1st Filter Select circuit except the 100 Hz and 30 Hz filter.

When 100 Hz resolution is selected, pin 6 (output 4) of U3070 is low. Diode CR3068 turns on and pulls line 5 low. Q2020 turns on to enable the 100 Hz/30 Hz path through CR1017. Q3013 is also biased on and shunts R3013 to ground through C4014. When 30 Hz resolution is selected, pin 7 (output 6) is low. Q2020 is again biased on to enable the 100 Hz/30 Hz path. Q3013 is biased off and R3013 is now part of the attenuator network at the input side to the crystal filter FL6015. This decreases the amount of attenuation and offsets or compensates for signal loss when in 30 Hz resolution.

The input signal, from the Band Leveling circuit via jumper EE, is routed through the selected filter to the Post VR Amplifier circuit, via jumper JJ. Nominal loss through the filter circuit is approximately 13 dB, with internal adjustment compensation for variations between the filters. The output level is nominally -14 dBm.

The filter for each bandwidth ranges from no filter at all to a temperature compensated crystal filter. An important difference between the 1st and 2nd filter select circuits is the addition of a gain adjustment in all except the 100 kHz circuit. This adjusts the amount of attenuation through the other filters and matches the output level to that of the 100 kHz filter. Since the Band Leveling circuit furnishes compensation gain to obtain equal signal levels for all bands, this adjustment compensates for variations between the filters.

No filter is used in the 1 MHz path because of the 1 MHz band-pass filter (FL 36) between the 2nd and 3rd Converters and the 1.2 MHz filter in the VR Input stage. An adjustable attenuator, adjusted by R1065, is used to provide initial signal leveling to compensate or offset the gain loss associated with the other filters in the resolution circuits.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C2050 and C5055 provide for filter tuning. A 6 dB attenuator (resistors R2048, R2047, and R2049) is included at the filter input. This attenuator and the filter form a reference to which the levels of the other circuits are adjusted. Impedance matching is accomplished at both input and output by series capacitors C1047 and C6052, respectively.

The 10 kHz filter uses a two-pole monolithic crystal filter. The impedances at the input and output are matched to 50 Ω by T5047 and T7050. An attenuator that contains Gain adjustment R3039 is included at the filter input for filter variation compensation.

The 1 kHz filter is also a two-pole monolithic crystal with impedance matching transformers T4044 and T7043. A gain adjustment is also part of the attenuator.

The 100 Hz/30 Hz filter is a compensated high-Q crystal filter. An attenuator that contains the gain adjustment is included at the filter input for filter variation compensation. A Freq Adjust, R4025 in a voltage divider circuit, calibrates the center frequency of the crystal filter.

Post VR Amplifier Circuit



The Post VR Amplifier circuit provides the final VR system gain to bring the signal to the required +6 dBm output level, and provides the final band-pass filtering. The circuit consists of two stages of gain followed by a filter.

The input signal, at a nominal -14 dBm, is applied through toroid transformer T2063 to the base of common-emitter amplifier Q2056. Gain adjustment R2038, in the emitter circuit, sets the Post VR amplifier gain. The output is transformer coupled, by T1059, to the base of feedback amplifier Q1048. This circuit includes emitter degeneration through resistor R2042 and collector-to-base feedback through resistor R1052. The collector feedback helps to provide a well-defined output impedance of 50 Ω. Input impedance is a function of transformer T1059 and resistor R1058 across the primary winding.

From the final amplifier, the signal is applied through the 1.2 MHz band-pass filter comprised of capacitors C2033 and C2018 and the components between. This filter is a double-tuned design with an insertion loss of approximately 2 dB.

As an aid to understanding the overall VR system functions, it is helpful to understand some aspects of filter design. When designing a wide band-pass filter, on the order of ten percent or greater, stop-band attenuation becomes a severe problem in two-pole filters. The result is that a given filter design will degenerate into either a high-pass or a low-pass filter. The design of the filter in the Post VR Amplifier circuit degenerates into a low-pass unit. However, since the VR system includes a band-pass filter at both the input and the output, and since the input filter in the Input circuit degenerates into a high-pass unit, the overall VR system exhibits clean stop-band performance. The output signal from the filter is applied through coaxial connector J682 to the Log Amplifier. The output level is nominally at +6 dBm.

LOGARITHMIC AMPLIFIER AND DETECTOR



The Logarithmic (Log) Amplifier and Detector accepts input signals from the VR circuits with a dynamic range to 90 dB. The signals are amplified so the output is proportional to the logarithm of the input. The output is then applied to a linear detector which outputs a video signal. By controlling the compression curve characteristics, each dB of change in the input signal level results in an equal increment of change in the output. In the 10 dB/div mode, each division of displacement on the screen represents a 10 dB change of input signal level.

Log Amplifier Circuits

The Log Amplifier circuits logarithmically amplify the input signal from the VR circuits and apply the output signal to the Detector circuit. These circuits consist of seven ac-coupled amplifier stages. Each stage has two gain values that depend on signal amplitude. In addition, the first three stages have an extra automatically selected gain value. The combined circuits provide high gain for low-level signals and low gain for high-level signals. For the output signal to be proportional to the logarithm of the input, more gain is required for a change from -80 dBm to -79 dBm than a change from -1 dBm to 0 dBm. For a given stage of the circuit, the gain starts at approximately 10 dB for a low-level signal and decreases to unity as the input signal level increases. In the first three stages, the gain becomes less than unity as the signal amplitude increases.

Input signal levels nominally range between -84 dBm and +6 dBm. As the signal level increases, the gain decrease begins with the final stage and proceeds, in succession, back through the remaining six stages to the first. Each stage initially produced approximately 10 dB of gain. That gain was reduced to unity, so the total gain reduction is 70 dB. With further increases in input signal level, three more gain change steps take place. The gain of the first three stages is reduced below unity approximately 7 dB for each stage. This reduction starts with the first stage and proceeds to the third, to provide an additional gain reduction of approximately 20 dB.

As the input signal increases from -84 dBm to +6 dBm, the gain through the amplifier decreases logarithmically so that the output signal is exactly proportional to the logarithm of the input. This is accomplished through a system of series diode limiting in each stage, with a second set of diodes for extra limiting in each of the first three stages.

Table 7-5
PROGRESSION OF GAIN REDUCTION

Input Level	Point 1	Point 2	Point 3	Point 4
Beyond Logging Range				
X - 10 dB	0.00316	0.01	0.316	0.1
X Level	0.01	0.316	0.1	0.316
X + 10 dB	0.0316	0.1	0.316	1.0
X + 20 dB	0.1	0.316	1.0	1.684
X + 30 dB	0.316	1.0	1.684	2.368
X + 40 dB	1.0	1.684	2.368	3.052
X + 50 dB	3.16	Beyond Logging Range		

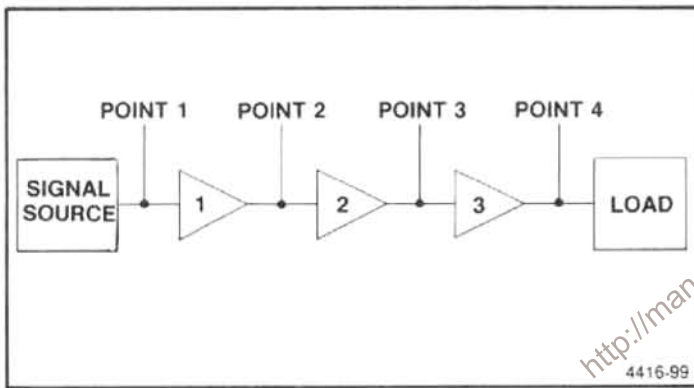


Figure 7-8. Block diagram of a three stage log amplifier.

The following description of a simple three-stage log amplifier, with one gain step in each stage, provides an aid to understanding the concept of a logarithmic amplifier. For the example amplifier described and shown in Figures 7-8, 7-9, and 7-10, the gain of each stage is 3.16 V (10 dB) up to an output level of 1 V peak, then unity for output levels greater than 1 V peak; that is, each stage uses one breakpoint. The breakpoint voltage is used for ease of illustration; the actual breakpoint voltage is significantly lower.

Figure 7-8 illustrates the amplifier and the input signal source. Assume that the source has a step attenuator at the output that allows the input signal to be incremented in 10 dB steps. Table 7-5 shows the progression of gain reduction above 1 V at each amplifier stage output. Note that with each input level change of 10 dB, the output change at point 4 is 0.684 V. The gain curve for one stage is illustrated

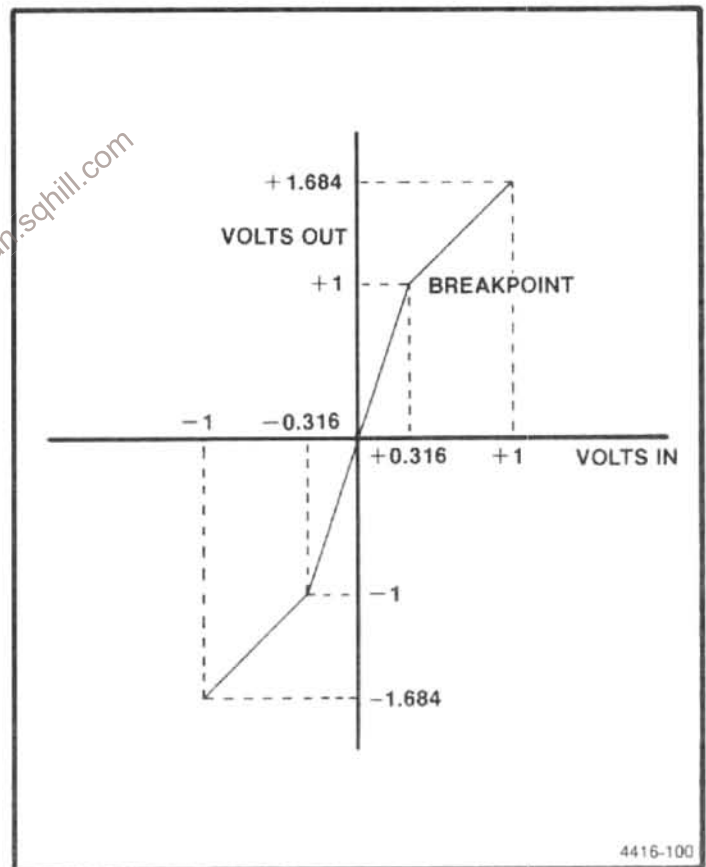


Figure 7-9. Log amplifier gain curve showing the break points.

in Figure 7-9. Also note that when the level at point 1 is increased beyond 1 V, it is beyond the logging range of the amplifier. Similarly, if the input level is decreased 10 dB below the nominal minimum input level, the output increment is

different. A curve of the ends of the logging range is shown in Figure 7-10.

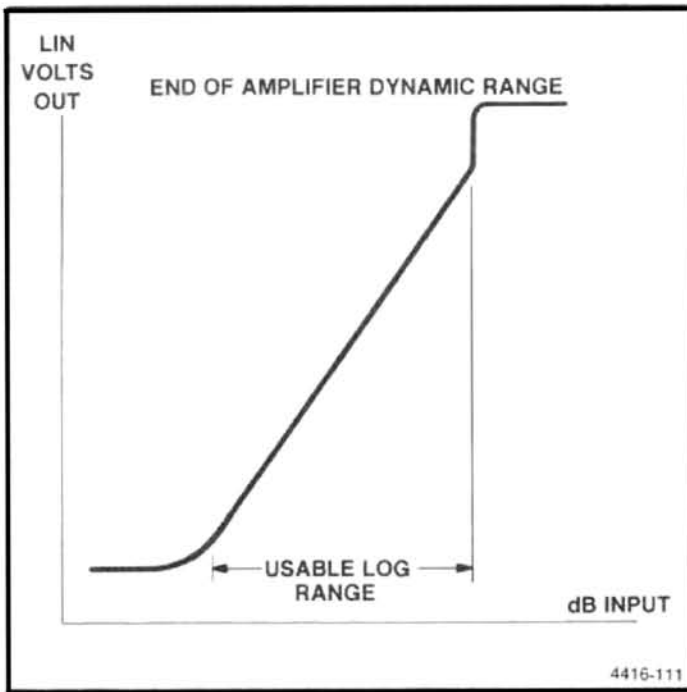


Figure 7-10. Curve showing end-of-range for a log amplifier.

The signal is applied, from the VR circuits, to input pre-amplifier Q3105, in the Log Amplifier circuits, through coaxial connector P621. The input preamplifier provides transfer from 50 Ω to the high-impedance input of the first amplifier stage. The input signal is also applied to transistor Q2105, a common-base amplifier that acts as a buffer to supply the 10 MHz IF signal to the rear panel connector.

From the input preamplifier, the signal is applied to the first of seven cascaded amplifiers that consist of Q3100/Q1095, Q3090/Q1080, Q3075/Q1070, Q3055/Q1050, Q3045/Q1035, Q3030/Q1025, and Q3015/Q6010, plus the associated circuitry. These stages are similar, with the exception the first three stages contain an extra set of diodes for a second gain step.

Typically, when the input level to transistor Q3015 is less than approximately 60 mV peak-to-peak, the transistor conducts enough to maintain forward bias on series limiting diodes CR4015 and CR4012. The RF signal path at that level is through both diodes, capacitor C5014, and resistors R4010H, R4010B, R4015, and R4010D, to common-base amplifier Q6010. The gain of the stage, under these conditions, is approximately 10 dB. As the input signal voltage increases, more current flows through CR4015 to increase the reverse bias of CR4012. This sharply reduces the stage gain to unity. The signal current then flows only in R4010B, R4015, and R4010D. This change takes place during the

positive-going portion of each cycle. The opposite occurs during the negative-going portion of the signal above the minimum input level. As the input signal increases beyond the point at which the gain of the final stage decreases to unity, the same sequence occurs in the preceding stage, Q3030/Q1025, and in succession, back to the first stage, Q3100/Q1095.

Signal levels above this point activate the second tier of gain reduction in the first three stages. Each stage incorporates a second set of diodes that reduces the gain by another 7 dB. In the first tier of gain reduction, reduction started at the last stage and proceeded to the first; in the second tier, the reduction starts at the first stage and proceeds to the third.

In the first stage, diodes CR3089 and CR2087 are forward biased when the stage is in the unity gain mode. Limiting occurs in the same manner as previously described, with a further increase in input signal level, and results in less than unity gain through the stage (approximately 1/3). The one-two-three reduction sequence is established by the values of pull-down resistors R3082, R2076, and R2066.

Detector Circuit

The Detector circuit detects and filters the Log Amplifier circuit output signal and produces the VIDEO signal that is transmitted to the Video Amplifier circuits. The circuit consists of an operational amplifier with a diode detector in the feedback path and a low-pass filter at the output.

Although the circuit is called an operational amplifier, it is not easily recognized as such. It is made up of grounded emitter amplifier Q4025 and a differential amplifier that consists of Q4030 and Q4035. The summing node for the negative input is the base of Q4025 (the positive input is at the grounded emitter of Q4025). Also, the differential amplifier is designed for high impedance output to allow the current that is available from Q4025 to drive the operational amplifier very rapidly during the period when both detector diodes, CR5033 and CR5027, are effectively open circuited; that is, when the output is near 0 V. When neither diode is conducting, it is necessary that the output change rapidly through that zone. Note that the network consisting of resistors R5032, R5029, R5020, and capacitor C5029 is included to stabilize the point of dc operation.

Figure 7-11 shows a simplified schematic diagram of the detector circuit. As shown in this diagram, detector diodes CR5033 and CR5027 are used, but only the negative half cycle is taken as the output (from CR5027). The output from the collector of transistor Q4035 is applied to the diodes through capacitor C5035. Ac coupling is used on both sides of the detector to prevent temperature coefficient effects of

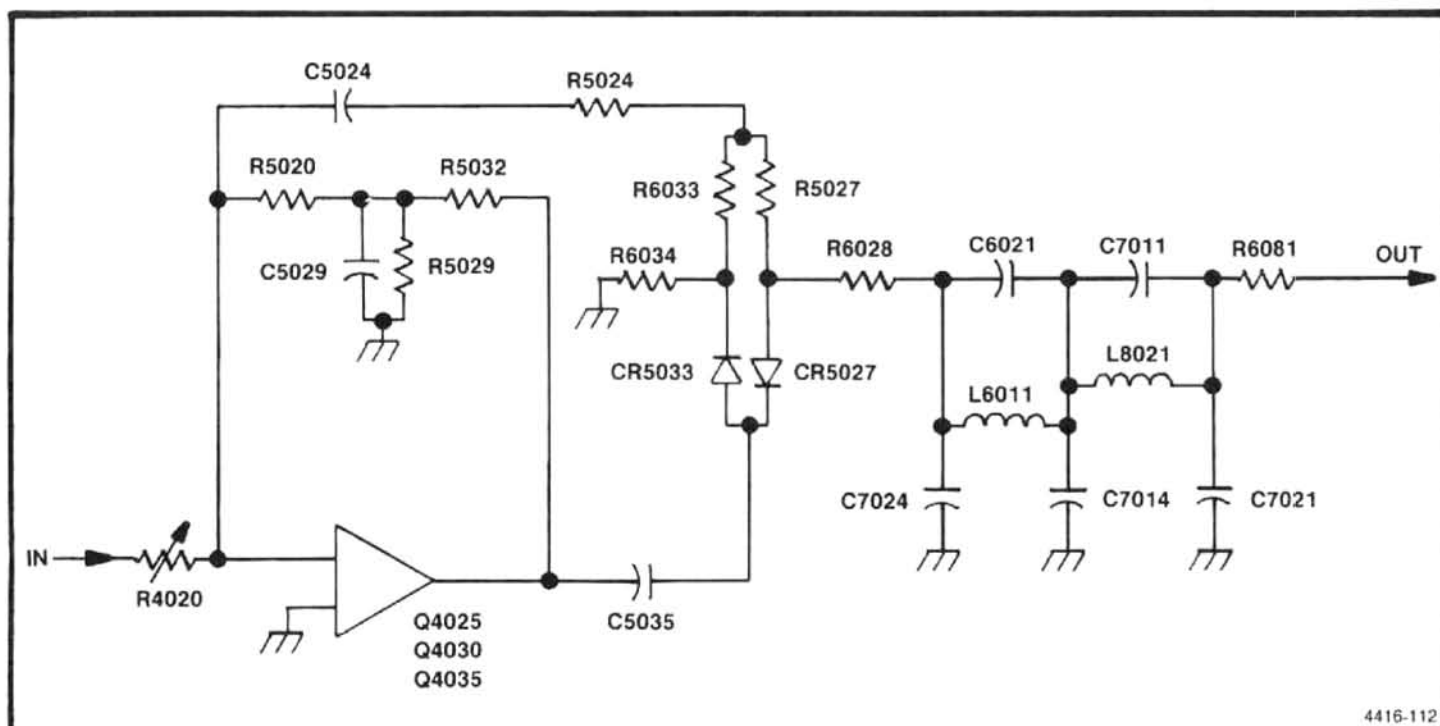


Figure 7-11. Simplified detector circuit.

the operational amplifier from affecting the detector output. This isolation occurs when the detector charges and discharges capacitors C5035 and C5024, by the current induced in each half cycle of the signal without a change to voltage level.

As shown in Diagram 22, the positive-going output signal from the detector to the Video Amplifier is applied through a low-pass filter that consists of capacitors C7024, C7014, C7021; C7011, C6021, and inductors L6011, L8021.

DISPLAY SECTION

FUNCTIONAL DESCRIPTION

The display section consists of the following major blocks:

1. The Video Amplifier processes the detected IF signal through logarithmic gain amplifiers or linear amplifiers for log or linear displays, and provides pulse stretching if selected for narrow pulsed signals.

2. The Video Processor provides band leveling to correct front-end unflatness through the bands, video filtering for noise averaging, out-of-band blanking to clamp the display to the baseline when the sweep is outside the range of the selected band, and video marker capability for use with a TV sideband adapter.

3. The Digital Storage digitizes the video and sweep signals and stores the data in memory. Stored data is then converted to analog signals for the Deflection Amplifier and Z-Axis circuits.

4. The Deflection Amplifier provides the drive voltages for the crt. This includes vertical and horizontal deflection signals as well as readout characters from the Crt Readout board.

5. The Z-Axis circuits receive and decodes data from the microcomputer; accepts control levels from the front-panel beam controls and generates unblanking signals to control the display appearance, brightness, and focus; detects power failure; monitors the instrument voltage supplies; and records the elapsed operating time.

6. The Crt Readout circuits generate the alphanumeric characters (letters and numbers) for the display.

VIDEO AMPLIFIER



Video signals, from the detector and log amplifier in the IF section, are received by the Video Amplifier. In the logarithmic mode, the signals are amplified linearly and applied to the Video Processor. In the linear mode, exponential amplification converts the logarithmic gain characteristic to linear function. In either mode, baseline compensation from the Video Processor is applied to the video signal to compensate for any unflatness in the front-end response. The

pulse stretch circuit at the output of the Video Amplifier alters narrow pulses so data can be acquired and displayed by the Digital Storage logic. Signal amplitude offset circuits provide display offset for the "Identify" mode operation.

Log Mode Circuits

The log mode circuits process VIDEO signal from the Log Amplifier, and add offset for selecting that segment of the log amplifier gain curve to be displayed. The circuits also select screen display gain steps from 1 dB/div to 15 dB/div.

The VIDEO and the VIDEO 1 signals are summed at the input to operational amplifier U4090A. Front-end unflatness is compensated by the VIDEO 1 signals, which are equal and opposite in amplitude to the unflatness. The two signals are also summed with the reference level, set by R4071, and the output of DAC U5041.

U5041 converts the microcomputer commands to an offset signal that selects the location on the log amplifier curve for the display (see Figure 7-12). In dB/div or log display, a change in Vertical POSITION control produces an effect, after the log amplifier, that is the same as a signal level or gain change before the log amplifier. Instead of using a large amount of linear gain before the log amplifier, the output of

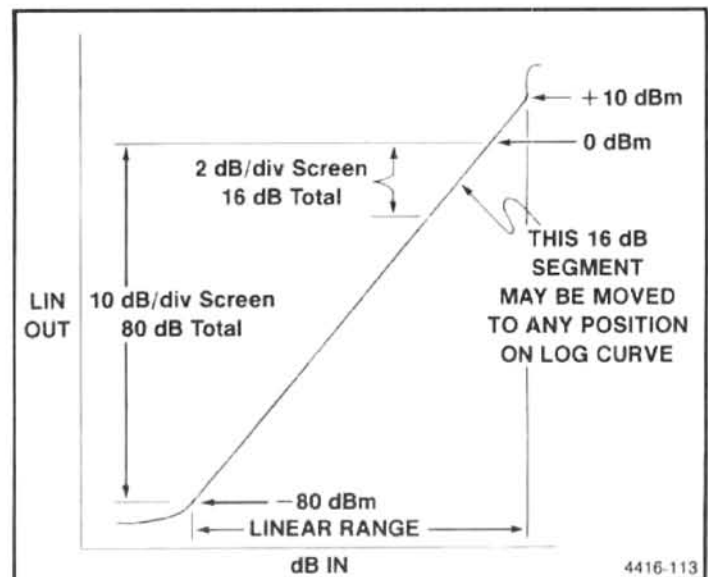


Figure 7-12. Selection of display position on the log scale.

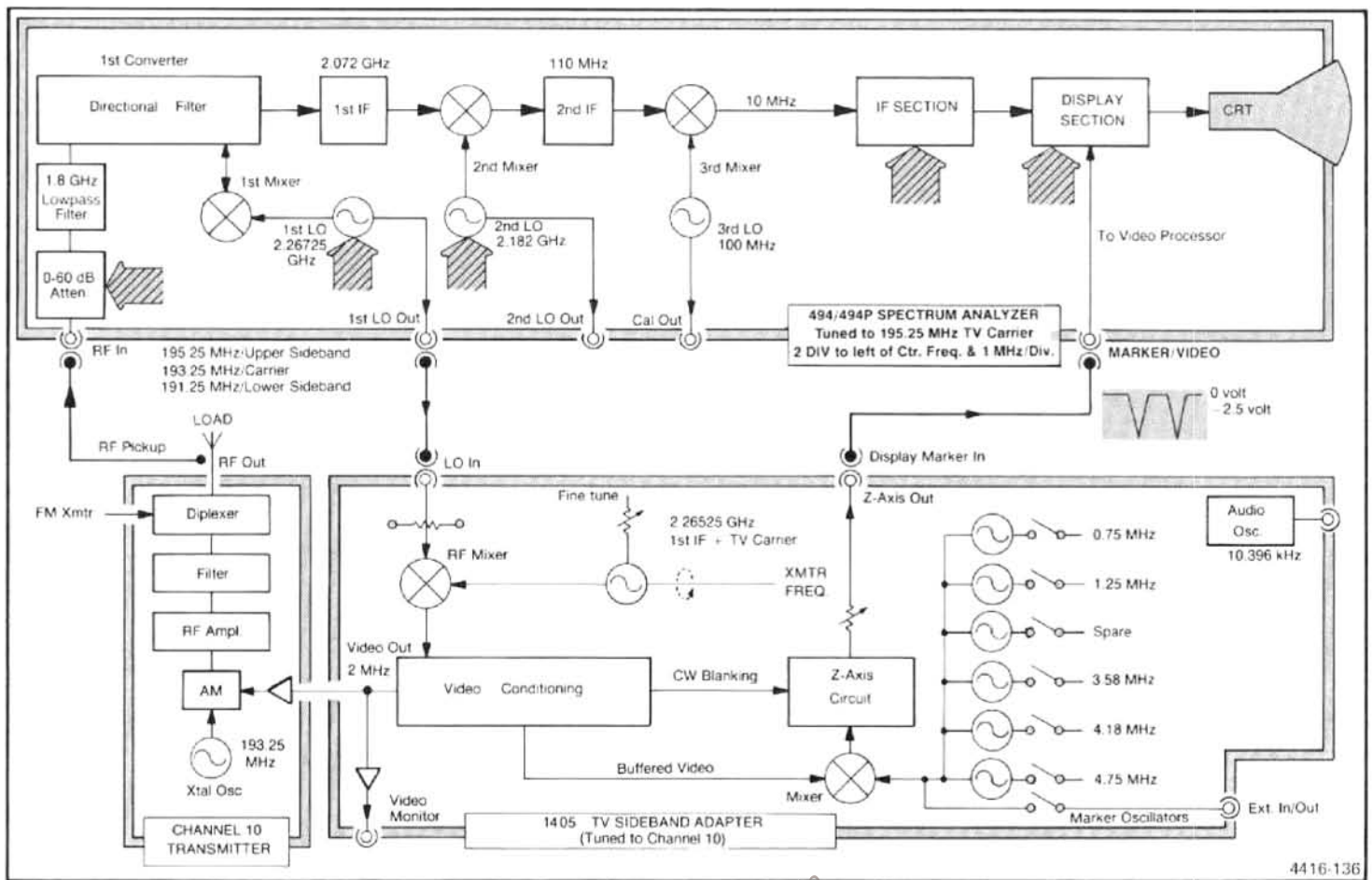


Figure 7-13. Functional diagram showing the 494/494P with the 1405 TV Sideband Adapter System.

mixed with a 2.26725 GHz signal from the 1st LO, forming three products. The subsequent stages of the analyzer accept only the 2.072 GHz product and reject the rest. For frequencies used in this example, the accepted product is the difference between the 1st LO and the upper sideband of the TV signal. The product is converted twice more, amplified, filtered, logged, and detected. This detected signal is applied either directly to the video amplifiers of the crt or to digital storage.

The spectrum analyzer 1st LO signal is applied to the RF mixer of the sideband adapter. The 2.26525 GHz signal from the tunable LO is subtracted from the 2.26725 GHz signal from the spectrum analyzer LO, yielding a 2 MHz product. This video frequency signal is conditioned with sync and blanking signals and applied to the video input of the TV transmitter.

When the 494/494P Spectrum Analyzer is sweeping, the video signal starts at 3 MHz, falls to 0 Hz, and rises up to 7 MHz. During this interval, the analyzer displays the lower sideband as it moves toward the carrier, displays the carrier, and then displays the upper sideband moving away from the carrier. Since the 494/494P and 1405 TV Sideband Adapter

system is similar to a tracking generator system, it rejects noise and uncorrelated signal. This allows normal in-service use of the transmitter by adding a low level (1 to 3 IRE units) cw signal to the video or by using full levels with a VIT inserter.

The sideband adapter can insert frequency markers at preselected deviations from the carrier frequency. Six selectable crystal oscillators have their outputs mixed with video signal and applied to a Z-Axis circuit. This circuit produces two negative pulses as the video signal sweeps through the crystal oscillator frequency. These pulses are applied to the spectrum analyzer marker input, where they appear on the crt as two notches on either side of the marker frequency. The sideband adapter allows the width and depth of the notches to be adjusted with the Width and Intensity controls.

Video Marker

The Z-Axis signal from the sideband adapter is applied to the MARKER input connector on the rear panel of the 494/494P instrument. This negative-going signal is applied through the Accessories and Mother boards to the Video

Processor board. The signal is applied to the emitter of Q4060 and turns the transistor on, which pulls the VIDEO OUT line down. This produces a notch in the video signal of the display to signify the location of the marker on the display.

Video Leveling

A minor slope in frequency response, caused by the 1.86 GHz low-pass filter in the front end, is corrected with band 1 Slope adjustment R1012. When operating in band 1, contacts 6 and 7 of U3025 are closed; therefore, a portion of the PRESELECTOR DRIVE signal is applied to the VIDEO 1 output signal, providing the offset necessary to correct slope difference.

Video Leveler Circuits

Video leveling compensates for analyzer front-end micro-wave circuit characteristics that cause unflat response in band 4 (5.4 GHz to 18 GHz). Since band 4 is a multiplied band, any unflatness is accentuated. Leveling is accomplished through programmable perturbation of the display baseline that is opposite in direction to the flatness error. As the signal power output decreases, the baseline rises an equal amount to compensate, and as power output increases, the baseline falls an equal amount. The perturbation is produced by a normalizer integrated circuit that produces 19 evenly spaced values of the input voltage, with each value corrected to compensate for unflatness.

The PRESELECTOR DRIVE signal from the 1st LO driver circuits is applied to a translation circuit that consists of two current drivers (U3045A and half of Q3038, plus U3045B and the other half of Q3038). The PRESELECTOR DRIVE signal is directly related in amplitude to displayed analyzer frequency. The nominal +10 V to -10 V excursion voltage versus frequency curve, in maximum span, relates to the full bandwidth. This 20 V maximum excursion is scaled to a precise current (from 1 mA at +10 V to 0 current at -10 V) that is applied to the normalizer IC to generate the baseline perturbation. Actual signal scaling is done by current driver U3045A/Q3038. The output signal is applied to the normalizer SWP IN input, pin 5 of U2039. The second current driver, U3045B/Q3038, generates a 2 mA reference current for the normalizer. Horizontal Freq adjustment R1069, in the input translation circuits, shifts the 19 evenly spaced points up or down in frequency to compensate for unflatness.

Normalizer IC U2039 operates as a shaper and contains 19 bi-polar transistors that turn on and off in sequence as the current input to pin 5 decreases from 1 mA to 0. The collector of each of these IC transistors is connected to a

potentiometer that allows output trimming as shown on Diagram 24. Potentiometer R1061 is active with no current, and R1013 is active at 1 mA. The trimming operation is described later.

From the normalizer, the output is applied through a jumper switch to buffer amplifier U2055B, which has a gain of five, then to offset amplifier U2055A. This amplifier has a gain of two, but its primary purpose is to offset the 0 to +5 V (normal), 0 to -5 V (invert), buffer output to the levels required by the Log Amplifier circuits. The range required by the Log Amplifier is 0 to -10 V. The output voltage is a series of linear interpolations of the voltage between adjacent trimming resistors at the outputs of the normalizer. Compensation adjustment R3030 sets correct interpolation.

Jumper plug P2060 selects the input side of buffer amplifier U2055B and proper offset voltage for U2055A. This provides the means to invert the buffer output during the instrument adjustment procedure. The adjustment procedure is described in that section of this manual.

As previously noted, only band 4 requires significant compensation. Selection of band 4 is indicated by data bit 0 switching to a 1 (see the Leveling table at the top right corner of Diagram 24). When DB0 is a 1, pins 3 and 2 of switch U2015 are connected, and the output from offset amplifier U2055A is supplied out as the VIDEO 1 signal.

Minor compensation is required for Band 1, to correct a minor slope caused by the 1.8 GHz low-pass filter and 2 GHz limiter. When pins 6 and 7 of switch U3025 are connected, the PRESELECTOR DRIVE signal is offset by R4023 and R4011 and Band Slope adjustment R1012 to provide an attenuated negative-going ramp to the VIDEO 1 output line. Switch U3025 is controlled by inverter Q4025. Q4025 is activated by data bit 6 going low. As shown in the Video Blanking table on the schematic diagram, DB 6 is 1 except when Band 1 is selected.

Video Filter Circuits

Video filtering provides selection of one of six bandwidths, under microcomputer control. As shown in the Video Filter table on Diagram 24, data bits 1 through 4 select any of six bandwidths: 30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz. Either wide or narrow-band filtering is selected at the front panel (Wide band is defined as 1/30th of the selected resolution bandwidth and narrow is defined as 1/300th of the resolution bandwidth). The microcomputer makes the selection, based on such factors as sweep rate and total dispersion. With no video filtering (all data bits are 0), the video system bandwidth is 500 kHz.

Two signal inputs (EXT MARKER/VIDEO) can be applied to the video filter circuits. The EXT VIDEO signal, from the rear-panel MARKER/VIDEO connector, is applied to pin 15 of switch U3063A through edge connector pin 53. The INTL VIDEO signal, from the Video Amplifier circuits (via the front-panel LOG CAL control), is applied to pin 2 of switch U3063A through edge connector pin 51. Note that the internal video sections of switch U3063A are normally held energized (pins 2 and 3 connected, pins 15 and 14 disconnected) by the +5 V supply through resistor R3064. If the EXT VIDEO SELECT line (from the rear-panel ACCESSORIES INTERFACE connector, through edge connector pin 55) is grounded, the external video section of U3063A are de-energized. When this occurs, the EXT VIDEO signal is applied through, or around, the filter to become the VIDEO FILTER OUT signal at edge connector pin 57. This is shown in the simplified schematic diagram of Figure 7-14.

As shown in Figure 7-14, when no filtering is selected (all data bits are 0), either the internal or external signal is routed through U3062 and around the filter, because the two sections of U3063B is selected by DB1. When DB 1 is high, the video is routed through the some filter value will be selected by bits 2, 3, and 4. These data bits control three sections of switch U2015B to add or delete filter time constant.

The filter consists of resistors R2023, R2021, R2022, and capacitors C3026 and C2016, connected between U3062 and U2066. Table 7-6 lists the filter components in the circuit for each of the six bandwidths. Data bits 2, 3, and 4 are applied to switch U2015B (pins 8, 16, and 9) which selects the components. From U2066, the signal is routed through contacts 7 and 6 of switch U3063B to edge connector pin 57 as the VIDEO FILTER OUT signal.

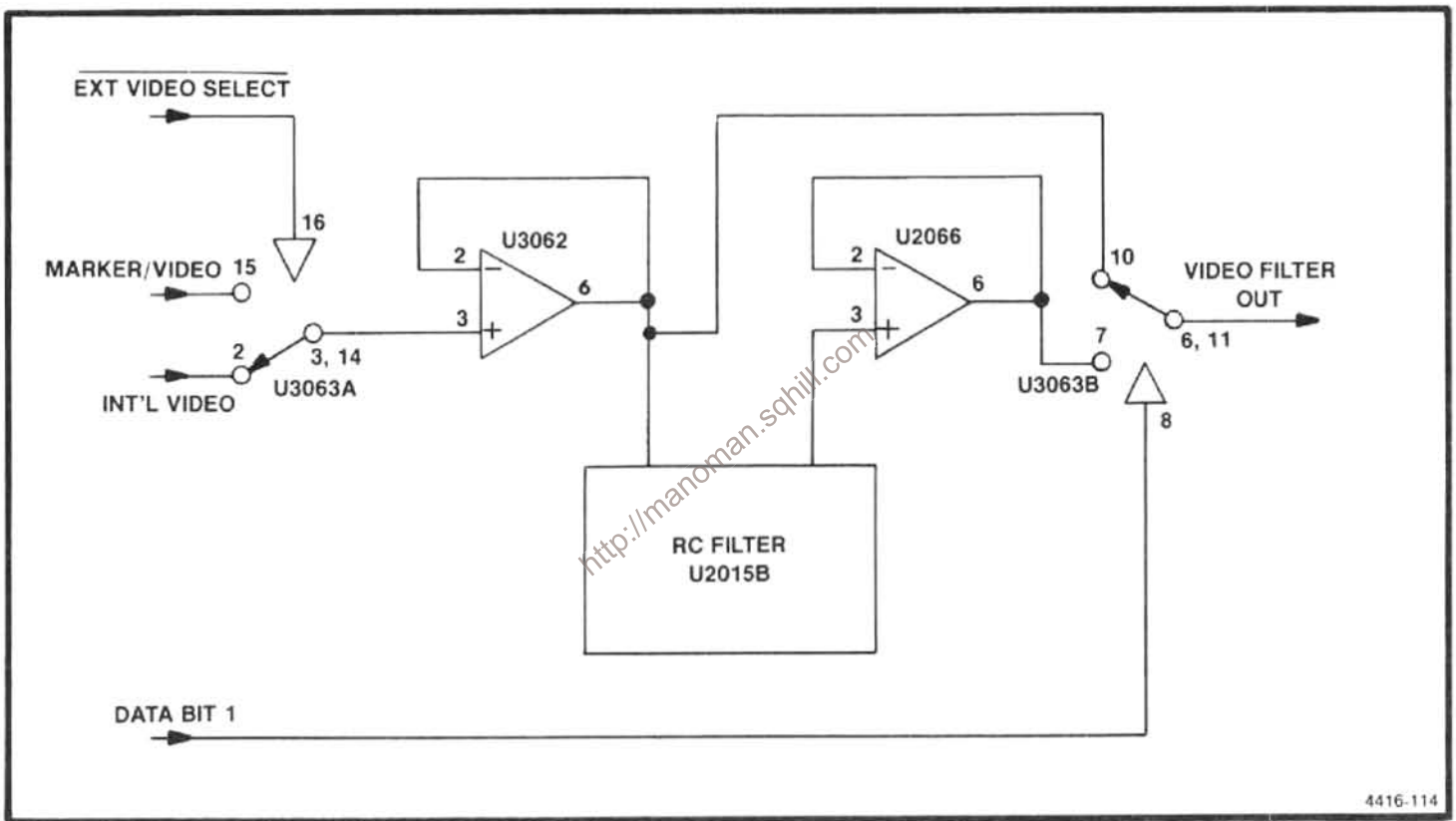


Figure 7-14. Simplified diagram of a video filter.

Table 7-6
FILTER COMPONENT COMBINATIONS

Bandwidth	DB=1	R2023	C3026	R2021	R2022	C2016
30 kHz	1	X	X	X	X	
3 kHz	1, 4	X	X	X		
300 Hz	1, 3, 4	X	X			
30 Hz	1, 2	X	X	X	X	X
3 Hz	1, 2, 4	X	X	X	X	X
0.3 Hz	1, 2, 3, 4	X	X	X		X

Video Blanking Circuits

The video blanking circuits allow selective blanking of the lower and upper ends of the local oscillator range. Selective blanking is required because the local oscillator sweeps the full span regardless of the band limits. The video system is designed to effectively open a display window only during the time for display. Data bits 5, 6, and 7, under control of the microcomputer, select the appropriate amount of display for each and.

Video blanking and the PRESELECTOR DRIVE signal (which provides frequency information, in voltage form) are located on the Video Processor board. Switch U3063 incorporates a disable function that, when provided a low input, opens all switch sections regardless of individual section input. This feature allows the VIDEO FILTER OUT signal to be easily blanked at will.

This disable function is controlled by a combination of outputs from comparators U3015A and U3015B. Inputs to these comparators are from the PRESELECTOR DRIVE signal and a combination of voltage dividers that are switch selected under control of data bits 5, 6, and 7. The PRESELECTOR DRIVE signal is applied from edge connector pin 54 through divider resistors R4013 and R4012 to the minus input side of U3015A, and through divider resistors R4014 and R4011 to the plus input side of U3015B. These dividers reduce the +10 V to -10 V excursion of the drive signal to +2.5 V to -2.5 V, which is the maximum input level to the comparators.

Input to the plus side of U3015A is from divider resistors R3011, R3012, and selected resistors R4024, and R4015. The inclusion of R4024 is controlled by DB5, through pins 15 and 14 of U3025, and R4015 is added by DB 7, through pins 2 and 3 of the same switch. The junction of divider resistors R3011 and R3012 may be connected to -5 V through R4024 or to ground through R4015. Refer to the Video Blanking table on the schematic diagram for data bit states for different bands.

Input to the minus side of U3015B is from divider resistors R4018, R4017, and selected resistor R3028. The inclusion of R3028 is controlled by DB6 through pins 10 and 11 of U3025. The junction of R4018 and R4017 is connected to +5 V through R3028 when it is selected. This switching arrangement of negative and positive levels for comparison with the reduced PRESELECTOR DRIVE signal enables the top and bottom extremes of the frequency excursion to be blanked. The blanking is activated by the disable function of switch U3063, which is microcomputer controlled.

DIGITAL STORAGE



The Digital Storage circuits select the display and process methods for information contained in the digital storage memories. This includes determination of the highest amplitude that occurred during a selected period (Max Hold mode), storage of a signal for later examination (Save A mode), subtraction of one signal from another (B-Save A mode), signal averaging (Averaging mode), and signal comparison (View A and View B modes). Two memories are used independently in these operations to store two complete signals that are each digitized at 512 points across the sweep. Therefore, two signals may be observed simultaneously or processed in separate ways.

In the Max Hold mode, the highest amplitude at each of the 1024 points in successive sweeps is stored and displayed. In the Save A mode, a signal is stored in one memory for later examination, and is not updated. In the B-Save A mode, the A signal is stored and not updated, then arithmetically subtracted from the B signal, which is stored, but continually updated. In the averaging mode, the display area is divided by a horizontal cursor. Signals above the cursor are peak detected and displayed, and signals below the cursor are averaged. In the View A and View B modes, the contents of the selected memory or memories are displayed.

Graphical presentation of mathematic functions or experimental data is common. One such graph has a single Y value for each X value. An alternate presentation of the data in this graph would be a table simply listing the X coordinate values along with a corresponding Y value for each X value. To further simplify the graph, if the first X value and the spacing between X values were known (all spaces assumed equal), the two-column table could be reduced to a single column with the X value implied by the position of the Y value in the column. This is the essence of digital storage—to convert a vertical analog voltage (Y coordinate value) to a binary number and insert that number in a stored table. The location of the Y value in the table is determined by the analog sweep voltage (X coordinate value) binary conversion. Once a set of binary numbers that represent values across a waveform is stored to create a table, the waveform can be recreated at any time by conversion of the table values (Y) and positions (X) back to analog voltages that represent amplitude and sweep positions.

The digital storage system uses a Table A and a Table B. Table B is updated every sweep. Table A is also changed unless the Save A mode is selected. There are 512 A values and 512 B values. The spacing between values is the same throughout both tables, but the starting point for Table B is shifted slightly so that when both tables are read, the read-out values are interlaced.

When the signals are recreated, the contents of either Table A or Table B can be displayed, or both tables A and B can be displayed. If both Tables A and B are to be displayed, and the Save A mode is selected, the contents of both Table A and Table B are drawn, each display in its own trace. If the Save A mode is not selected, the contents of both Table A and Table B are displayed on one trace, with 1024 value positions across the screen. A third trace option is also available. In the B—Save A mode, the displayed values are those that result from an arithmetic operation and are the difference between the contents of Table A and Table B for each X value of analog sweep voltage.

Since a signal waveform is continuous and a table has discrete X values, an algorithm determines the Y value to be stored for a particular X value. This allows the operator to select one of two methods to determine Y values; peak or average. The Y analog voltage is continuously sampled, with the sampling rate dependent upon sweep speed. For each X value, there are always at least two samples, and there may be as many as 2^{17} samples. From this set of samples, either the largest sample value (peak value) or the mean of all the samples (average value) can be selected. Selection between peak and average is controlled by the front-panel PEAK/AVERAGE control, which sets a dc level that is compared with the analog vertical input to produce the PEAK/AVG logic signal. When the input signal is below the level selected by the front-panel control, the signal is averaged; when the input is above that level, the peak signal is displayed. The dc level appears on the display as a positionable horizontal line. This marker line is created when the dc level to the analog output line is switched during the marker cycle to produce the MARKER logic control signal.

Superimposed on the marker line is an intensified spot called the update marker, which indicates the X value at which new Y values are being computed for display update. The update marker is formed when the analog sweep input is compared to the display analog X output. When the two are the same value, the sweep is forced to pause, which increases the marker intensity at that point. Refer to the block diagrams adjacent to Diagrams 25 and 26.

U1023 and U2032 are the heart of the digital storage circuits. U1023 contains the vertical acquisition and display logic, peak detection, signal averaging, Z-Axis blanking, and special Y-value processing circuits. U2032 contains the horizontal acquisition address counter, horizontal display counter, 10-bit RAM address multiplexer, and a programmable logic array system control matrix. The remainder of the digital storage control circuits consists of two 8-bit digital-to-analog converters, two 10-bit digital-to-analog converters, one 10-bit latch, 8k bits of random access memory, and various auxiliary circuits. Timing is controlled by $\phi 2$ clock pulses (at 1 MHz) from the Processor board to the Horizontal Digital Storage board.

Vertical Section



Vertical Control IC block diagram is shown in Figure 7-15. The vertical analog voltage is converted to a Y binary value by an 8-bit successive approximation register. Nine clock cycles are required for each Y conversion. After the conversion has taken place, the successive approximation register produces the negative-going SYNC signal. Most functions on both the vertical and horizontal control ICs are synchronized by this signal. On the negative-going transition of SYNC, the successive approximation register is reset to 10 00 00 00 (binary) and the next conversion cycle begins. Incoming data bits are latched into the register on the negative-going clock transition. From the register, the output data is applied to the peak and the averaging circuits.

The averaging circuit consists of three groups of circuits; those that accumulate all of the Y values for a given X value into a grand total (called the numerator), those that count the number of samples that make up the numerator (this total is called the denominator), and those that subtract and shift to perform the division process.

As each new Y value is converted, it is added to the eight least significant bits of the numerator. Each carry from the most significant bit of this addition is counted by a 17-bit ripple counter. The contents of this counter and the 8-bit sum are cascaded to form a 25-bit grand total. Each time a new sample is added to the numerator, another 17-bit ripple counter is incremented to produce the denominator.

A division cycle is initiated when horizontal control IC U2035 detects a change in the X value. At that time it generates the ST DIV (start divide) signal. Upon receipt of this signal, and in synchronization with the SYNC signal, vertical control IC U1023 performs five functions (refer to Figure 7-15).

1. U1023 latches the current numerator in a 25-bit latch (25-to-1 data concentrator in Figure 7-15) and latches the denominator in a 17-bit latch (17-to-1 data concentrator).
2. U1023 clears the numerator adder circuits (25-bit summation register in Figure 7-15).
3. U1023 performs a 17-bit priority encode on the denominator and loads a 1 in the appropriate cell of the 25-bit shift register.
4. U1023 loads the latched numerator and denominator serially into the divide circuit (subtractor in Figure 7-15) using the contents of the 25-bit shift register as a mask.

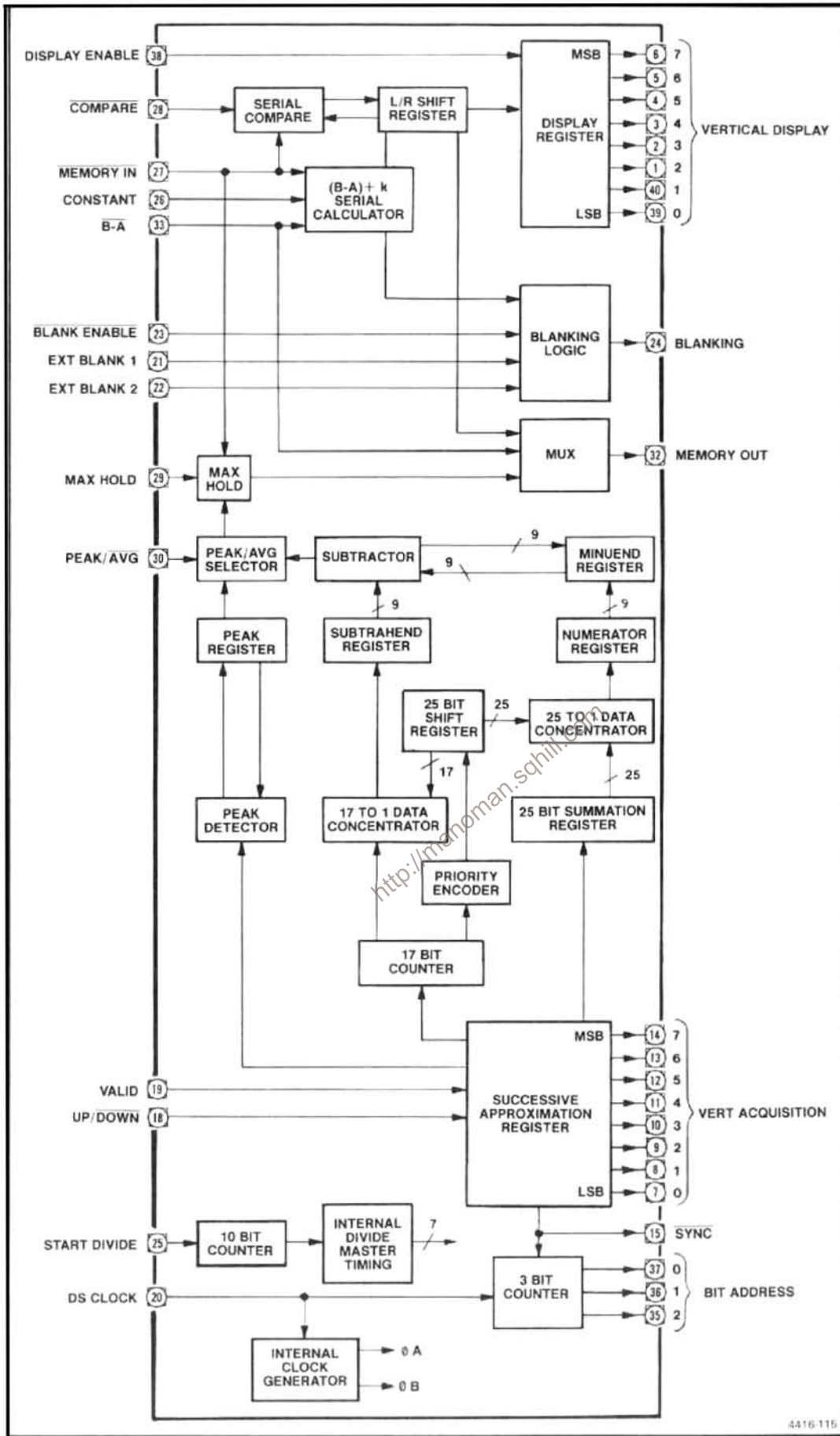


Figure 7-15. Vertical control IC, U1023, block diagram.

5. U1023 clears the denominator ripple counter (17-bit counter in the block diagram) to zero.

Ten clock periods are required to load the numerator and denominator into the divide circuit. The cycle starts on a SYNC pulse. The first bit of the quotient is available shortly after the first clock pulse that follows the next SYNC pulse. Division is performed by repeated subtract and shift operations. The quotient is arrived at serially with the most significant bit first. Since only 8-bit accuracy is required, with the priority encoder output used as a mask, the divider circuit is loaded with the 8 most significant bits of the denominator and the 16 most significant bits of the numerator. (Ripple borrow for a 17- by 25-bit subtractor would be so long as to be impractical.)

The peak circuit consists of a peak detector and an 8-bit peak shift register. In operation, the previous peak Y value from the last set of samples is still stored in the peak shift register at the start of a conversion cycle. At that time, the peak detector, which is a serial compare circuit, is set to the state that questions whether the old or new number is larger. Each bit of the new value is then compared with the corresponding bit of the old value, most significant bit first. When one value is found to be larger, a flip-flop is set and the smaller number is gated out of the shift register. The start divide logic signal being true then forces the peak detector to select the new value and ignore the number in the shift register.

The peak/average selector, a multiplexer, selects either the peak or average value to be routed to the memories under control of the PEAK/ $\overline{\text{AVG}}$ signal. The selector output is routed through the Max Hold circuit, which functions in the same manner as the peak detector. When the MAX HOLD signal is high, the value that is routed to the output multiplexer is the larger of two values; the current memory value at the subject X coordinate or the previously-selected peak or average value.

Timing to set up the divide operation and clear the numerator, denominator, and peak circuit is controlled by a 10-stage Johnson counter. NOR gate taps are taken from appropriate stages to develop the necessary clear and latch timing pulses. Because the denominator is loaded into the divide circuit using a priority encoder, the most significant bit is always a 1. Space and power are saved by modifying the subtractor and not storing this 1.

All data enters and leaves the memory serially. Data read from memory enters an 8-bit shift register and, timed by the SYNC signal, is transferred to the vertical display output latch (display register on Figure 7-15). The same shift register is used for other purposes, so the DSPL EN (display enable) signal prevents non-display information from being

transferred to the output latches. An example of data moving through this shift register is seen in the B—Save A display mode. The A value is first read from memory and stored in the shift register. As the B value is read, the subtraction is done serially and the answer is applied to the shift register. Since the subtraction must be performed with the least significant bit first, a set of exclusive-OR gates change the order of extracting B from memory. The shift register direction is reversed to present the most significant bit to the proper display latch. The shift register output is also applied to the output multiplexer.

In subtraction, the operation performed by the serial calculator is not merely B minus A. The actual expression implemented is $(B - A) + K$, where K is a serial input external constant specified by the user. This permits zero to be placed anywhere on the screen. To avoid confusion when $(B - A) + K$ results in an off-screen position, the subtractor blanks the display. (The subtractor examines the carry bit and borrow bit when the most significant bit is calculated. If either bit is a 1, the screen is blanked.)

When the Save A mode is not selected and both A and B are being displayed, maximum resolution is obtained (1024 points across the display). If this display includes a very narrow pulse, it is possible that the top of the pulse is only as wide as a single X coordinate (2^{17} samples). If this maximum value were in the B Table and the Save A mode was selected and B turned off, there would be an apparent drop in amplitude. For this reason, when the Save A mode is selected, a special set of circuits in U1023 compares all A and B values that have the same X value, and stores the larger in Table A. The B value is read and stored in the display shift register. Then, as the A value is read, it is compared with the B value and the larger of the two is loaded into the display shift register. Finally, the number in the shift register is written into memory. This operation is performed once each time that the Save A mode is selected.

Vertical control IC U1023 contains a 3-bit synchronous counter that identifies the specific bit of an 8-bit vertical value that is to be read from memory or written into memory. This is the only memory addressing that is performed by U1023. All other addressing is performed by horizontal control IC U2035.

Digitizing Circuits. The input vertical signal, VID FLTR OUT, coupled through edge connector pin 60 is applied through buffer U2033 to sample and hold switch U1033C. U1033C is controlled by flip-flop U1011B. Flip-flop U1011B generates the sample pulse, and is enabled during the clock cycle after the last sample, as indicated by the least significant bit from the successive approximation register in U1023. The switched sample is then applied through buffer U2032 to a summing junction. At this point, the output current from digital-to-analog converter U2024, that is supplied

from the successive approximation register, is subtracted from the sample current. The difference current is then applied through comparator U1031B and synchronizing flip-flop, U1017A, to pin 18 of U1023 as the UP/DOWN signal. The binary equivalent of the input sample is effectively produced by the combination of the successive approximation register, the digital-to-analog converter, and the sample and hold circuit.

Address Decoding. The address decode logic accepts inputs from the address bus and produces the control signals for read and write operations; CONT W (control write), DATA W (data write), and DATA R (data read). The control write signal is used to gate the control word from the data bus into control register U1022 to generate mode control signals. This control word consists of five bits that represent front-panel functions. If output Q6 is low, a peak operation is forced; if output Q6 is high and Q7 is low, an average operation is forced. The data read and data write signals are applied to the interface logic to control memory read and write operations.

Interface Logic. The interface logic, in general, performs control and interface functions between the active data circuits in the vertical and horizontal sections and the rest of the 494/494P. It allows the microcomputer to control the storage system functions and to access the digital storage memory. It also contains the circuitry for serial-to-parallel and parallel-to-serial conversion. (The microcomputer uses parallel transfer; the digital storage memory uses serial transfer.) Shift register U2021 is used to read data from memory to the data bus. Register U1021 is used to store information from the data bus for transfer to memory. Multiplexer U2016 performs the parallel-to-serial conversion and applies the data output to gate U2015B, which acts as a buffer to supply either the multiplexer output or the MEM OUT (memory output) signal from U1023 to the memory as the DSDI (digital storage data input) data train.

The interface circuit group on the Vertical Digital Storage board is the handshake logic that works with the horizontal control circuits to access the memory and to determine when to increment the memory address counter. In either a data read or data write operation (when the corresponding signal goes high), flip-flop U2014B is triggered. This releases the BUS REQ (bus request) line to allow that signal to go high and signals the horizontal control circuit that memory access is required. When the horizontal circuits recognize the request, those circuits pull the BUS REQ line low at the same time that SYNC is low. The interface logic detects the BUS REQ and SYNC low condition through U1013A, U1013B, U2011A, and U2012A, and produces the low BUS GRANT signal to indicate memory access. The BUS GRANT signal then enables shift register U2021 to shift data from memory or enable register U1021.

BUS GRANT also enables multiplexer U2016 to shift data to memory as indicated by the DATA R and DATA W lines. At the end of a data read cycle, gates U1012B and U2023C produce the INCR ADRS (increment address) signal to increment the address register in the horizontal circuits.

Maximum Hold. As described previously, when the Max Hold mode is selected, the signal from Q5 of control register U1022 causes the circuits in U1023 to compare the binary equivalent of the input signal for a given X value with the information in memory for that same X value. This causes the larger value of the two to be stored in memory. The signal from Q5, in combination with the VALID signal from the horizontal circuits, produces the MAX HOLD command to U1023 through buffer U2023E and gate U1025A.

Constant Circuit. As described previously, in the B—A operation, a constant is used. This constant is selected internally with switch S1014. This switch, in combination with multiplexer U1015, supplies the CONSTANT data to U1023. Multiplexer U1015 is, in turn, controlled by address bits 0, 1, and 2 to provide the proper constant data bit to U1023.

Output Circuits. From the U1023 vertical display register, the parallel data output is applied to 8-bit digital-to-analog converter U1024. The converter output is then applied to the output storage/cursor switch, U1033B, through a vector generator that consists of an integrator (U1032 and C1031) with an associated feedback loop sample and hold circuit. Integrator U1032 has a time constant that provides a ramp to last between the existing sample and the new sample (that is, between sync pulses). Circuits U1033A and U1034 and capacitor C1038 make up a sample and hold circuit with U1034 acting as an output buffer. From U1034, the output current through resistor R1032 subtracts from the digital-to-analog converter output current to modify the slope of the output ramp. The output of the vector generator is then applied to switch U1033B. U1033B, controlled by the MKR (marker) signal from the horizontal section, selects between the recreated video signal from U1032 and a dc (Peak/Average) level from buffer U2034, to be sent out as the vertical signal. The dc level is displayed only during retrace as the PEAK/AVERAGE cursor.

Peak/Average Level Circuits. The buffered PK/AVG LVL signal, from U2034, is compared with the sampled Video Filter Out signal, from U2032, by comparator U1031A. The output of U1031A is a high (1) if the Video Filter Out signal is greater than the PK/AVG LVL, or low if it is less. This output commands U1023, via U1025C and U1025D, to send peak or average data to the output. U1025B, C, and D are used if the instrument is under GPIB control to select one of three possible modes; Peak, Average, or front panel control knob.

Horizontal Section



Figure 7-16 is a block diagram for the Horizontal Control IC U2035. The horizontal analog voltage is converted to a current table value through a 10-bit tracking analog-to-digital converter, which consists of up/down interlock and 10-bit up/down counter in U2035, and external 10-bit digital-to-analog converter U2042. As the sweep moves right, the counter increments; as the sweep retraces, the counter decrements. Each time the counter increments, it generates a new X coordinate value (the D to A input) and a ST DIV (start divide) signal to start the storage cycle. The increment clock is the SYNC signal, and the decrement clock is the basic digital storage clock divided by two. When the Save A mode is selected, the counter skips every other binary number, so only B coordinates appear as addresses.

A programmable logic array ROM state device (PLA) provides the horizontal system intelligence. This PLA determines which trace is to be written on the screen, determines when to switch from read to write, generates the B-A coordination signals for vertical control IC U1023, controls the incrementing of the 9-bit display counter, and processes requests for the memory bus. The only one of these functions that is not obvious is the memory bus request.

When an external device elects to read from or write to memory, it allows the BUS REQ (bus request) signal to go high to request permission from the PLA. When the time becomes available, the PLA pulls the BUS REQ line low, which signals the start of a request cycle. For the next eight clock cycles, the internal multiplexer output lines are driven to the high impedance tri-state mode.

The combination of the up/down interlock, 10-bit up/down register, 9-bit display counter, and horizontal display multiplexer constitute the primary circuits that either write to or read from memory. To generate X values to be written into memory, the circuits convert the sweep voltage to binary form. These circuits also count the sync cycles to cause the external logic to read stored data from memory and produce a vertical signal (Y value) for each corresponding X value.

During acquisition cycles, the 10-bit up/down counter, controlled by the up/down interlock, operates in a loop with the external 10-bit digital-to-analog converter. This allows the counter to acquire the equivalent (X value) of a sample section of the sweep voltage. From the counter, the 10-bit output is applied to the 10-bit up/down register. During display cycles, the 9-bit display counter counts sync pulses to acquire the X value. Either the 10-bit up/down register output or the display register output is applied to the horizontal multiplexer under control of the SELECT signal from the PLA. From the multiplexer, the output is applied to the memories as an address.

Address Registers and Buffers. Registers U2023, U2016, and U2014 perform address counting for bus transfer. These registers count INCR ADRS (increment address) pulses after having been reset to zero by the CONT W (control write) signal from the vertical section. From the address register, the outputs are applied to tri-state buffers U1023 and U1016. Then, the 10 bits of address from the counters are buffered as well as the DS R/W (digital storage read/write) signal line from the vertical section interface logic. Those signals are multiplexed onto the HD (horizontal display) lines and R/W (read/write) line to the memories. These buffers are enabled only during the bus grant portion of the cycle for display of memory data. At all other times, horizontal control IC U2035 outputs control the HD lines to determine the memory address for update of memory data.

Tracking Digital-to-Analog Converter. The 10-bit digital-to-analog converter operates as part of the loop that acquires a binary equivalent of the SWP (sweep) input signal from the Sweep board. Converter U2042 accepts the output from the 10-bit up/down counter of U2035 and converts that output to an analog current. The analog current is then subtracted from the SWP signal (which is applied at edge connector pin 60 through buffer U2047B). The result of this subtraction is supplied to up comparator U1045A and down comparator U1045B. This creates the UP or DOWN signal, as appropriate to control the count direction of the 10-bit up/down counter in U2035. The counter then counts in the appropriate direction, which changes the digital-to-analog converter output to reflect the proper value. Overflow detector U1035 and underflow detector U1041 prevent the counter from counting too high or too low.

Update Marker Circuits. From U3025, the HD (horizontal display) signals are applied to 10-bit latches (U1022 and U1027) and clocked into the latch with DSPL EN. When DSPL EN is high, it indicates that the data currently in the vertical shift register in U1023, on the Vertical Digital Storage board, is to be displayed by shifting the data to the vertical display output latch in U1023. Lack of DSPL EN indicates that the display latches are not to be changed. The outputs of these latches are applied to 10-bit digital-to-analog converter U1042. The output current of the converter is applied through buffer U2047A, where it is converted to a voltage called HORIZ SIG. HORIZ SIG is a voltage that is sent to the Deflection Amplifier to deflect the crt beam horizontally when digital storage is being displayed. HORIZ SIG is compared to the sweep voltage in U2043. The output of the comparator is applied to a one shot multivibrator U1014A. The period of this one shot is determined by counter U2024, which is incremented by the rising edge of DSPL EN (display enable) from the PIA in the horizontal control IC U3025. The rising edge of the output from U1014A produces the INTENSITY signal that temporarily prevents counting by the 9-bit display counter in U2035. This effectively stops the beam for a short time and causes a bright spot on the marker trace (cursor) to indicate the X point being updated. Note that buffer U2047A also produces the HORIZ SIG (horizontal signal) that is sent to the Deflection Amplifiers.

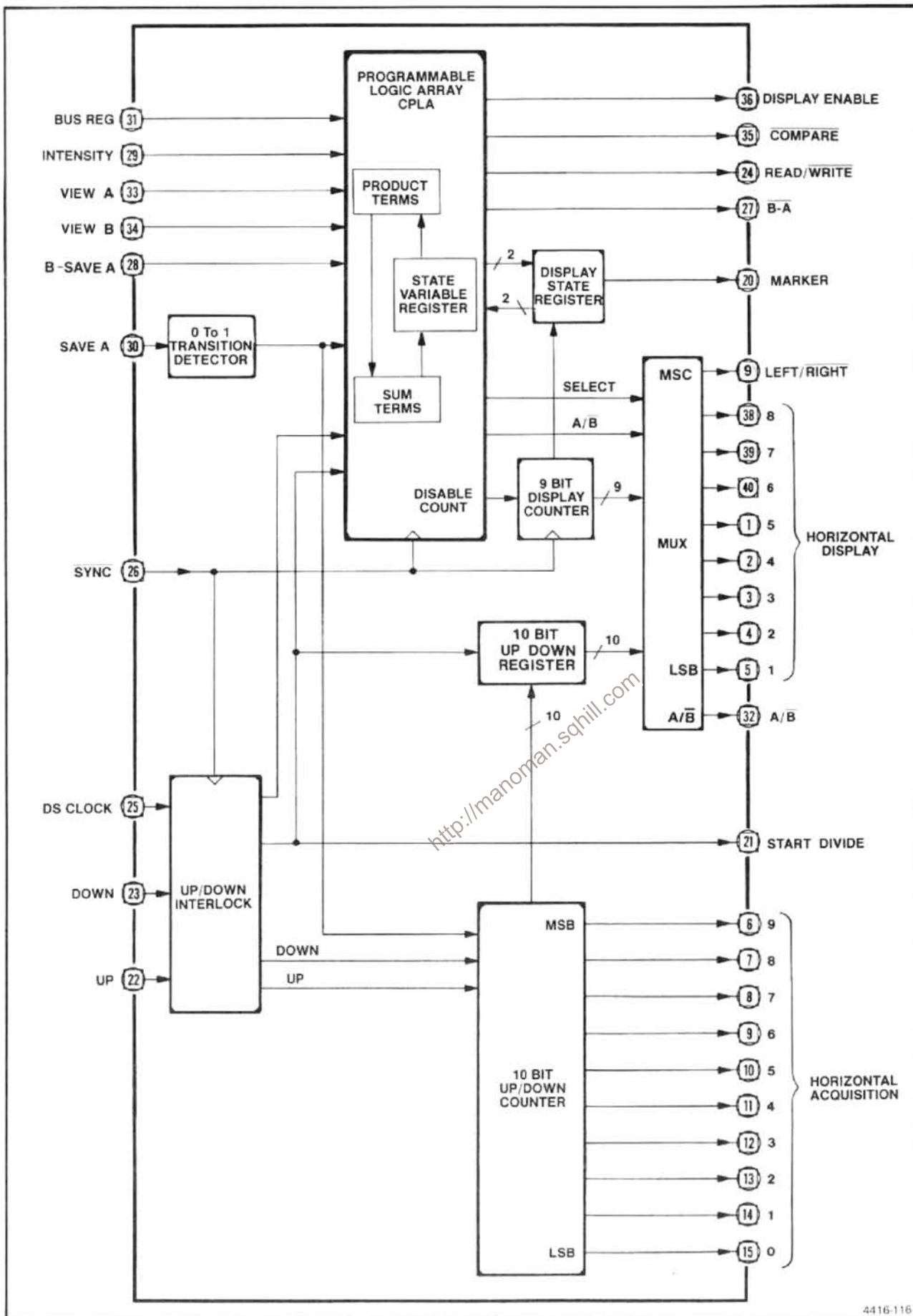


Figure 7-16. Horizontal control IC, U2035, block diagram.

Fast Retrace Blanking. Between the display of the B memory contents and display of the A memory contents, a fast retrace occurs. This retrace, unlike the one that follows the A memory display (cursor), is not required to be seen and is blanked. This is accomplished by blanking control flip-flop U1014B, which is controlled by the most significant bit of the memory address and the DSPL EN signal during a marker cycle.

Memories. Integrated circuits U1026 and U2026 provide 8 k bits of random access memory for storage of the 1024 data points used in the digital storage system. Addressing during bus transfer of memory data is controlled by address tri-state buffers U1023 and U1016 and by horizontal control IC U2035 during memory update.

DEFLECTION AMPLIFIERS



Refer to the block diagram adjacent to Diagram 27 as well as the schematic diagram. The Deflection Amplifier receives vertical signal information from the vertical section of Digital Storage or the Video Processor, and horizontal or sweep voltage from the horizontal section of Digital Storage or the Sweep board. Readout data for the display comes from the Crt Readout circuits. The output of the Deflection Amplifier drives the crt deflection plates. The amplifiers contain the switching circuits necessary to perform the selection functions and they also contain the amplifier stages needed to produce the deflection plate drive signals.

Horizontal Section

Signal lines HORIZONTAL SIGNAL, (from the digital storage circuits through edge connector pin 49) and SWEEP (from the Sweep circuit through edge connector pin 51) are applied to switch IC U7055A. U7055, under control of the STORAGE OFF signal (from the digital storage circuits through edge connector pin 7) selects either the HORIZONTAL SIGNAL or SWEEP input. The SWEEP signal is selected when the STORAGE OFF line is floating or pulled high. The HORIZONTAL SIGNAL is selected when the line is pulled low. Resistive divider R7051 and R7081 reduces the selected signal from 1 V/div to 0.5 V/div. U7073 buffers the selected signal. It goes out to the HORIZ OUT rear-panel connector via edge connector pin 48. U7073 applies the signal to switch U7055B. The HORIZ R/O signal, from the Crt Readout circuits, is also applied to U7055B. The R/O OFF signal, from the Crt Readout circuits selects between these two signals. When R/O OFF is floating or pulled high, the switch transmits the signal from buffer U7073 to the shaper. When the line is pulled low, it selects the HORIZONTAL R/O signal.

U7055B applies the signal to a shaper network to compensate for non-linearity in the crt deflection characteristics. This network consists of resistors R5059, R5058, R5057,

R5062, R4061, and R4059, plus diodes CR4052, CR4051, CR4058, and CR4056. The HORIZONTAL POSITION voltage, from the front panel via edge connector pin 47, through resistor R6032, is applied to the shaper circuit so the shape correction factor relates to the crt deflection.

The shaped signal is then applied through preamplifier U2060 to the deflection amplifier circuits. Horiz Gain adjustment R1055, calibrates the amount of gain compensation required for proper deflection sensitivity.

The horizontal deflection amplifier consists of two circuits similar to each other, one for each horizontal deflection plate. One circuit is an inverting amplifier, the other operates in-phase. Inputs to Q4038A of the inverting side are through the parallel combination of resistors R4049 and R4048 and capacitor C4057. The series connection of resistor R4048 and variable capacitor C4057 provides high-frequency response compensation. Capacitor C2047 controls high-frequency feedback.

Input to the non-inverting side is through resistor R5029 to the base of Q4025A. R4019 and R5035 set the dc level for the feedback loop to the base of Q4025B. Variable capacitor C5021 provides adjustment to set transient gain. High-frequency feedback is controlled by capacitor C3021.

Gain of each amplifier section is approximately 20. (Horizontal deflection sensitivity of the crt is approximately 21.3 V/div per side.) Each section is single-ended and incorporates a gain-degenerated dual PNP transistor at the input side (for temperature compensation) connected as a differential amplifier. For example, Q4038B of the right deflection amplifier drives emitter follower Q4047.

Signals with a low rate of change drive the output transistor through R5037 and P3033. As the rate of rise increases, the drop across R5037 increases and when it reaches 0.6 V, either Q4035 or Q4042 are biased on. These transistors provide the high current drive for the output transistors. When the signal rate of change is low, Q1043 drives the crt deflection plate and Q1049 provides bias current for the amplifier. As the rate of rise increases, C3039 couples the signal to the base of Q1049. Q1049 provides the positive drive to the deflection plate, and Q1043 provides the negative drive. Each output transistor can provide a 200 V excursion in approximately 1 μ s.

The horizontal amplifiers operate with approximately 1 mA of bias current in the output stage, as set by the current through resistor R3031, R1052, and R1049 at the base and emitter of Q1049. Current through resistor R3031 also provides the current for the input stage, Q4038A/Q4038B. Emitter follower Q4047, operates at approximately 2.5 mA.

Resistors R1045 and R1034, in the emitter circuit of Q1049 and Q1043, degenerate the output stage for fast steps. Current from the -15 V source through resistor R4033, sets the output operating level. Feedback resistor R3045 sets this output level at approximately 142 V.

Operation of the right-hand (inverting) section is basically the same as the left-hand (non-inverting) section.

Vertical Section

VIDEO FILTER OUT, from the Video Processor, and VERTICAL SIGNAL, from the Digital Storage, are routed through switch IC U6055A, under control of the STORAGE OFF signal from the Digital Storage board. Note that the VIDEO FILTER OUT signal is buffered by IC U7065 to prevent a change in load transients from affecting the signal level. A high on the STORAGE OFF line selects the buffered VIDEO FILTER OUT signal, and a low selects the VERTICAL SIGNAL. U6065 inverts the selected signal and clamps it to ground. Both the VIDEO FILTER OUT and the VERTICAL SIGNAL are specified at 0.5 V/div with 0 V for the baseline and positive voltages above the baseline.

The signal is re-inverted and offset by buffer U6073 so center screen represents 0 V. Buffer U6073 supplies a sample of this centered signal to the rear-panel VERT OUT connector via edge connector pin 46. The output of U6073 is also applied through switch U6055B, when the R/O OFF line is high, to the vertical shaper circuit. When R/O OFF line is low, the VERTICAL R/O signal is applied to the shaper.

The vertical section shaper (R4062, R4065, R4067, R4069, R4064, and CR4063, CR4064, plus the preamplifier U2062) operates the same as the horizontal section. Q4078 limits positive excursions to approximately one division above the top of the screen to protect the output stages from being overdriven.

The vertical output stages are similar to the horizontal stages, with the exception of higher bias current. Current flow of approximately 1 mA, through resistors R3089 and R3098, produces approximately 5 mA in the output stages. To correct for the increased current in the dual input stage transistors, Q4083 and Q4101, resistors R5081 and R5099 are lower value than their counterparts R5041 and R5027 in the horizontal amplifier.

U6024 compares the signal level from the baseline clamp, U6065, with a reference level set by divider R7032/R7034. This produces the CLIP signal for the Z-Axis interface circuits. When the VIDEO FILTER OUT signal is more negative than the reference level (approximately 1 division above baseline), it pulls the CLIP line low. R7021 pulls

the CLIP line high if the signal is more positive than the reference level.

Z-AXIS AND RF INTERFACE BOARD

Refer to the block diagram adjacent to Diagram 28 as well as the schematic. The Z-Axis and RF Interface board contains the RF interface circuits, crt Z-axis drive circuits, power monitor circuits, and a timer that measures operational hours. This board provides beam intensity (nominally from the front panel), baseline clipping, and unblanking logic for the signals or readout data. Unblanking logic comes from the Sweep board, the Crt Readout, the Deflection Amplifiers, and the Digital Storage. The RF Interface circuits receive data from the microcomputer that controls the RF Attenuation, transfer switch, and IF selection. A power fail circuit on the board detects any change in input power frequency or power supply voltage and notifies the microcomputer. An elapsed time meter is also located on the board to give a indication of total instrument operating time.

RF Interface Circuits

The RF interface includes the digital control circuits that receive the address and instruction data from the microcomputer and decode it to control the RF Attenuator, Transfer Switch, and IF selection. The power supplies that are required to drive the attenuator and switches are also included.

Digital Control. Address decoder U2045 latches the data at the input of U3046 whenever the microcomputer selects address 4F. Table 7-7 lists the purpose of each data line from the buffer.

Table 7-7
RF INTERFACE LINES

Line	Purpose
Q1	Enables 10 dB attenuator
Q2	No connection
Q3	Enables 30 dB attenuator
Q4	Enables current drivers Q2025 and Q3028
Q5	Enables transfer switch driver
Q6	Selects 829 MHz IF (high state) or 2072 MHz IF (low state)
Q7	Enables 20 dB attenuator
Q8	Enables baseline clipping

When Q4 of U3046 goes low, Q2025 and Q3028 conduct. This raises the Vcc of attenuator drivers U3034, U3029, and U3038 to +16 V for approximately 100 ms to energize the attenuator solenoids. A diode protects each attenuator driver output line from the inductive voltage surge that occurs when the solenoids change state.

Transfer Switch. Operation of the Transfer Switch is dependent on the output of Q3025/Q3024. The Q5 output of U3046 is applied to the input of operational amplifier U4023, which drives differential amplifier Q2025/Q3024. When Q5 goes high, Q3025 is biased on and the Transfer Switch selects the external mixer. When Q5 goes low, Q3024 is biased on, and the internal mixer is selected. Diodes CR3018 and CR3017 protect the transistors from voltage spikes induced when the Transfer Switch changes state.

Z-Axis Circuits

The Z-Axis circuits provide the drive currents and bias voltage to operate the crt. They consist of the intensity control logic circuits, which control the crt beam current for normal signal display operations, and the unblanking gates, which furnish current to the Z-Axis drive amplifier to drive the crt control grid.

Z-Axis Drive Amplifier. The Z-Axis Drive Amplifier is an operational amplifier that consists of transistors Q3047, Q4058, and Q4059, and related components. R1050 is the input resistance for the amplifier, and R2066 is the feedback resistor. The output is clamped by diodes CR3059 and CR3066 to protect the amplifier from transient surges in case of crt arcing. The amplifier is driven by two sources, exclusive of each other; U2038B/Q2042 drives the amplifier during readout display periods, and U2038A/Q2044 drives the amplifier during sweep display periods. U2039 is an AND-NOR gate that provides the logic to one input of NAND gate U2038A to turn Q2044 on or off. The R/O OFF line and the output of U2039 must both be high for U2038A to furnish current to Q2044. Table 7-8 lists the conditions under which U2039 will output a high to U2038A.

Table 7-8
U2039 TRUTH TABLE

	Condition
U3046 output (line Q8)	0 0 0 1 1 1 0 0 0
CLIP	0 0 0 0 0 0 1 1 1
Z-Axis Blank	1 1 1 1 1 1 1 1 1
Storage Off	0 0 1 0 0 1 0 0 1
SWP GATE	1 0 1 1 0 1 1 0 1
U2034, pin 10	0 0 0 0 0 0 0 0 0

Only the combinations shown in Table 7-8 plus a high on the R/O OFF line will gate a low out of U2038A. When the U2038A output is low, emitter current is furnished to Q2044, which in turn furnishes current through R2051 (the input resistance of the Z-Axis drive amplifier) to Q3047. U2034B is a single-shot multivibrator that produces a 3 μs pulse to blank the crt beam during trace return, between readout and signal display.

The other source of input current to the Z-Axis drive amplifier is Q2042. This transistor is turned on by U2038B when R/O UNBLANK is high and R/O OFF is low.

Q1028 is the current source for divider R1030/R1025 that establishes the operating point for Q2042 and Q2044, which sets the intensity level. Diodes CR1045 and CR1043, connected from the base of Q2042 and Q2044 to the emitter of Q2022, limit the display intensity. These diodes prevent the bases from going more positive than approximately 0.6 V above the emitter voltage of Q2022. This circuit, which includes Int Limit adjustment R1027, sets the maximum current for both Q2042 and Q2055.

Transistors Q1017 and Q1015 provide current for the trace rotation coil. Trace Rotation adjustment R1021 sets the current so the displayed trace is aligned with the graticule.

Power-Fail Detector

This circuit detects an instrument power failure and transmits the information to the Processor and Memory boards. The LINE TRIGGER signal from the Power Supply board through edge connector pin 60 is supplied to Q2011. Q2011 buffers the signal and applies it to the input of retriggerable one-shot U2034A. U2034A performs as a missing-pulse detector to generate a power-fail signal through Q3011 to notify the Processor and Memory boards if more than two 60 Hz cycles are dropped. To avoid an undefined state, the output from U2034A is latched low by U2051. Under normal operating conditions, the POWER-FAIL signal from Q3011 is high.

Power-Supply Monitor

This circuit detects if one or more of the instrument power supplies have failed. Each voltage supply in the instrument is fed into thick film resistor network R3051, which balances the currents to provide a null output (approximately 1 Vdc). Any line change of more than ±25% drives the input to window comparator U3051 beyond its ±200 mV threshold and generates a low output. Q2059 and Q2067 drive the dual light emitting diode DS1062 to provide visual indication of power-supply status (green indi-

icates normal operation and red indicates a fault condition). The output of U3051 is also fed to tri-state buffer U3052. After instrument power up or if a failure is detected, the microprocessor will poll address CF to determine power-supply status over the data bus.

Timer

An electromechanical timer, M1019, is calibrated for a duration of 5000 operating hours. The current through R1015 and the timer causes the copper band to progress along the scale.

HIGH-VOLTAGE SUPPLY

Refer to the block diagram adjacent to Diagram 29 as well as the schematic diagram. The High-Voltage Supply furnishes the -3860 V crt bias and 6.3 Vac filament voltage to the crt cathode, and provides dc restoration for the Z-AXIS DRIVE signal. The supply consists of the following four main circuits:

1. The high-voltage oscillator circuit produces the crt filament voltage and the 200 Vac that is stepped up and applied to the voltage doubler circuit.

2. The voltage doubler circuit rectifies and filters the high voltage for application to the crt cathode.

3. The high-voltage regulator circuit samples the high voltage and regulates the operation of the high-voltage oscillator.

4. The Z-Axis clipper and rectifier circuits couple the Z-AXIS DRIVE signal to the crt control grid.

High-Voltage Oscillator. This circuit consists of transistor Q1073, transformer T2065, and associated components. The approximately 200 Vac, oscillator output is coupled across T2065, where it is stepped up for application to the voltage doubler, and stepped down for application to the crt filament.

Voltage Doubler. The voltage doubler consists of CR4041, CR4035, C4027, C5021, C4024, R3038, and R1039. The output of the doubler is taken off the anode of CR4035 and applied to the crt cathode through the filter consisting of R3038, R1039, and C4024. Reference voltage for the regulator is also taken off the end of R1039. R1039 keeps the filament at the same potential as the cathode.

High-Voltage Regulator. This circuit consists of amplifier U4083 and surrounding components. The high voltage is applied through a voltage divider that consists of R1017B and R1017C. This voltage divider is connected through R1042 to $+15$ V. The sample of the high voltage at pin U is applied through R4075 to the input of comparator U4083. The correction signal, in the form of dc drive, is applied as bias to Q1073 to set the oscillator current.

CR4078 and CR4077 at the input to U4083, protect the input against excessive voltage excursions. The high-voltage oscillator is protected by CR4071, R3079, and R4074 in case the $+100$ V supply should fail. Normally, CR4071 is back biased. If the $+100$ V is not present, CR4071 conducts and clamps the input negative; the output of U4083 swings negative and Q1073 remains cut off. This circuit ensures that Q1073 will begin to oscillate only after the 100 V supply reaches a voltage sufficient to sustain oscillation. CR3077 (in the regulator output circuit) protects the base of Q1073 from excessive negative voltage.

Z-Axis Clipper. This circuit consists of diodes CR1056 and CR1046, plus associated components. The 225 Vac from pin 8 of T2065 is coupled through C1058 and R1048 to the junction of CR1046 and CR1056. The regulator circuit, that consists of VR1041, R2050, R2040, and Q2048 holds the cathode of CR1046 at approximately $+100$ V to 143 V, depending on the setting of R2040. CR1046 and CR1056 clip the incoming 225 Vac to a total excursion of $(V_{\text{CR1046 cathode}} - V_{\text{Z AXIS DRIVE}} + 1.2 \text{ V})$. R2040 is adjusted for complete cut-off of crt with Z-Axis DRIVE at minimum. The voltage that passes the clipper circuit is coupled through C1031 to the Z-Axis rectifier.

The clipped Z-AXIS DRIVE signal is rectified by CR2044 and CR2046, which are the principle components of the second section of the Z-Axis circuit. The rectified voltage is then fed to the grid of the crt. C1041 couples the fast changes of drive voltage to the crt grid to speed up the response of the grid circuit. The crt grid is protected from high-voltage arcs by neons DS2052, DS2054, and DS2057. R1043 protects CR2046 and CR2044, respectively, from high-voltage surges if the crt should arc.

CRT READOUT

The Crt Readout assembly stores readout characters and generates deflection and Z-Axis signals to display those characters. It also handles the frequency dot marker display. Both characters and frequency dot displays are time-shared with the spectrum trace.

Generating Readout

Crt readout is handled by sequential logic, clocked at 3.41 MHz, supplied by the Processor board. The readout circuitry (Figure 7-17) is composed of the following elements.

1. Readout On Timing—RAM for character storage.
2. Character Counter—to access the RAM and control the scan.
3. Character Generator—to unblank the crt beam.

4. D/A Converters—to deflect the crt beam.
5. Instrument Bus Interface—to store characters and control the display. A more detailed block drawing is provided adjacent to Diagram 30.

Forty (40) characters can be displayed per line, with up to 16 lines selected, under software control. Normally, up to three lines are displayed while simultaneously displaying the spectrum. When over three lines are to be displayed, the spectrum display is disabled in order to keep the readout refresh rate above 60 Hz.

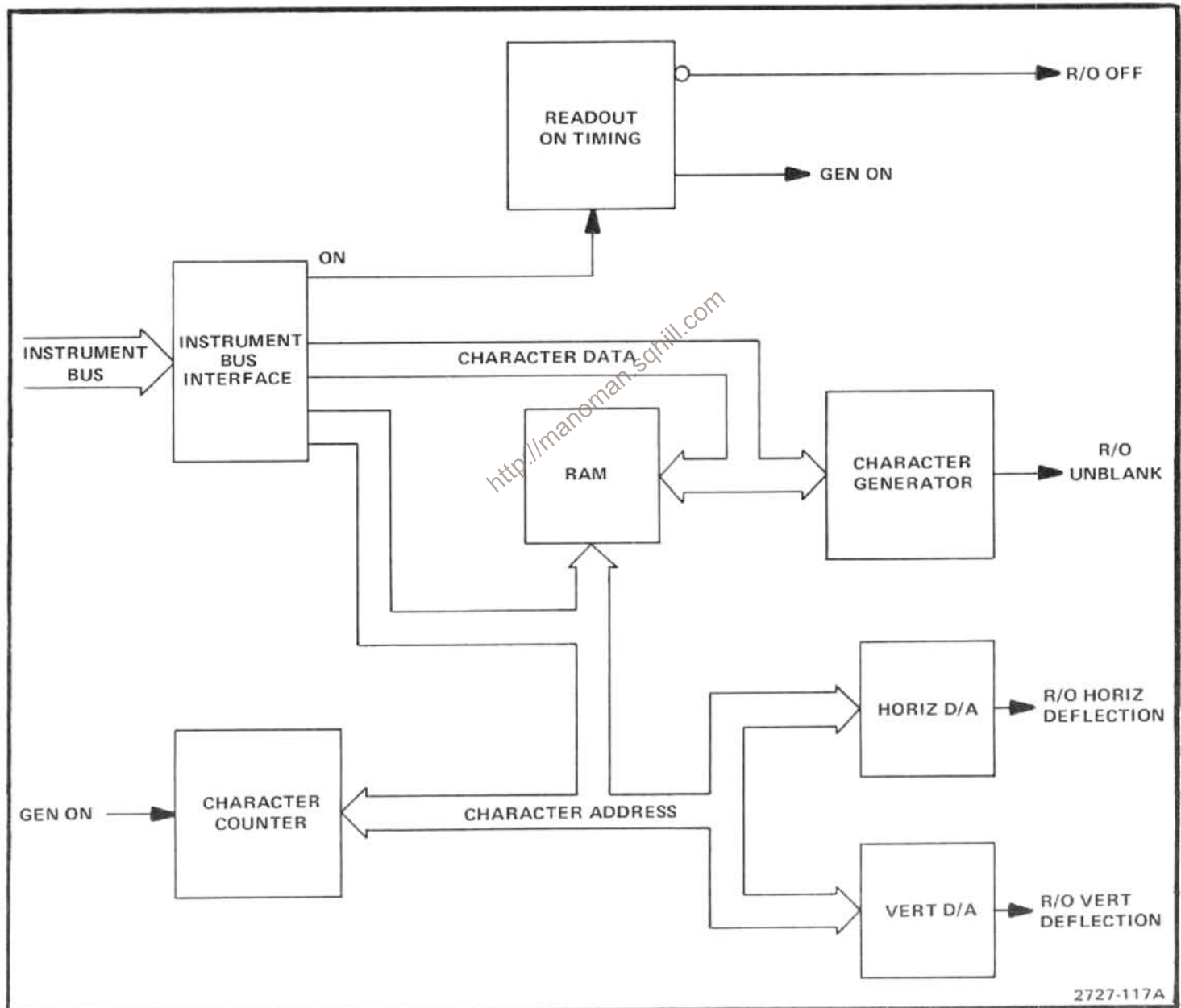


Figure 7-17. Block diagram of crt readout.

Readout-On/Off Timing. Characters are written one at a time. This allows a portion of the spectrum to be drawn between each character. The character duty cycle is between 10% and 25% because it varies with the character drawn. The time sharing between character writing and spectrum display is pseudo-random to reduce the effect of gaps in the spectrum display by moving them on the trace.

The readout-off time is set to $140\ \mu\text{s}$ by one-shot multivibrator U1055 (Figure 7-18). Flip-flop U1041B asserts GEN RUNNING after U1055 times out, allowing a character to be drawn. After a character is written, ROW 0 COL 0 resets the flip-flop, which clocks off time one-shot U1055. The ON control bit must have been asserted by the microcomputer to get readout (as described under Instrument Bus Interface later in this section).

If BLANK (MSB of the character data) is not set, the GEN RUNNING flip-flop unasserts R/O OFF through OR gate U2044B; this switches the readout deflection signals for the deflection amplifier inputs (Diagram 27). BLANK can be set by the microcomputer to load a space into the character RAM so the readout does not use time for the spectrum trace to scan a blank character.

Character Scan. Although the 8678 character generator IC, U2048, is often used in raster scans, in this application it is used to write complete characters, as shown in Figure 7-19. A character is drawn as a pattern of dots in an 8×8 matrix where the top row and first three columns are blank. These blank dots allow for beam retrace and spacing. The idle position between characters is indicated on the figure.

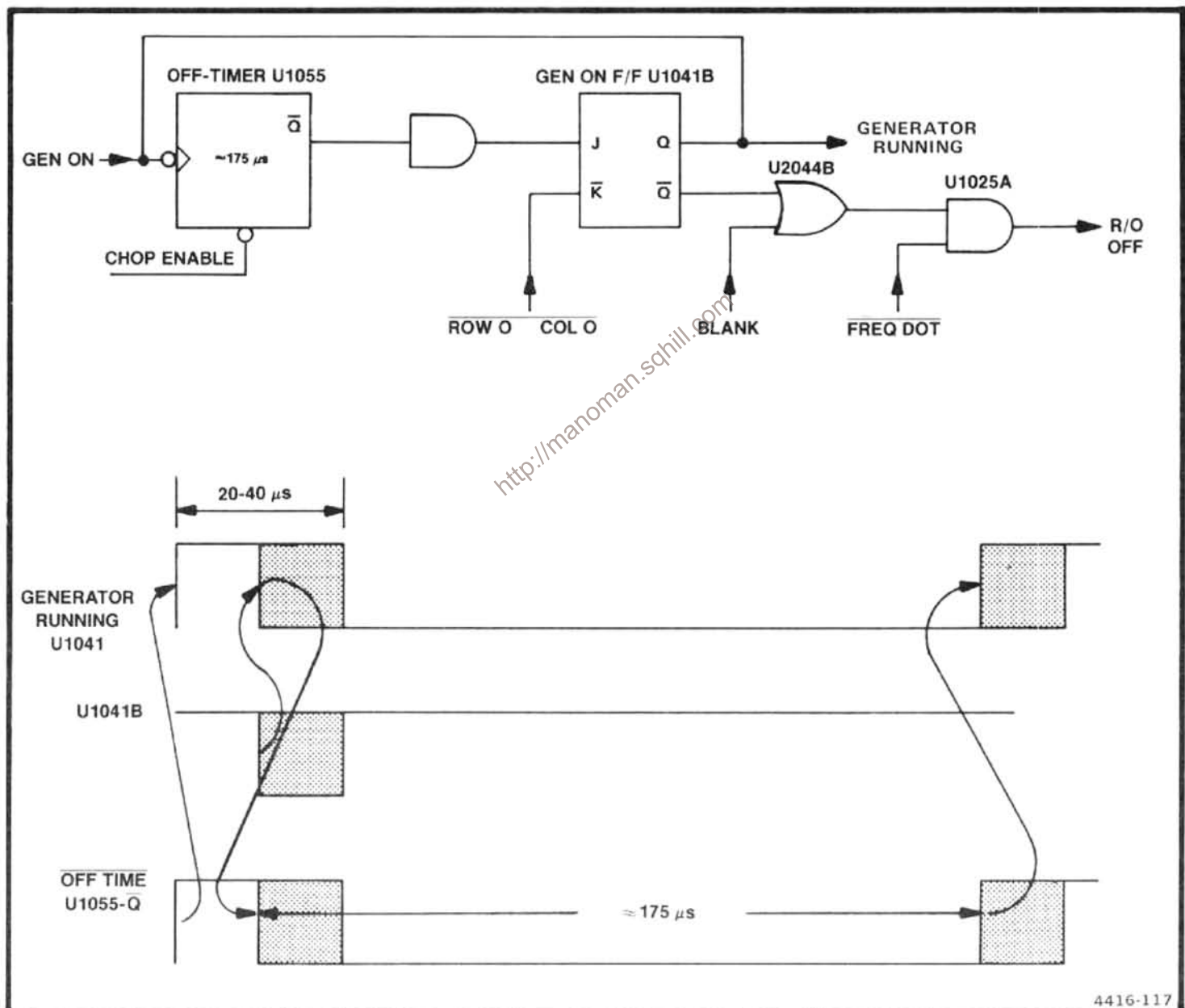


Figure 7-18. Character on/off timing.

		COLUMN 0-7								
		0	1	2	3	4	5	6	7	
IDLE POSITION	ROW 0-7	0	X	X	X	X	X	X	X	X
	1	X	X	X	O	O	O	O	O	
	2	X	X	X	O	O	O	O	O	
	3	X	X	X	O	O	O	O	O	
	4	X	X	X	O	O	O	O	O	
	5	X	X	X	O	O	O	O	O	
	6	X	X	X	O	O	O	O	O	
	7	X	X	X	O	O	O	O	O	

X = BLANK
O = DOT ON OR OFF

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Figure 7-19. Character scan.

Character counters synchronize the horizontal and vertical scan with the Z-Axis signal from the character generator IC to draw the character. These counters, U2022, U2018, U2026, and U2014, are wired to divide by 8 for the columns within a character (columns A, B, C), divide by 8 for the rows within a character (rows A, B, C), divide by 40 for the characters within a line (characters A, B, C, D, E, F), and divide by 16 for the lines within a display. The counters are enabled only when the generator has control of the crt beam (GEN RUNNING line asserted) and INCR (increment) is high when INCR is low, the crt beam is stopped to write a dot on the crt).

The SKIP line from U2052 permits software control of the allowable states of line counter U2014. By placing a one in this bit of a character, the line counter is allowed to count up to the next state. This will continue until a character is encountered with the "skip" bit set to zero. This allows the addition of a third line to the normal two-line readout for status messages, by operating with the circuit normally in the 16-line mode (all but the bottom and top lines start with a readout character of 40 hex, which has the SKIP line set high). Thus, all but the bottom and top lines are skipped. When large messages are to be displayed, the SKIP line is set low for all characters and 16 lines are displayed.

The counters are wired to force the D/A converters to step through the character horizontally, a row at a time. At the same time, the pattern of dots is accessed under the control of the timing decoder logic, U2039B and U2031. The AND gate and decoder combine to control the character generator, U2048, which generates the correct pattern of

blanking to draw the pattern of dots for the character. U2048, the 8678 character generator IC (Figure 7-20) contains a ROM with the correct pattern of 64 bits for each of the 64 characters in its repertoire. The bit patterns are accessed by a decoder that operates on the ASCII code on the character generator inputs. The pattern of bits is multiplexed, one 8-bit line at a time, into a shift register that is clocked out one bit at a time to control the crt Z-axis.

Character Generator Timing. The character generator timing lines are called DOT, LINE CLK, \overline{LE} , and \overline{CLR} . Each cycle of DOT clocks one dot (bit) out of the shift register. A positive transition on LINE CLK switches the next line (row) of dots onto the shift register inputs; the dots are latched by a negative transition on \overline{LE} (load enable), setting up the shift register to display another row of dots. \overline{CLR} resets the line counter to begin drawing another character.

GEN RUNNING, INCR, and CRT CLK are combined through AND gate U1037B to generate DOT to clock the character generator, U2048. Inversion by the gate restores the phase relationship of the DOT input and the inverted LINE CLK. \overline{LE} is gated by U2039B when the character counter reaches column 2. This loads the shift register with the next row of dots, which is displayed starting at column 3. LINE CLK advances the line (row) counter after the scan of the current row begins to set up the next row of dots on the shift register inputs; this occurs at column count 4. Decoder U2031 outputs a $\overline{ROW\ 1\ COL\ 1}$ when the character counter reaches row 1, column 1 (the first non-blank row of dots scanned in each character). This is asserted once during the scan of each character.

The sequence of events to scan a character is illustrated in the character timing diagram (Figure 7-21). At 1, the character generator finishes a character. Then, when the counter advances, decoder U2031 asserts $\overline{ROW\ 0\ COL\ 0}$, resetting the GEN RUNNING flip-flop, U1041B, on the next clock. This stops the counter at row 0, column 1 (2 on the figure). When readout-off time one-shot U1055 completes the time-out period, it allows the GEN RUNNING flip-flop to be set. Just before the scan enters the actual character clock area (at 6), \overline{CLR} resets the character generator line counter (at 5). \overline{LE} (at 5a) loads one row of dots into the output shift register so that the first dot is output at 6. The break (7 on the figure) indicates that the scan continues. After the character is scanned, the scan returns to the idle state; 8 and 9 correspond to 1 and 2 on the timing figure.

Dot Delay. Each bit shifted out of the character generator is the value of a dot in the 5 x 7 character matrix; 0 for a blank and 1 for a dot that is to be written. As the scan progresses at 3.4133 MHz, a rather faint character display might be expected. To brighten the dots that are written, a shift register is used as a delay element so that dots are displayed and counters disabled for 3 clock cycles.

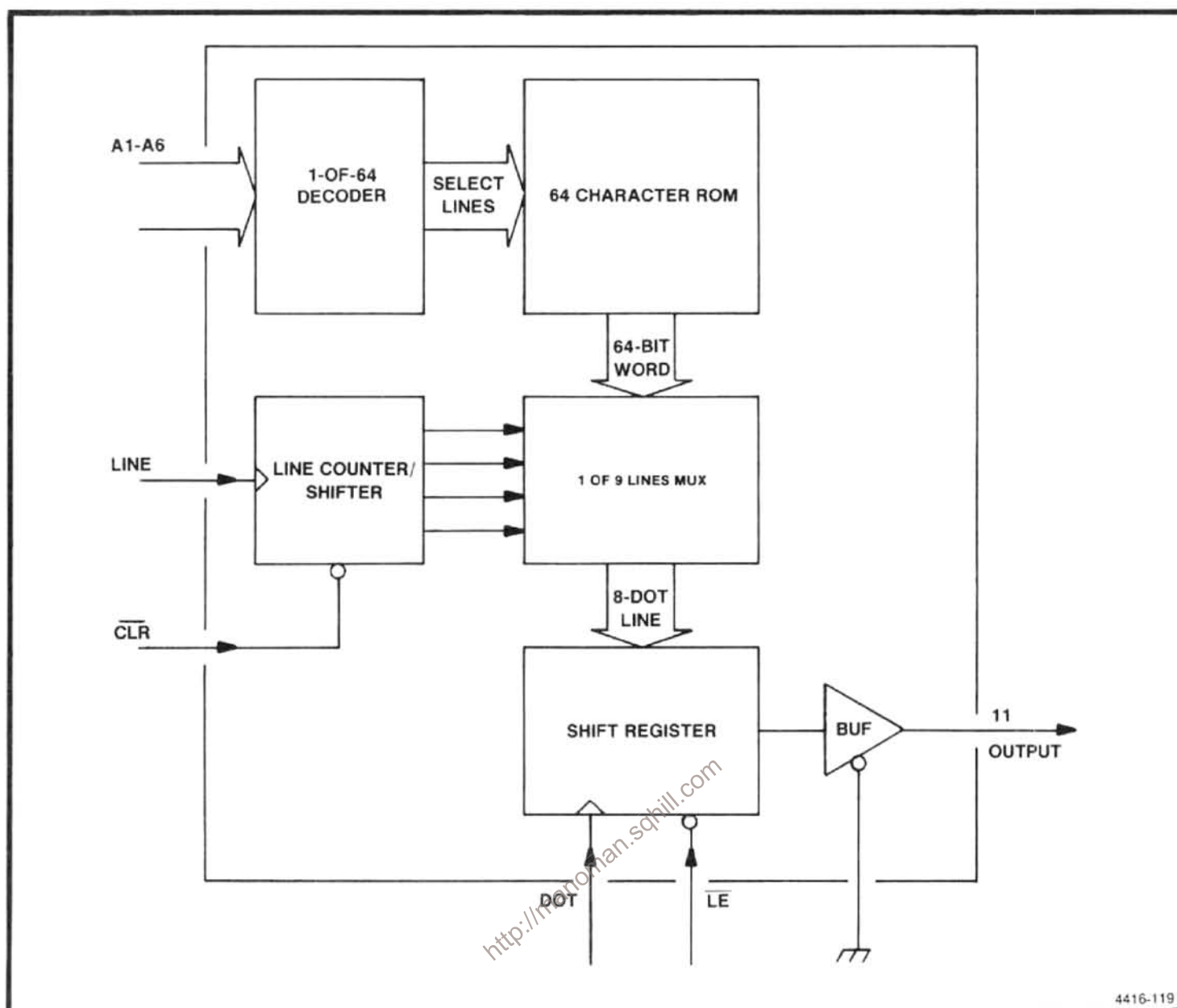


Figure 7-20. Character generator (U2048) block diagram.

Assume that no dots have been displayed for several dot clock cycles, so the output of the character generator, pin 11 of U2048, is low. Thus, U1020B output is high, and the outputs of the delay shift register U1025C and U1020B are low. When a dot is displayed, the character generator output (pin 11 of U2048) goes high. This causes INCR to go low and disable the counters. It also causes the input to the delay shift register, pin 11 of U1020B, to go high. On the next clock pulse, U1020A output follows INCR and goes low. The shift register clocks the one in, and the unblank flip-flop, U1016B, goes high, turning the crt beam on. This is the only "1" it will clock in, because the output of U1020A is now low. The circuit is now in a lock-up state with the counters disabled. Two more clock cycles will go by until the "1" in the shift register is clocked out, allowing the output of

U1033C to go high. A high on the output of U1033C starts the counters again and resets unblank flip-flop U1041A.

Instrument Bus Interface

The microcomputer controls the crt readout and frequency marker dot over the instrument bus through the following ports.

Port	Hex Address
Control/Address	5F
Address/Data	2F

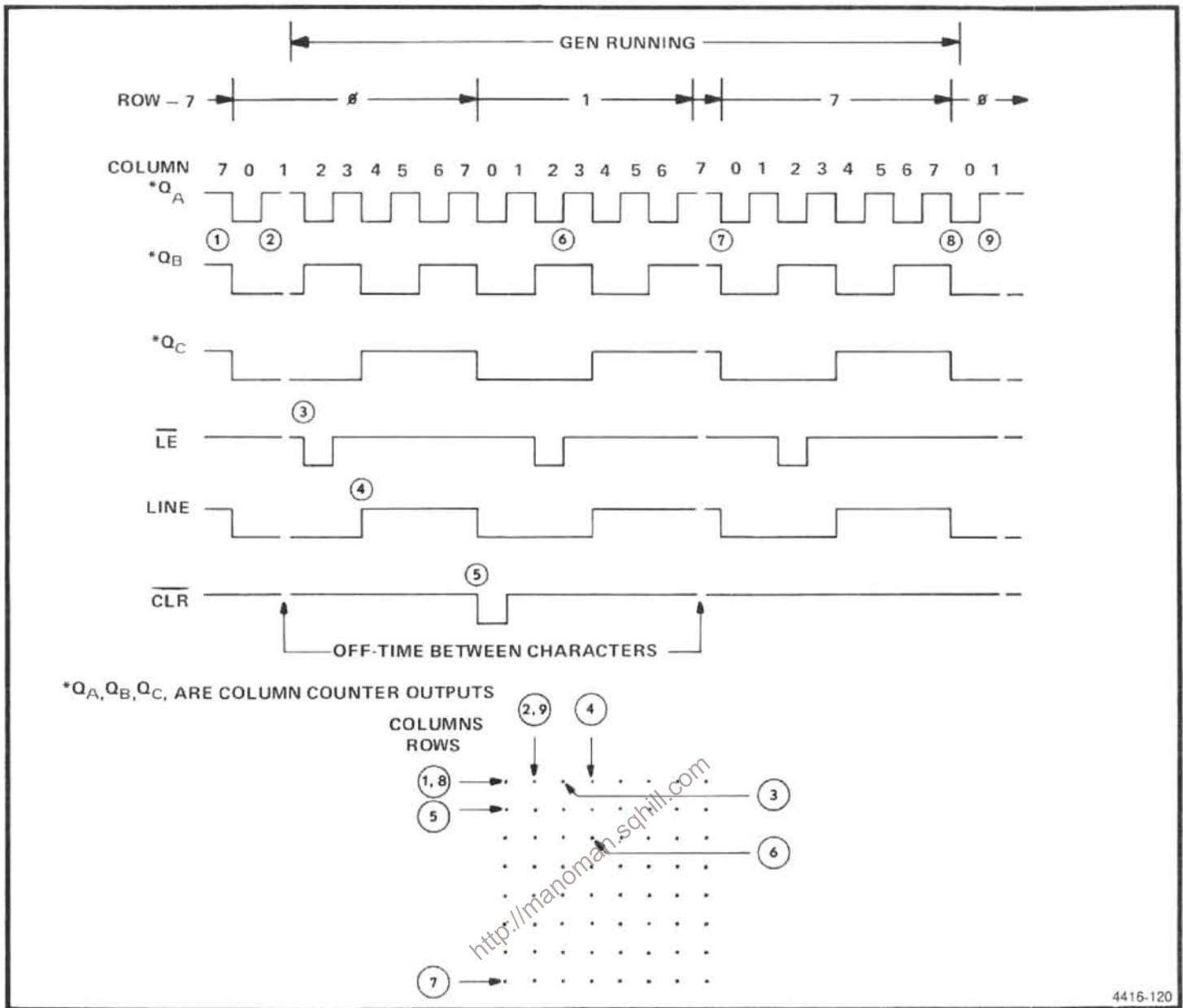


Figure 7-21. Character timing diagram.

Decoder U3051 asserts 5F when it sees a value of 5 on the upper four bits of the instrument bus address lines, and 2F when it sees a value of 2. The decoder must be enabled by DATA VALID high on the instrument bus. The false transition of DATA VALID causes the addressed port to latch the data on the instrument bus.

Control Port. The control address port, U3034, turns the readout on or off, steers data sent to the address/data port, controls the mode of the frequency marker dot, and contains two bits of the RAM address. The bits are defined in Table 7-9. Bit numbering on the instrument bus starts at zero. However, the D and Q pins of U3034 (and some other ICs) are numbered in accordance with their data sheets, starting at one.

Bit 0 turns the crt readout display on (1) or off (0). When set, this bit releases CLEAR from the GEN RUNNING flip-flop and allows the off timer, U1055, to set U1041B. Also, when the ON/OFF line goes high, it enables the INCR gate, U1037C, to steer the position counter onto the character RAM address inputs through line driver U3042 and multiplexers U1050 and U1046. When cleared, this bit places an address, latched in U3038 and U3034, on the

Bit 1 interprets data sent to the address/data port as an address (1) or data (0) for the character RAM. Setting this bit disables the character RAM for input and sets up the clock signal to latch the address.

When this bit is set, Q8 of U3034 gates a high on the output of U2044A. This high prevents input to the character RAMs, U2057 and U2052, by setting its R/W input high. This high also disconnects the instrument bus from the character RAM data inputs by disabling U3047; meanwhile, U2037A is enabled to gate the clock signal that latches the address. The positive clock transition is applied to U3038 when DATA VALID goes false at the end of a write cycle to the address/data port, releasing 2F.

When this bit is cleared and $\overline{2F}$ is asserted, U2044A enables the character RAM for input and passes the data through U3047.

Table 7-9
CONTROL PORT

Bit	Function
0	Readout on/off
1	Address/data
2	A9 of RAM address
3	Max Span dot
4	A8 of RAM address
5	$\overline{16}$ line mode
6	$\overline{40}$ characters/line
7	Spectrum display available

Bit 2 is the MSB of the RAM address.

Bit 3 controls the frequency dot marker. This bit is set in the MAX SPAN mode to position the frequency dot with BFRD TUNE VOLTS from the first local oscillator. When cleared, this bit centers the frequency dot on the spectrum display.

Bit 4 is the A8 address line for the character RAMs.

Bit 5 is the select for 16 lines mode.

Bit 6 selects the 40 character/line mode.

Bit 7 enables the clipped display with the spectrum. When high, U1055 is enabled and causes 140 μ s periods to occur between characters when the spectrum is disabled. When low, U1055 is disabled, R/O OFF is forced low to disable the spectrum display, and W1028E forces the current boost addition to be disabled. Also, U1016 is disabled at the marker dot is not displayed.

Address/Data Port. The microcomputer loads characters for crt display through the address/data port. Each character requires the following four write cycles.

1. Bit 2 in the control port is set for an address transfer, and the upper 2 bits of the RAM address (A8, A9) are sent.
2. The lower 8 bits of the address in the character RAM are sent to the address/data port.
3. Bit 2 in the control port is cleared.
4. The data is sent to the address/data port. The bits are defined in Table 7-10. Bits 0-5 are the lower six bits of the character RAM address or are the ASCII code for the character.

Table 7-10
ADDRESS/DATA PORT

Bit	Function
0-5	Address of ASCII code
6	Skip bit
7	Blank character

Bit 6 causes the line counter, U2014, to skip a line, if set.

Bit 7 is used to reduce overhead readout display. It is set when a space is transferred to the character RAM, so the readout does not steal time from the spectrum trace to scan a blank. When set, this bit prevents the GEN RUNNING flip-flop from gating R/O OFF low through U2044B.

Frequency Dot Marker

The frequency dot marker is refreshed immediately after the last character position in the lower readout is scanned. Normally, the marker is centered on the screen just below the upper readout as a pointer for the center frequency readout. When MAX SPAN is selected, however, the dot marker moves to a point on the display that corresponds to the center frequency value.

The negative transition of line D triggers the marker generator. A simplified diagram of the circuit and its timing is shown in Figure 7-22.

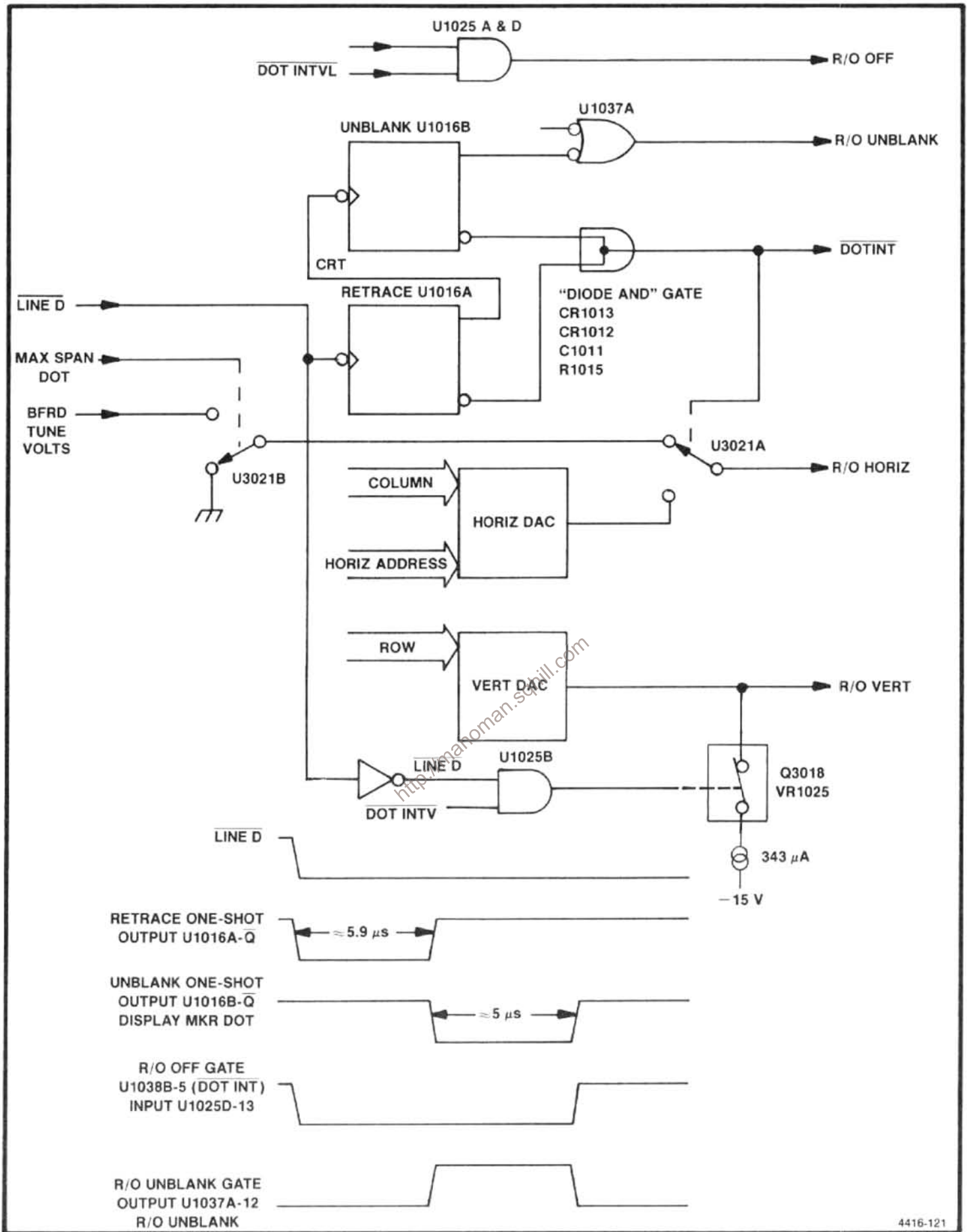


Figure 7-22. Frequency dot marker simplified diagram with timing waveforms.

U1016A delays the marker dot to allow retrace while gating $\overline{\text{DOT INV}}$ low to set up the display. $\overline{\text{DOT INV}}$ affects the readout deflection outputs in the following ways.

1. The horizontal output is connected either to ground, for a center-screen dot, or BFRD TUNE VOLTS, for a max span pointer. BFRD TUNE VOLTS is proportional to the center-frequency readout offset from the center of the frequency range.

2. The U1025B output goes low during the dot interval to cause Q3018 to insert an offset current into the vertical output, to shift the dot position down on the screen.

3. R/O OFF is gated low to switch the deflection amplifier inputs from the Trace Mode to the Readout Mode, using the marker dot horizontal and vertical signals.

When the retrace one-shot times out (approximately $5.9 \mu\text{s}$), it's Q line triggers the unblanking one-shot U1016B, which sets R/O UNBLANK high for approximately $5 \mu\text{s}$, via $\overline{\text{DISPLAY MKR DOT}}$ through U1037A. This refreshes the dot. $\overline{\text{DISPLAY MKR DOT}}$ also holds $\overline{\text{DOT INTVL}}$ low through CR1013, until the dot marker is drawn. R1015 and C1011 slow the rise of $\overline{\text{DOT INTVL}}$ to prevent a spurious signal through the "diode AND" gate.

FREQUENCY CONTROL SECTION



The Frequency Control section performs the tuning and scan function for the Preselector, 1st LO, and 2nd LO. It also provides the sweep voltage for the deflection amplifiers in the Display section so the crt display is coincident with the frequency scan and tuning. This section contains the following major circuits.

Sweep. Circuits on the Sweep board accept trigger inputs from line, internal and external sources, and the normal free-run mode of operation. They also receive external horizontal and manual sweep inputs. The circuits produce a PEN LIFT signal for chart recorder applications, a SWEEP GATE signal for crt display blanking, a SWEEP signal to drive the crt beam across the horizontal axis and drive the horizontal portion of the digital storage circuit, plus a ramp (OSC SWEEP) that is fed through the Span Attenuator to the Preselector Driver, the 1st LO Driver, and the 2nd LO.

Span Attenuator. This circuit attenuates the ramp signal as required, to sweep the frequency of the 1st and 2nd local oscillators, and tune the Preselector so it tracks the center frequency.

Center Frequency Control. The Center Frequency Control circuit provides a tuning voltage for the 1st and 2nd Local Oscillator circuits that results in a linear center frequency change as the front panel FREQUENCY control is changed. The circuit is directly controlled by the micro-computer, so remote control of the frequency is possible, by way of the GPIB rear-panel connector. The COARSE TUNE VOLTS signal from this circuit is applied to the 1st LO Driver circuits for summing with the SPAN signal to drive the 1st LO. The FINE TUNE VOLTS signal is applied to the

Preselector Driver for summing with the IF Offset voltages, and to the 2182 MHz Phase Locked 2nd LO circuit for summing with the 2nd LO SWEEP signal.

1st LO Driver. The 1st LO Driver performs the following: 1) combines the COARSE TUNE VOLTS signal with the SPAN signal and outputs a current to drive the 1st LO; 2) produces the tuning and sweeping signal for application to the Preselector Driver circuits; 3) produces the mixer bias voltages; 4) produces the BUFFERED TUNE VOLTS signal that is applied to the Display section; 5) produces a reference voltage that is used in both the 1st LO Driver circuit and the Preselector driver; 6) produces a supply voltage for the 1st LO.

Preselector Driver. The Preselector Driver combines the FINE TUNE VOLTS signal, from the Center Frequency Control board with the PRESELECTOR DRIVE signal and the SPAN VOLTS signal from the 1st LO Driver. This combined signal is offset, to compensate for the selected 1st IF, then shaped so the Preselector tracks with the 1st or 2nd LO as it is tuned by the output current. The Preselector Driver also drives the Filter Select switch that selects either the Preselector or the Low-pass Filter, depending on the frequency band selected.

SWEEP



An overall block diagram of these circuits appears adjacent to Diagram 31. The circuits on this board provide the ramp voltage that drives the horizontal deflection amplifier, the 1st LO Driver and the Preselector Driver, and the 2nd

LO. The sweep board also provides signals for the Z-Axis circuitry, an external plotter pen, digital storage, and it is the interface between the microcomputer and the Reference Lock module located on the RF deck.

Three instrument bus addresses are associated with the sweep board. Address 0F and 1F are write addresses and 9F is a read address.

U3032 is the instrument bus address decoder and outputs a low on the appropriate pin if address 0F, 1F, or 9F is selected. U2032 is an eight bit register (D flip flops) which retains data written on the data bus at address 0F. U1032 is another eight bit register that retains data written at address 1F. Only seven sections of U1032 and U2032 are used (DB0-DB7), DB0 is routed through UI3038C. These registers are responsible for storing the microcomputer's latest command and controlling most of the operation of the sweep board.

Commands that can be written at address 0F are: 1) sweep start for single sweep mode (bit 0 high); 2) internal frequency reference on or off (bit 1 low for on and high for off); 3) single sweep operation (bit 2 high); 4) sweep rate selection (bits 3-7, see Table 7-11)

**TABLE 7-11
SWEEP RATE SELECTION CODES**

Sweep Rate	D7	D6	D5	D4	D3
20 μ s/div	1	1	0	1	1
50	1	0	1	1	1
100	1	0	0	1	1
200	0	1	0	1	1
500	0	0	1	1	1
1 ms/div	0	0	0	1	1
2	1	1	0	0	1
5	1	0	1	0	1
10	1	0	0	0	1
20	0	1	0	0	1
50	0	0	1	0	1
100	0	0	0	0	1
200	1	1	0	0	0
500	1	0	1	0	0
1 s/div	1	0	0	0	0
2	0	1	0	0	0
5	0	0	1	0	0
10	0	0	0	0	0
Manual	1	1	1	1	1
External	0	1	1	1	1

Commands written to address 1F control the triggers and sweep holdoff time. These commands are as follows: 1) abort sweep without starting another in the single sweep mode (bit 0 goes high); 2) ignore input trigger signals (bit 1 high); 3) disable sweep gate and blank non-store display (bit 2 high); 4) trigger mode (controlled by bits 3 & 4, see Table 7-12); 5) sweep holdoff time (bits 5 & 6, see Table 7-13); 6) interrupt at end of sweep (bit 7 goes high).

Table 7-12

TRIGGER MODE	D4	D3
Free run	0	0
Internal	0	1
External	1	0
Line	1	1

Table 7-13

SWEEP HOLDOFF	D6	D5
Short	0	0
Medium	0	1
Long	1	0

Address 9F reads the Frequency Reference Lock module status. An interrupt is generated when a change in status of the reference lock occurs. When the internal reference frequency is in use, bit 0 is high. When an external reference is used, the bit goes low. When the 100 MHz, 3rd LO, is locked to the frequency reference, bit 1 is high; and conversely, if the bit is low the 3rd LO is not locked.

The sweep board consists of five major circuits: 1) the sweep generator, which generates the voltage ramp that drives the Deflection Amplifiers, Digital Storage, the Preselector, and the swept oscillators; 2) the trigger circuits, which process and multiplex the three trigger signals; 3) the sweep control circuit, which generates the SWEEP GATE and PEN LIFT signals and determines the holdoff time for the sweep generator; 4) the digital control circuits, which receive and decode the address and instructions from the microcomputer, select the sweep rate, holdoff time, trigger source, sweep mode, select internal or external reference frequency, and control interrupts to the microcomputer; 5) the interface between the microcomputer and the Reference Lock module.

The analog section of the Sweep board consists of, the ramp or sweep generator plus its output buffers that drive

the deflection amplifiers, the oscillators, digital storage, Z axis, and the trigger circuits. The sweep and trigger circuits are digitally controlled.

The Sweep Generator

The sweep generator is an integrator circuit consisting of operational amplifier U2062 with one fixed and two selectable capacitors in the feedback circuit. The fixed capacitor (C1061) is used for the faster sweep rates. The other two capacitors (C1065 or C1062) are added, to change the time constant, when either Q1061 or Q1058 are switched on by comparators in U3054. These comparators are driven by register U2032, which interfaces to the instrument bus. For manual sweep operation, Q1064 is turned on and the integrator (U2062) becomes an amplifier.

Timing resistors are connected between a -12 V reference, out of U3059B, and the input to the integrator U2062 by multiplexer U3064. Data bits D5, D6, and D7 of address OF drive the select inputs of the multiplexer. The voltage reference of -10 V out of U2061 is boosted to -12 V by U3059B. A voltage divider (R2065, R2063) sets the non-inverting input of U2062 to -8 V and feedback sets the inverting input to the same potential. Therefore a difference of about 4 volts exists across the timing resistors. The timing current through the resistors varies over two decades such that $1/I$ is proportional to a 2-5-10 sequence by U2061.

Switching in feedback capacitors C1061, C1065, and C1062, changes the sweep rate 100 times. Sweep Accuracy adjustment (R1063) compensates for differences in timing voltage or timing circuit values. The timing capacitors are matched so one adjustment compensates for small variations in each set.

Trigger Circuits:

The sweep circuit can be triggered by: an externally applied signal, the internal video, or from the line. Each trigger signal is converted to TTL level before it is applied to the trigger multiplexer which is part of the trigger control circuit. The trigger control circuit selects the desired triggering signal and triggering mode or rejects the trigger so the sweep circuit free runs, is manually controlled or the external sweep mode is used.

An external trigger signal, that is applied to the external HORIZ/TRIG connector, is converted to TTL level by Q1052. CR1046 and CR1044 limit any voltage surges that may be on the line. Line trigger signals, from the power supply, are filtered by R1026 and C1039 then applied through comparator amplifier U1015C to the multiplexer. Video signals from the Video Processor are buffered by Q1051 and converted to TTL level by Q1053. Both the ex-

ternal and video trigger signals are applied to multiplexer U2026, through a Schmitt trigger inverter in U1037.

Under control of the data (D3,D4) out of register U1032, the multiplexer selects the trigger signal and passes it to flip-flop U1026B. After retrace and holdoff time, U1026B allows a trigger to pass through U2026 and U2015C to reset the Sweep State Control flip-flop U3021. When U3021 is reset the integrator starts a new sweep.

Sweep Output Circuits

The sweep ramp from the integrator is applied through buffer amplifiers, U3042 and U3048, and a bus on the Mother board to; the Deflection Amplifiers, Span Attenuator, and Digital Storage board. The sweep out of U3042 is an 11 V peak-to-peak ramp centered around 0 V. The sweep out of U3048 is a 22 V peak-to-peak ramp for the oscillator.

The sweep signal also drives a pen-lift comparator U1015B, and the end-of-sweep comparator U1015A. The threshold for the pen-lift comparator is $+7.4\text{ V}$. The threshold for the end-of-sweep comparator is $+8\text{ V}$. The sweep ramp, from the integrator, starts at -8 V and rises towards $+8\text{ V}$. When the signal reaches $+7.4\text{ V}$, the pen lift comparator toggles. This output is gated through U3015B and the pen lift signal goes high. When the sweep ramp reaches -8 V , the end-of-sweep comparator, U1015A, toggles. The resultant low output is applied through U1037A to become the EOS (end-of-sweep) signal.

Sweep Control Algorithm

U3021 is the Sweep State Control flip-flop. When reset, the high at the \bar{Q} output turns the FET Q1062 off and allows the integrator capacitors to charge. When the Sweep State Control flip-flop (U3021) is set, by a low on pin 4, its \bar{Q} goes low. This switches the output of comparator U3054B so its output turns Q1062 on and discharges the timing capacitors. The \bar{Q} output of U3021 connects to pin 5 of U2021A so this low switches the output pin 6 to its high impedance state (its output is open collector). The Q output of U3021 is high. Both U1026A and U1026B were previously set when the Q output was low. This starts the holdoff cycle or retrace time which is described detail further on.

The Sweep State Control flip-flop U3021, is set by a low out of NOR gate U2015A when either the EOS (end-of-sweep) or the ABORT SWEEP lines go high. ABORT SWEEP is generated when a 1 is written to D0 that is coincident with address 1F. The Sweep Control flip-flop is reset by either a trigger signal from multiplexer U2026 or a high on the MNL or EXT SWP line. The microcomputer writes to

bits 5 and 6 at address 0F for the manual or external sweep mode.

Trigger Control Algorithm

A sweep is initiated by the microcomputer, in single sweep or manual mode as noted above, or by one of three trigger signals selected by the multiplexer U2026. Data bits D4 and D3, at address 1F (see Table 7-12) select the input trigger signals and route them to the clock input of U1026B. During sweep time the flip-flop U1026B is set by a low on the Q output of U3021.

The high on the \bar{Q} output of U3021 is also applied through an inverter buffer, in U2021A, and the resultant low out discharges the holdoff capacitor C1018, at the input to U1015D. The output of U1015D is low so the output of NAND gate U1038D is high. The multiplexer U2026 requires a high-to-low transition to clock any input through. Since it is high, incoming trigger signals will have no effect on the circuit.

At the end of sweep, the \bar{Q} output of U3021 goes low. This switches the output of U2021A to its high impedance state and the holdoff capacitor, C1018, starts to charge towards +15 V through R1020. When it reaches +5 V the comparator output switches high. This, along with a high on pin 13 of NAND gate U1038D, causes the output to go low and the high-to-low transition clocks U2026 so the incoming trigger signal can now clock U1026B and produce a high at the \bar{Q} output. This is gated through U2026 to the input of U2015C, so the output of the NOR gate will now reset the Sweep Control flip-flop, U3021, and start a new sweep.

In the free-run mode the multiplexer U2026, selects the +5 V on pin 6. This high is clocked through to the Sweep State Control flip-flop immediately after retrace. Incoming trigger signals are ignored and the sweep runs in an astable mode. The microcomputer writes a "1" to bit 1 at address 1F. This is inverted by the buffer in U2021 and pulls the input to NAND gate U1038D, low which disables the multiplexer U2026.

In single sweep mode the sweep circuit cannot be re-triggered until it is armed by the microcomputer. A "1" is written into bit 2 at address 0F. This appears as a high on pin 2 of U3015A. Since U1026A has been set by the previous sweep, the two highs at the input produce a low at pin 13 of U1038D. Incoming triggers therefore, are disabled. The sweep is now in an idle state and can not run until the microcomputer "arms" the trigger circuit again. This is done by writing a "1" to address 0F which produces a high out of U3038C and clocks flip-flop U1026A. The resultant low at pin 1 of U3015A forces a high at pin 11 of U1038D, and arms the trigger circuit. Thus a signal can now trigger the sweep circuit and the single sweep cycle repeats.

Sweep Holdoff

During retrace, the sweep must be held off long enough for the timing capacitors in the integrator to discharge and the circuit to stabilize. To prevent flicker, the holdoff period must vary as sweep time changes. U1015E and three selectable timing capacitors (C1018, C2022, and C2023) plus a resistor (R1020) form the holdoff circuit.

During sweep time pin 5 of U2021A is high. This pulls pin 6 low and discharges C1018. During retrace, pin 6 is released and the timing capacitors start to charge. When they reach +5 V, comparator U1015E toggles and its output goes high. This, along with the high on pin 13 of the NAND gate U1038D, provides the clock pulse for U2026 to pass a trigger signal through to the Sweep State Control, U3021.

Interface Circuits

In addition to the sweep circuits, there are circuits that interface between the microcomputer and the Reference Lock module. These circuits; generate an interrupt (SER REQ) when a change of status in the Reference Lock module occurs, respond to the POLL routine, and provide data so the microcomputer can monitor the status of the Reference Lock module.

To determine the status of the Reference Lock module, the microcomputer reads the status of bits 0 and 1 (DB0 & DB1) of the data bus. These two bits connect, through tri-state buffers U1042A and U1042D, to the INTL REF and REF LOCK lines from the Reference Lock module. INTL REF line is high when the internal reference is used and low for external reference. REF LOCK goes high when the 3rd LO is not locked to the frequency reference and low when it is locked. The buffers in U1042D are enabled when address 9F is read.

At the time a read is done, U2043 is enabled and latches the input data. Thus, the bits on pins 1, 2, and 5, 6, of the exclusive-nor gates on U1048 match each other. The open-collector outputs are wired together, so when the outputs are high, inverter U2021B applies a low to the clock input of flip-flop U2048A. When a change in status occurs, one of the bits to the exclusive-nor gates (pin 1 or pin 5) changes. There is now a difference between the present status and the previous status, stored in U2043. One output of U1048 now outputs a "0" and a low-to-high transition occurs on the clock pin of U2048A. This triggers an interrupt and causes the microcomputer to inquire about the new status. Reading the new status, activates the latch and resets the circuit. Transistor Q2038, driven by bit 1 at address 0, turns the INTL REF (internal reference) on or off. When "0" is written at address 0F, the status of data bit 1 turns the frequency reference off or on.

U2048 is part of a circuit that generates the instrument bus interrupts and responds to the subsequent poll routine from the microcomputer. There are two sources of an interrupt from the sweep board, either an EOS (end-of-sweep) has occurred or a change of status of the reference lock module has occurred. When an EOS occurs, and provided the EOS Interrupt Enable bit is high, the flip-flop U1022A is clocked and its \bar{Q} goes low. This produces a high out of U1038B which turns Q2036 on to pull the instrument bus line SER REQ (service request) low and forces an interrupt.

The microcomputer response to an interrupt is with a poll routine. It first writes "FF" to the instrument address bus. None of the decoders respond, but bit 7 of the address bus (AB7) goes high. The microcomputer raises the POLL line and reads the instrument data bus. The output of U3038A goes low. This, added with the low out of U1022A, generates a high to turn Q2034 on and pull bit 4, of the instrument bus, low. When the microcomputer reads a low on bit 4 it lowers the POLL line and writes 7F on the instrument bus. None of the decoders respond, however, bit 7 (AB7) of the address is pulled low. The microcomputer now writes a word to the data bus with all bits except 4 high. This acknowledges the interrupt. The microcomputer now raises the POLL line and, since both inputs to U3038B are high, the output of the gate goes low. The POLL line is then pulled low and the low-to-high transition clocks the low on the D input of U1022B through to reset U1022A. Its Q output then sets U1022B. Q2036 is cut off, the interrupt is removed, and the circuit is now ready for another EOS.

When a change-of-status occurs, in the reference lock module, a low-to-high transition occurs on the clock input of U2048A to latch the Q (pin 5) output high and the \bar{Q} output low. This low is gated through U1038B to turn Q2036 on, and pull SER REQ line low. When the microcomputer responds, by writing "FF" and raising the POLL line, U3038A output goes low, however, at this time U2015B output goes high, because of the low on pin 6 of U2048A-6. This turns Q2018 on and bit 6 on the data bus goes low. The microcomputer reads this and pulls the POLL line low. Address "7F" is written on the address bus and the POLL line is raised. This forces U3038B to output a low and the POLL line again goes low to toggle U2048B. The low output at Q resets U2048A to remove the interrupt or SER REQ. At the same time U2048B is reset and the circuit is ready to repeat the sequence.

SPAN ATTENUATOR



The Span Attenuator, under control of the microcomputer, selects the appropriate attenuation factor for the incoming sweep signal, to establish the frequency span. Refer to the block diagram adjacent to Diagram 32 as well as

the schematic diagram. The Span Attenuator consists of digital control circuits, which receive and decode the address and instructions from the microcomputer; the input amplifiers, which perform noise reduction and signal inversion on the incoming sweep signal; the digital-to-analog converter, which attenuates the sweep signal to the desired amplitude for driving the 1st LO Driver and Preselector Driver circuits; and the decade attenuator, which provides three decades of attenuation for the output signals.

Digital Control

Decoder U5025 decodes the address information from the address bus and sends a low signal to either of the two latches, U1025 (address 75) or U2015 (address 76), when a latch is addressed and the DATA VALID line moves high. (The data is stored in the latches on the trailing edge of the DATA VALID signal. Logic buffer U4015 reduces loading of the data bus. Latch U1025 stores data that controls the eight least significant digits of the span attenuation factor. Latch U2015 stores data that controls the two most significant digits of the span attenuation factor, and other functions on the board. When a span attenuation factor is selected, the microcomputer selects an address and places the first byte of the data on the bus. The DATA VALID signal causes the data to be stored in one of the two latches. Then the second address is called and the next byte is stored in the other latch. The block diagram illustrates the significance of each bit in tables near the affected circuit. A logic 1 represents the more positive of two levels or high state, and a logic 0 represents the more negative of two levels or low state.

Input Section

The sweep signal and its ground reference are applied to differential input buffer U3036. Any signals or noise induced in the two signal transmission paths are cancelled by this stage.

The following stage consists of amplifier U3032, plus switching transistors Q2025, Q2028, and Q2023. Different mixing modes require the 2nd LO frequency to either increase or decrease to increase the signal frequency. Thus, this circuit is a unity gain amplifier that can be changed from inverting to non-inverting, under bus control. When line Q8 of latch U2015 is low, Q2023 conducts and its collector moves positive to about +5 V. This in turn causes both Q2025 and Q2028 to conduct. Pin 3 of U3032 is effectively grounded, the sweep signal is applied through R3028 to the summing node of the amplifier, and the gain of the stage is -1. If line Q8 is high, Q2023 does not conduct and the voltage at its collector falls to nearly -15 V. Neither Q2025 nor Q2028 are now in conduction, so the sweep signal is applied to pin 3 of U3032, and pin 2 is disconnected. Now, the gain of the stage is +1.

Digital-To-Analog Converter

The magnitude of the sweep signal is determined by the desired frequency span, band, and option installed in the instrument. The microcomputer calculates the proper magnitude for each combination, and sends the appropriate codes to the data latches, which in turn control the attenuation factor of the digital-to-analog converter. This stage consists of converter U1042, amplifier U2042, and a complementary pair, Q2062 and Q3056, that form the output current buffer.

Figure 7-23 illustrates a simplified two-bit digital-to-analog converter. The circuit works by current division. Since the summing node of the amplifier is at ground potential, the magnitude of the current through a resistor is not affected by the position of the switch that selects that resistor. For example, when switch S1 is at position B, the current is shunted to ground. When S1 is at position A, the current through R1 becomes part of the total output current. Thus, the output current can be 0, 1/4, 1/2, or 3/4 of the total current available. Because of the resistance ratios, the ratio of the output voltage to the input voltage equals the ratio of the output to the total current ($V_{out}/V_{in} = I_{out}/I_{total}$). In this 2-bit converter, there are 2^2 or 4 output values possible. In the actual 10-bit converter, there are 2^{10} or 1024 output values ranging from 0 to 1023/1024 of the input.

In converter U1042, each internal resistance is switched in or out by a CMOS FET (internal to the device). The CMOS inputs are each protected by a series input resistor. Since the sweep signal is applied to the V_{ref} input, U1042 serves as a digitally controlled attenuator for the sweep signal.

The attenuated sweep signal from U1042 is applied to U2042, an operational amplifier. It in turn drives an output current buffer, consisting of complementary pair Q2062/Q3056. The pair is biased to produce a standing current of about 10 mA in the absence of an applied signal. This eliminates crossover distortion of the output signal. Diodes CR2051, CR2053, CR1051, and CR1049 provide temperature stabilization for the bias current in the stage. When high current is passing through the pair, diodes CR1056 and CR1061 clamp the voltage across the emitter resistors to reduce voltage drop.

Feedback for the output stage is provided by R1056, plus an internal resistor in U1042. The internal feedback resistor ensures better temperature tracking. The internal resistor provides a gain slightly less than unity; R1056 increases the stage gain and permits gain calibration, as described below.

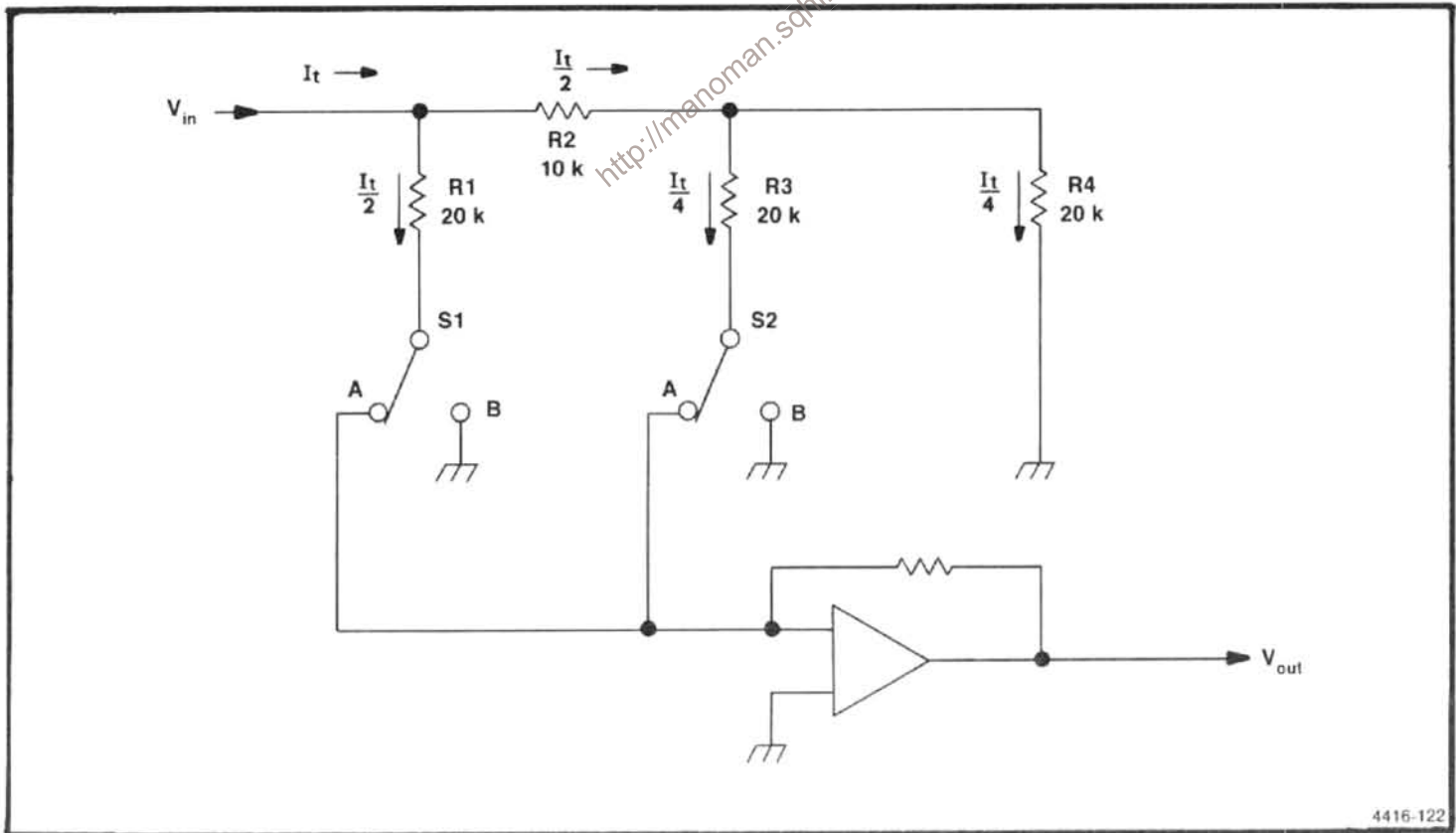


Figure 7-23. Simplified digital-to-analog converter (DAC).

One-of-four decoder, U4025, uses data bits DB3 and DB4 lines from U2015, to control three sections of a quad FET switch, U3025. (RC circuit inputs of each FET control line filter out noise from the digital circuits.) The code is exclusive; i.e., only one FET is switched on at a time. See Table 7-14 for a listing of the codes. When a FET is switched on, it connects a calibration adjustment potentiometer to the summing node of the operational amplifier. Adjustment R1065 sets the 1st LO tune coil sweep, R1071 sets the 1st LO FM coil sweep, and R1067 sets the 2nd LO span.

Table 7-14
CALIBRATION CONTROL SELECTION CODES

U4025		Selected Adjustment
DB 3 (Pin 3)	DB4 (Pin 2)	
0	0	R1065 (main coil)
0	1	R1071 (FM coil)
1	0	R1067 (2nd LO)

Decade Attenuator

Since accuracy of the digital-to-analog converter is specified as a percentage of full scale, the accuracy decreases as the attenuation is increased. To maintain accuracy at 1%, it is never used at an attenuation factor of more than ten. If more attenuation is required, the decade attenuator, consisting of K4072, K3075, K3065 and the connected divider network, provides further sweep attenuation of X0.01, X0.1 and X1 (see Figure 7-24 for a simplified circuit diagram).

The "2" side of U4025 is controlled by data bits, DB5 and DB6, on the Q6 and Q7 lines from U2015. The "2Y" outputs of U4025 are applied through buffers in U4042 to select the appropriate attenuation factor for the output sweep. Table 7-15 lists the states required to energize the attenuation relays. A diode across each relay coil protects the driving circuit from inductive feedback transients.

Table 7-15
ATTENUATION SELECTION CODES

U2015		Attenuation Factor
Pin 15 DB5	Pin 16 DB6	
0	0	X1 (K3065)
1	0	X 0.1 (K3075)
0	1	X 0.01 (K4072)

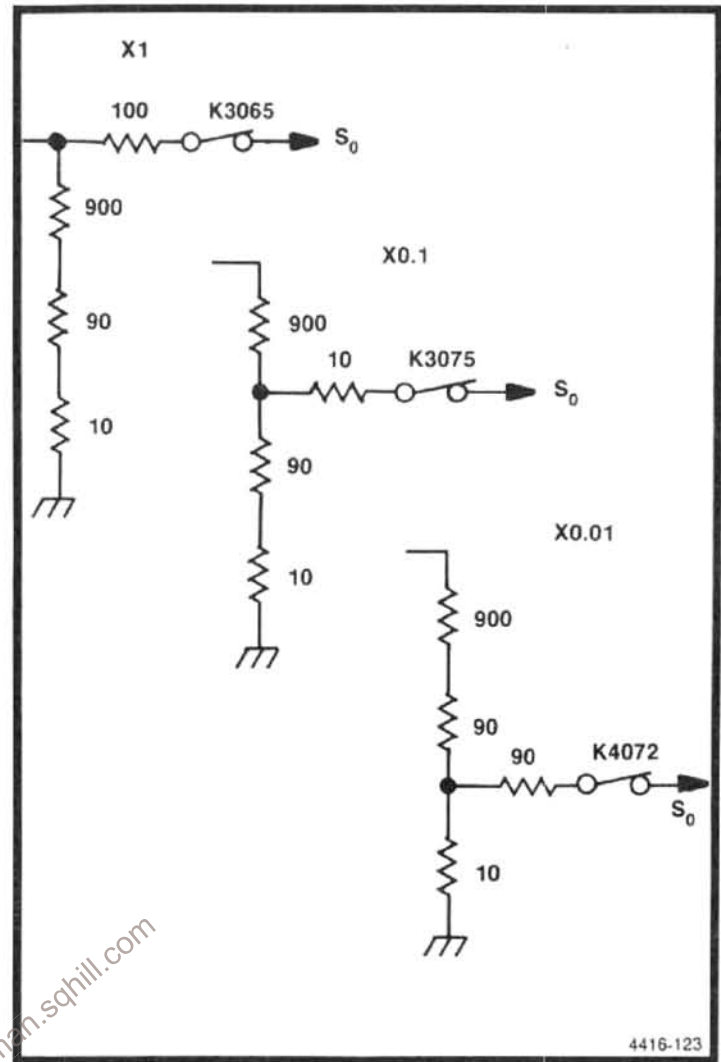


Figure 7-24. Simplified span decade attenuator.

1st LOCAL OSCILLATOR DRIVER 33

The 1st LO Driver performs the following functions: 1) Buffers the TUNE VOLTS signal and applies it to the dot marker circuit; 2) combines the SPAN VOLTS with the COARSE TUNE VOLTS and outputs the combination to the Preselector Driver (the combined signal is also applied to the Oscillator Driver circuits, which drive the 1st Local Oscillator coil); 3) selects and outputs the appropriate bias voltage to the internal or external 1st Mixer; 4) outputs a voltage to the Preselector Driver that peaks the Preselector; 5) controls the oscillator filter switch; 6) produces a stable and precise -10 V reference for both the 1st LO Driver and the Preselector Driver circuits.

The major circuits and their function are as follows:

1. The digital control circuits buffer the incoming data from the data bus, decode the address data, select the required mixer bias, connect or disconnect the TUNE VOLTS and SPAN VOLTS signals to the summing amplifier, energize the filter switch in the 1st LO assembly, and control the drive and filtering of the oscillator driver stage.

2. The tune volts buffer buffers the COARSE TUNE VOLTS signal between the Center Frequency Control and the dot marker circuit on the Crt Readout board. It also reduces the signal amplitude to drive the dot marker circuits.

3. The oscillator filter switch driver furnishes drive current to the capacitor switching relay in the 1st LO assembly.

4. The input switching circuit connects or disconnects the SPAN VOLTS and COARSE TUNE VOLTS signals to the input of the summing amplifier.

5. The summing amplifier furnishes the drive signal to the oscillator driver. The summing amplifier sums the SPAN VOLTS ramp signal, from the Span Attenuator, with the COARSE TUNE voltage, from the Center Frequency Control circuit. In less than maximum span, a sweep voltage of ± 10 V sweeps the oscillator at a rate of 333 MHz/division. As the TUNE VOLTS signal varies from -10 to $+10$ V, the oscillator's center frequency is moved over its full range.

6. The oscillator driver furnishes the current drive for the 1st LO coil.

7. The -10 V reference supply produces a precise -10 V reference for the 1st LO Driver and the Preselector Driver.

8. The mixer bias circuit produces and outputs the required bias voltages for the 1st Mixer.

9. The programmable bias circuit provides peaking voltage for the Preselector or external mixers bias voltage based on data supplied by the microcomputer.

Digital Control

The digital control circuit sets the oscillator span volts, the 1st Mixer bias and programmable bias for the 494P. Decoder U4034 output Y1 (pin 14) goes low when the input address is 72 and output Y7 goes low for address 7E. When output Y1 goes high, data is clocked or latched into U4017, and when Y7 goes high data is latched into U4024 and U4022.

Data for U4017 consists of control codes for the oscillator drive circuits and the switches in U1016, which select 1st Mixer bias or the bias set by the front panel MANUAL PEAKING control. The codes are described where each applies to the description and in Table 7-16. Data for DAC U3022 is converted to an analog signal which provides the Programmable Bias for the instrument.

Tune Volts Buffer. The tune volts buffer consists of amplifier U1025B and surrounding components. The COARSE TUNE VOLTS signal, from the Center Frequency Control circuits, is divided down by R1028,R1027, and applied through a unity gain amplifier, U1025B, to the dot marker stage in the Crt Readout circuits.

Table 7-16
U4017 OUTPUT LINES

Low		High	
Q1(DB0)	Bias 1 connected	Bias 1 disconnected	
Q2(DB1)	Bias 2 connected	Bias 2 disconnected	
Q3(DB2)	Bias 3 connected	Bias 3 disconnected	
Q4(DB3)	Manual peaking connected	Peaking disconnected	
Q5(DB4)	Driver filter disconnected	Driver filter connected	
Q6(DB5)	Driver input connected	Driver input disconnected	
Q7(DB6)	SPAN VOLTS line disconnected, oscillator filter connected	SPAN VOLTS line connected, oscillator filter disconnected	
Q8(DB7)	Maximum span; TUNE VOLTS line disconnected	Normal span; TUNE VOLTS line connected	

Input Switching. This stage consists of FET Q2033, comparators U3014A and U3014C, and FET Q2026. When maximum span is selected, line Q8 of U4017 goes low, causing U3014C to switch. This turns Q2026 on and shunts R2031 with R2030, increasing the stage gain of U2032. This low is also applied to the comparator U3014A, which switches and cuts off Q2033. This disconnects the TUNE VOLTS signal to the summing amplifier U2032; the TUNE VOLTS is now used to position a marker on the display at the center frequency. The span voltage sweeps the oscillator over its full frequency range.

If the main coil of the oscillator is not to be swept, DB6 (line Q7 of U4017) goes low. This cuts Q3028 off, de-energizes K3034 and disconnects the SPAN VOLTS signal to the summing amplifier. Diode CR3031 protects Q3028 from the inductive feedback surges that occur at turn-off.

Oscillator Filter Switch Driver. When relay K3034 is deenergized, DB6 is low, Q2029 is biased on which drives a capacitor-switching relay on the 1st LO Interface board. The capacitors are switched across the main coil, when it is not being swept, to filter noise riding on the tuning current. Capacitor C2025 provides a gradual decay of current through the relay after power is turned off.

Summing Amplifier. Amplifier U2032 and the complementary pair of transistors, Q2035 and Q2039, plus related components, comprise an operational amplifier. The COURSE TUNE VOLTS and the SPAN VOLTS are summed at the input to U2032. The feedback resistor, for the operational amplifier, is R1038. The input resistance is R2027 for the COARSE TUNE VOLTS signal and R2031 for the SPAN VOLTS signals. (R2030 is switched across R2031, as mentioned previously, to increase stage gain for maximum span operation.) The output of the summing amplifier, which can swing from -10 V to $+10$ V, is applied to the Preselector Driver circuits and to the Video Processor board.

Oscillator Driver. The output of the summing amplifier also drives the input to the oscillator driver stage when FET Q2040 is switched on. The oscillator driver stage consists of active components Q2045, U2043, Q3047, and Q352. The input resistance consists of R2041, the 1st LO Sensitivity adjustment R1031, plus R2043. The feedback resistance is R2042. The amplifier converts a voltage input into a current drive for the 1st LO tuning coil by controlling the voltage across current sense resistor R1040, which is in series with the oscillator tune coil. Q3047 assures that Q352 base current remains within the oscillator tuning coil circuit. Q2040 is biased on except when the oscillator is degaussed. The output of the operational amplifier U2032, Q2039 and Q2035, is applied through the 1st LO Sensitivity adjustment R1031, and summed with an offset voltage set by the 1st LO Offset adjustment R1032, at the input to the preamplifier stage

Q2045. Adjustments R1031 and R1032 match the oscillator driver stage to the oscillator characteristics. R1032 adds offset to the input of the preamplifier to place the oscillator at center operating frequency when the amplifier input is at zero volts.

Q2045 is a low-noise, matched, dual transistor. The feedback path through R3040 and R2042 sets the voltage across a four-terminal resistor R1040. This voltage sets the current through the resistor which is also emitter current for driver transistor Q352. The 1st LO Sensitivity adjustment R1031, sets the voltage gain of the amplifier. This in turn, changes the current drive to the oscillator coil.

Capacitor C3038 lowers the noise bandwidth of the output amplifier when it is switched into the circuit by Q3042. Because of its effect on the tuning rate of the 1st LO, the capacitor is only in the circuit in phase locked spans with the ϕ Lock switch off (other than 494/494P spectrum Analyzers). Since the 494/494P control system does not allow the phase lock to be turned off, DB4 is held low and Q3042 is biased off, effectively removing C3038 from the circuit.

Reference Supply. Preamplifier Q2052 plus amplifier U2052 and emitter follower Q2051, are the active components of the -10 V reference supply. Bias for one side of Q2052 is set by VR1055. The other side is set by the -10 V Ad. R1034. Any change in the supply is amplified by Q2052 which changes the drive to the pass transistor Q2051 which compensates for the change. The diode network across the base-emitter junction limits the emitter current to about 30 mA, protecting the transistor from damage.

Mixer Bias Driver. The mixer bias driver circuit, which consists of quad FET switch U1016, amplifier U1025A, and buffer Q2025/Q1028, plus associated circuitry, furnishes the required bias current (up to 20 mA) to the 1st Mixer circuit. The bias voltage varies from $+1$ V to -1 V for the internal mixer, and from $+1$ V to -2.25 V for an external mixer. External mixer bias voltage range can be changed to -1 to $+2.25$ V by moving the strap J2014 from $+12$ V to the -12 V supply.

Mixer bias is selected, by the data out of U4017 to the quad FET switch U1016, and fed to the inverting input of U1025A. The output of U1025A drives the base of a pair of complementary transistors Q1028 and Q2025 which provide the 1st Mixer Bias voltage. When any of the Q1 through Q4 (D0 to D3) lines of U4017 go low, the respective switch within U1016 closes and connects one of the Bias adjustment potentiometers or the output of U2018 (the programmable bias line) to the input of U1025A.

When the Q4 (DB3) line of U4017 goes low, U1016 selects the Programmable Bias line as the 1st Mixer Bias source. This occurs when External Mixer mode is selected. The Programmable Bias is set by the data loaded into DAC U3022, by the microcomputer, or by the front panel MANUAL PEAK control. The MANUAL PEAK control is connected to the input of U2018 when the Q5 line (DB4) of U4024 goes low and turns Q3019 on. When MANUAL PEAK is selected, the DAC output is set for 0 V.

Programmable Bias. When the microcomputer sends address 7E to decoder U4034, pin 7 (output Y7) goes low. At the end of data output cycle, data is clocked into either U4024 or U4022, depending on which latch is enabled by DB6 or DB7. This data is then converted to an analog current by U3022 which is the current source for operational amplifier U2018. The resistance between output terminals 16, 2, and 15 of U3022 is the input resistance for operational amplifier U2018. R2022 is the feedback resistance. The output of U2018 is a bias voltage that is fed, via the Programmable Bias line, to either the Preselector Driver board where it is summed with the drive voltage for the Preselector; or, it is fed through U1016/U1025A, and Q1025/Q2025 to the 829 MHz Diplexer, then through the Transfer Switch on the RF deck to the External Mixer port.

Oscillator Collector Supply. This circuit comprises amplifier U4055, buffer Q3049, and surrounding circuitry. U4055 holds Q3049 in saturation, so the collector of the transistor remains at a fraction of a volt below +15 V. This voltage is applied to the 1st LO collector.

PRESELECTOR DRIVER



The Preselector provides RF input selectivity between 1.7 and 21 GHz. This selectivity reduces spurious responses over this frequency range. Refer to the block diagram adjacent to Diagram 34 as well as the schematic. The Preselector Driver supplies the drive current to the Preselector coil, depicted on Diagram 12, to tune the Preselector. It also furnishes a voltage that is proportional to frequency change through the rear-panel ACCESSORIES connector for an external preselector, if used. The circuit also operates the filter select relay that selects either the Preselector or Low-pass Filter. The major circuits and their function are as follows:

1. The digital control circuit, which stores and decodes the data from the microcomputer and controls the other circuits within the Preselector Driver. The digital control circuit; applies the SPAN VOLTS signal to the oscillator voltage processor when FM coil spans are selected, selects the gain of the oscillator voltage processor, turns off the drive signal to the current driver for degauss cycles or when the preselector is not in use, selects the IF offset voltages to be

combined with the FINE TUNE VOLTS signal, adds noise filtering at the driver output when the preselector is not being swept, and controls the filter select switch;

2. The oscillator voltage processor, which attenuates and offsets the input signal for application to the summing amplifier.

3. The IF offset stage, which applies an offset voltage to the summing amplifier. This offset is proportional to the 1st IF frequency in use, including the effects of fine tuning frequency changes of the 2nd Local Oscillator.

4. The summing amplifier, which combines the effective oscillator frequency voltage and the IF Offset voltage to drive the tracking adjustment circuits.

5. The tracking adjustment circuit, which compensates for different preselector sensitivities, compensates any preselector offset, and compensates for non-linear operation caused by magnetic saturation of the Preselector.

6. The final driver stage, which changes the applied signal voltage into a current drive for the Preselector coil.

The preselector switch driver, which drives the filter select switch, depicted on Diagram 12. The switch requires a positive pulse to select the Low-pass Filter and a negative pulse to select the Preselector.

Digital Control Circuits

The microcomputer interface circuits, which exercise digital control of the Preselector Driver circuits, consist of address decoder U5036 and latch U5031. Both the write address (77) and the read address (F7) are decoded by U5036.

Data is latched into U5031 on the trailing edge of the DATA VALID signal for address 77. This event coincides with the rising edge of the pulse on pin 3 of U5036. Table 7-17 lists output lines from U5031.

In some 49X series instruments, the read address function is used by the microcomputer to determine if the instrument is equipped with an option that includes the Preselector. The Preselector is installed in all versions of the 494/494P. When address F7 is specified, the Y7 line of U5036 goes low. This pulls data line D4 low, informing the microcomputer that a Preselector is used.

Table 7-17
U5031 OUTPUT LINES

High		Low
Q1(DB0)	Selects X1 gain for U2028.	Selects X3 gain for U2028.
Q2(DB1)	Not used.	Not used.
Q3(DB2)	Connects tracking adjustment output to final driver stage.	Disconnects tracking adjustment output from final driver stage. (Preselector current goes to zero.)
Q4(DB3)	Connects SPAN VOLTS signal to U1011A input for FM coil spans.	Disconnect SPAN VOLTS from U1011A.
Q5(DB4)	Selects Low-pass Filter (Band 1).	Selects Preselector (Bands 2-5).
Q6(DB5)	Disconnects output filtering.	Adds output filtering.
Q7(DB6)	Connects -829 MHz offset.	Disconnects -829 MHz offset.
Q8(DB7)	Connects $+829$ MHz offset.	Disconnects $+829$ MHz offset.

Oscillator Voltage Processor

The oscillator voltage processor consists of U1011A, U2028, and related components. The Preselector Drive signal from the 1st LO Driver is applied to a voltage divider and scaling network consisting of R1022, R1023, R1024, and Input Offset adjustment R1031. The input voltage is ± 10 V. This voltage is the summation of the sweep and tune voltages, with appropriate scaling. The output of the voltage processor is about 1 V at 2.072 GHz to about 3 V at 6.35 GHz, which corresponds to a scale factor of 2.1 GHz/volt. The voltage is directly proportional to frequency; thus the offset is such that if the oscillator could operate to 0 Hz, the voltage processor output would be at 0 V.

Since the preselector drive input is not swept by the 1st LO Driver, when FM Coil spans are used, the SPAN VOLTS, from the Span Attenuator, must be summed by this stage. Line DB3 (Q4 of U5031) goes low when FM coil spans are selected, which turns Q1011 on. This switches the FET Q1022 on so the Span Volts signal is now applied to the inverting input of U1011A, where it is inverted and applied to the input of U2028.

Operational amplifier U2028, has a gain of 1 or 3, as directed by the microcomputer. The output signal in the X3 gain mode represents the effective oscillator frequency swing for bands 4 and 5 when the 3rd harmonic of the LO is used. When the DB0 (Q1 line of U5031) goes low, the respective output of quad comparator U5022 is also low, which holds FET Q2024 cut off. U2028 is now a unity-gain, non-inverting amplifier. When the DB0 goes high, Q2024 switches on and the gain of U2028 is a factor of three. The X3 Gain adjustment, R1052, sets the gain to precisely three in the tripler mode.

IF Offset

The -10 V reference, from the oscillator driver, furnishes the precise reference voltage for the IF offset circuit. Since the offset voltage is proportional to the IF -2.072 GHz, no offset is required for the $+2.072$ GHz IF. FET Q2034 adds the $+829$ MHz network into the circuit and Q2036 adds the -829 MHz network. DB6 and DB7 (Q7, Q8 of U5031) through two comparators in U5022, control the two FET switches Q2034, Q2036. One, but not both, transistors are switched on to provide the offset voltage to the inverting input of U2045. An output voltage of -9 V from the amplifier corresponds to (-829 MHz) -2072 MHz or -2901 MHz.

The signal on the FINE TUNE VOLTS line, from the Center Frequency Control board, which is used to tune the 2nd Local Oscillator, is applied to the input of U2047. Since it is applied here, it is independent of the voltage tripling action in the voltage processor circuit. The tuning voltage is also applied to the input networks of U2045 through R3044, Q2034, and R1037, Q2036. By varying the magnitude of signal in the inverting path compared to the direct path, the proper magnitude and polarity of fine tune offset for each IF is provided. Table 7-18 lists the offset voltage required for each frequency band.

Summing Amplifier

The effective oscillator frequency voltage, from U2028, and the offset IF voltage, from U2045, are applied to the inverting input of U2047. This stage drives the tracking adjustments stage and furnishes a signal for external preselector drive circuits as well. The external drive line has its own return to reduce ground loops.

Table 7-18
PRESELECTOR FREQUENCY BANDS

Band	Frequency Range	IF	Harmonic	Approximate Voltage Offset
2	1.7-5.5 GHz	- 829 MHz	1st	9.0 V
3	3.0-7.1 GHz	+ 829 MHz	1st	3.9 V
4	5.4-18.0 GHz	- 829 MHz	3rd	9.0 V
5	15.0-21.0 GHz	+ 2.072 GHz	3rd	0 V

Tracking and Shaper Circuits

This stage consists of gain-setting, offset, and shaping circuits. Presel Sensitivity adjustment R1065 compensates for sensitivity variations between preselectors. Presel Offset adjustment R1064 compensates for the offset in the preselector. This adjustment sets the preselector frequency to 2072 MHz when the output of U2047 is at zero volts.

The four other adjustments R1054, R1056, R1061, and R1063, are part of a shaper network. The network compensates for magnetic saturation in the Preselector, which would cause a deviation from linearity at frequencies above 14 GHz. Each shaper network is switched in by a resistive divider that, at a given frequency, provides forward-bias to the diode in the shaper to shape the current output.

The front panel MANUAL PEAK control applies a small offset through R5065 to the input of the current driver stage. This corrects for non-linearity or temperature drift in the 1st LO and Preselector.

Current Driver

This stage consists of the output stage Q565/Q5052; FETs Q3061, Q3077, and Q2074; amplifiers U2054 and U3054; and transistor Q4037. When the Preselector is not in use, DB2 goes low and turns Q2074 off to reduce the coil current to zero.

Preamplifier U2054 reduces the temperature drift of the output stage. Driver Offset adjustment, R2066 nulls the offset voltage (at which point the temperature drift is least). U2054 drives amplifier U3054. Q3061 isolates U3054 from the output driver Q5052/Q565.

Current amplifier Q5052 drives the main preselector driver transistor, Q565. The stage is biased so the current divides, with most of the current going through the output transistor, and a lesser portion through the bias circuits. The currents rejoin at the Preselector coil. One set of terminals for R4049 carries the coil current, the other set senses the voltage.

When DB5 line goes low, the Preselector is not swept, Q4037 and Q3077 turn on, which adds C4071 across the Preselector coil to reduce noise at the output.

Preselector Switch Driver

Operational amplifier U1011B and the complementary pair of transistors Q4025/Q3025, form the preselector switch driver. This circuit drives the filter select relay as is shown on Diagram 12. This relay requires a positive pulse to select the Low-pass Filter and a negative pulse to select the Preselector.

When DB4 line (Q5 of U5031) goes high, a positive pulse of about 100 ms in duration, generated through RC network C3021/R3021, is applied to the input of U1011B. The output of the operational amplifier drops to about -12 V and a positive pulse is passed through the transistor pair, selecting the Low-pass Filter. When the DB5 line goes low, a negative pulse of the same duration is passed to U1011B. The amplifier output rises to about +12 V and a negative pulse is passed through the transistor pair to select the Preselector.

When the circuit is quiescent neither Q3025 nor Q4025 conduct, since the sum of the zener voltages of VR3011 and VR3012 is greater than the combined supply voltages. When the output of the operational amplifier comes near one of the supply voltages, the transistor, that is connected to the other supply, becomes saturated, and supplies the drive current to actuate the relay coil. CR4012 and CR4013 protect the driver transistors from induced voltage surges and C3028 and R3028 dampen oscillation that occur in the coil.

CENTER FREQUENCY CONTROL

Refer to the block diagram adjacent to Diagram 35 as well as the schematic. The Center Frequency Control converts digital information, from the front panel FREQUENCY control or on the GPIB bus, via the microcomputer, to analog voltages for the 1st LO Driver and Preselector Driver.

These in turn control the center frequency of the analyzer. The Center Frequency Control board contains the following major circuits:

1. The Digital Control circuit, which buffers and decodes the addresses and other data to control the other circuits.
2. The coarse and fine storage registers (latches), which store the numerical bytes that control the DAC (digital-to-analog converter) stages.
3. The coarse and fine DAC stages, which convert the digital inputs from the storage registers into analog current and voltage equivalent values.
4. The coarse and fine track/hold amplifiers, which store the analog output values during the approximation routine and compare the stored value to the approximated value for the microcomputer.
5. The write-back circuits, which inform the microcomputer when the stored value and the approximated values are equal.

Operating Modes

An explanation of circuit design principles is given before the operation of the circuit is described. Although DAC IC's can now furnish high resolution, two DAC IC's are used in tandem to get the required resolution for the 494/494P. This method, however, can cause errors and non-monotonic behavior in the overall converter circuit. To circumvent this problem, the outputs of the tandem DAC units are summed together so that the two units are overlapped by three bits (that is, the MSB of the low-order DAC is weighted equally with the third least significant bit, or $2E-10$ bit of the high order DAC). The overlap means that the lower DAC will have sufficient range to monotonically tune the output of the converter over the entire range of the analyzer, but only if the proper codes of the lower DAC device can be found. Now, suppose that the tandem DAC is loaded as follows:

```
Upper order:  1 0 0 0 0 0 0 0 0 0 0
Lower order:      1 1 1 1 1 1 1 1 1 1 1
```

The contents of the devices are shown overlapped to illustrate the bit weighting. Now assume that the low-order device is to be incremented one bit. The MSB of the low-order device must be moved into the high-order device before the low-order device can be incremented. Thus, the two must appear as follows:

```
High-order:  1 0 0 0 0 0 0 0 0 0 0
Low order:      1 1 1 1 1 1 1 1 1 1 1
```

If the high-order device operated with no overall linearity inaccuracy, the operation would now be complete and the low-order incrementation could occur. However, the DAC device can vary by one LSB of the correct value. Figure 7-25 illustrates a graph of the best and worst case output. Note, that even in the worst case, the output may move only once every two or three state changes, but the output is always monotonic and within one LSB of the correct value.

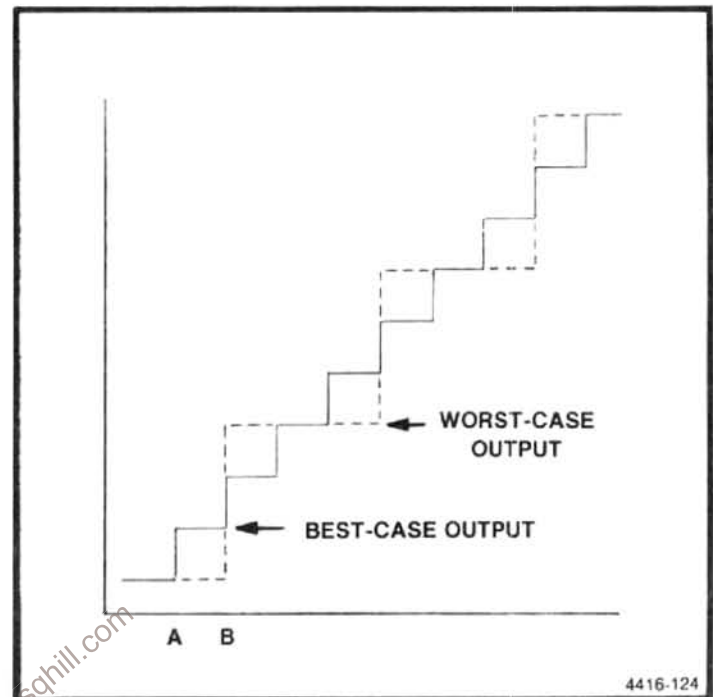


Figure 7-25. DAC variance graph.

If, in the example shown previously, the high-order device is at point A in Figure 7-25, incrementing the device to point B has no effect on the output. If the MSB of the low-order device is set to zero, as shown in the first example, the combined output will actually decrease. Ordinarily, the Center Frequency Control circuit can increment and decrement whenever the microcomputer commands without going through a special routine. However, as just described, some microcomputer adjustment is necessary to compensate for the disparity that usually occurs between the low-order and high-order DAC units.

The first operating mode is the tracking mode, where the preamplifier and integrator are connected together by the disconnect stage, and the entire unit acts as an operational amplifier. Figure 7-26 illustrates the basic circuit. While the circuit operates in this mode, the amplifier tracks the DAC stage and sends the voltage out to the tuning circuits.

When the transfer of bits from the lower to the upper DAC is required, the microcomputer commands the circuit

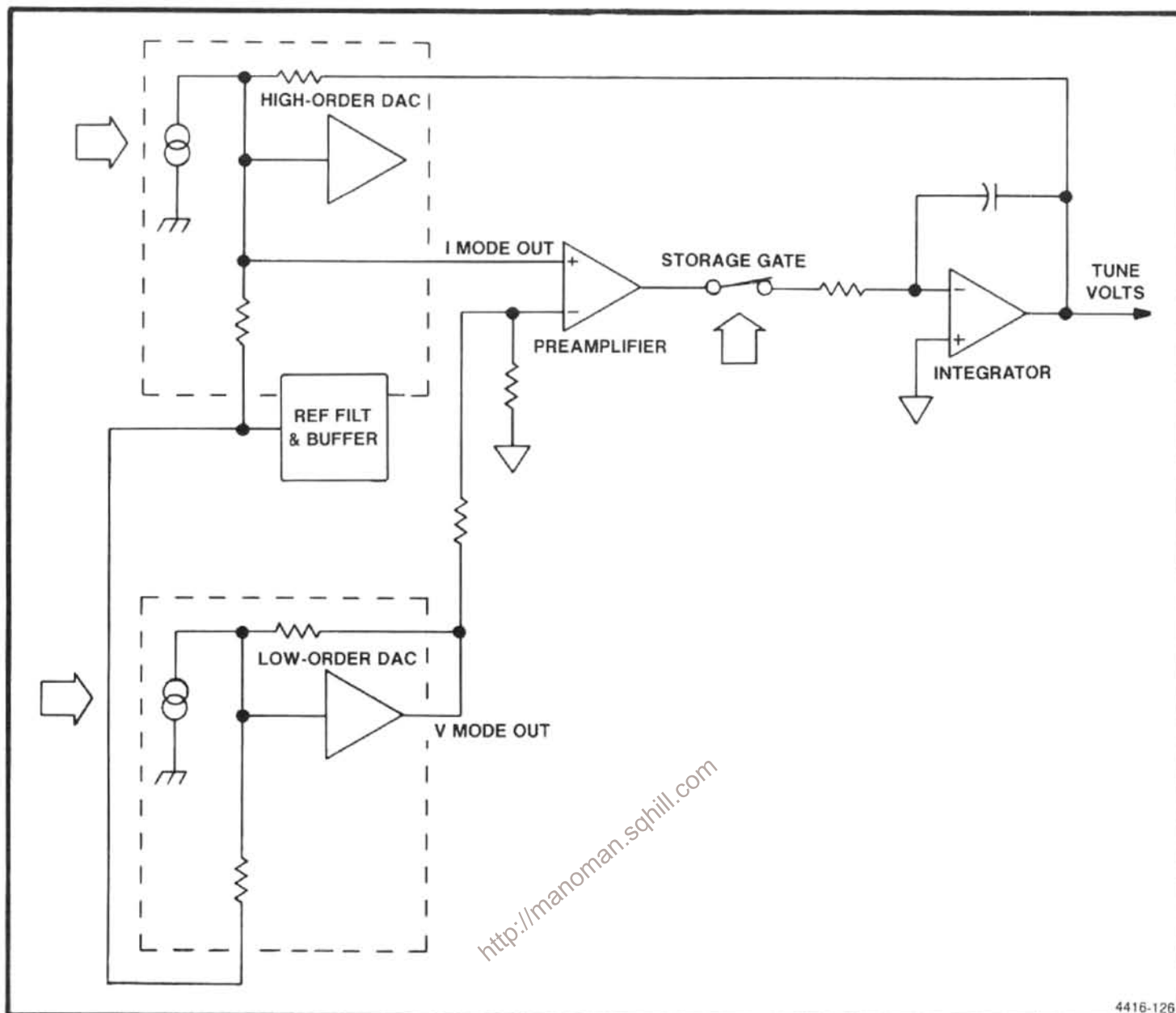


Figure 7-26. Simplified tune voltage converter.

to shift to the hold mode. The command comes through the decoder to shut off the disconnect stage, and the preamplifier output is disconnected from the integrator. The integrator holds the voltage that was previously at the output for comparison, and the approximation cycle begins.

The microcomputer resets the low-order DAC to zero. Then, the highest order bit in the low-order DAC is set to one, and the circuit is queried to find if the DAC output and integrator output is greater or less than required. If less, the microcomputer loads the next lower bit in addition and queries the circuit once more. This process goes on until the two values are the same. Had the microcomputer found that the DAC output was greater than the integrator output at the first inquiry, it would have set the highest order bit to

zero and loaded the second-order bit into the low-order DAC, then continued to load successively lower order bits, one at a time, until the circuit signalled that the comparison had reversed. By this process, which is known as the successive approximation method, the circuit finally reaches the point where the outputs are equal, and the microcomputer commands the circuit to shift back to the track mode.

Digital Control

The digital control circuits consist of buffer U2016, address decoder U2014, steering register U2022, and the steering gates (U2024A, U2024B, U2024D, U2026A, U2026B, and U2026C). Because of the quantity of data that

must pass through these circuits, a steering register is used that has a separate address. The first byte of data, which is the steering byte, is clocked into U2022 by ADDRESS 70. The output levels are applied to the steering gates, and the circuit waits for the next byte. The microcomputer then furnishes the first byte of data to be sent to low-order, fine-tune, digital-to-analog converter (DAC); for example, via storage register U3022. The byte is clocked into the register by the coincidence of low states at the inputs of U2026C; one from the steering byte and the other from the ADDRESS 71 signal, which is used to clock the steered data bytes into the correct register. This continues until seven bytes of data have been clocked into the circuits, including the steering bytes. The third output from U2014, ADDRESS 80, controls transistors Q2043 and Q1039, which enable the write-back function.

In addition to the six steering lines, that drive the steering gates, U2022 also controls, by means of the TRACKf and TRACKc lines, the hold/track selector transistor for each converter side. Table 7-19 illustrates the format for ADDRESS 70. Addresses are expressed as hexadecimal numbers. Table 7-20 lists some of the significant states that are used to tune the DAC.

Table 7-19
ADDRESS 70 FORMATS

DB0	Fine Tune low byte enable
DB1	Fine Tune mid byte enable
DB2	Fine Tune high byte enable
DB3	Fine Tune hold
DB4	Coarse Tune low byte enable
DB5	Coarse Tune mid byte enable
DB6	Coarse Tune high byte enable
DB7	Coarse Tune hold

Storage Registers. Six storage registers are used in the circuit (U1014, U1016, U1022, U3014, U3016, and U3022 respectively). Since both sets are identical, only the first three are described.

Data from U2016, the data buffer, is clocked into the registers each time a different tune voltage is required. U1022 feeds the lowest eight bits to the low-order DAC, U1020; U1014 feeds the highest eight bits of the high-order DAC, U1026; and U1016 feeds the remaining bits to both units.

Digital-To-Analog Converters. Each side of the converter has two DAC stages contained on sub-assemblies A46A1 DAC 1200 Interface and A46A3 DAC 1200 Interface. These sub assemblies plug into the Center Frequency Control board, A46, through IC sockets J1024 and J1030, for the Coarse Tune circuit, and J3024 and J3030, for the Fine Tune circuit. Since both sets operate the same, only Coarse Tune units are described. Each DAC furnishes current or voltage outputs that are commensurate to the data applied. Figure 7-26 is a functional block diagram of each DAC, illustrating its operation in the circuit. U1020 is the low-order DAC, U1026 is the high-order DAC. U1012 and Q1018 and the associated circuitry are used to filter and buffer the +10 V Ref output of the high order DAC to provide the V Ref in voltage for both DAC's.

The DAC unit is basically a programmable current generator that drives an internal high quality operational amplifier. In this configuration, only the low-order DAC uses the internal operational amplifier. Thus, the low-order unit operates in the voltage output mode, and the high-order unit operates in the current output mode. The two devices feed the two inputs of preamplifier U1044, which sums the two inputs, amplifies the sum, and sends it through the switching circuit to the integrator.

Table 7-20
DAC TUNING CODES

Tuning Point	Data	Address	Results
Positive full-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DAC's.
Mid-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DAC's
	33	70	Enables high byte latch, track mode
	80	71	Loads 80 into DAC's. Midrange value
Negative-full-range	00	70	Enables all latches, track mode
	FF	71	Loads FF into all positions of both DAC's

Since the DAC units generate the dc voltage that tunes the entire instrument, noise and extraneous signals must be kept at a minimum. Thus, each tune voltage is provided with an isolated ground system, U1042A/U1042B for the Coarse Tune voltage converter, and U3041A/U3041B for the Fine Tune voltage converter.

Track/Hold Amplifiers

Since the coarse and fine amplifiers are identical in operation, only the coarse amplifier is described here. The amplifier consists of preamplifier U1044, control transistor Q2044, storage gate FET Q2046, and integrator amplifier U2046.

The output of the low-order DAC (U1020) is fed through input resistor R1048 to the inverting input of preamplifier U1044. The current output of the high-order DAC U1026, is fed directly into the non-inverting input of the preamplifier. Feedback resistor R1044 establishes the gain of the stage at about 10,000 (ratio of R1044 to R1046). The combination of CR1046, CR1045, and R1047 in the feedback circuit, prevents the output from swinging to extreme voltages with large input signals. Thus, whenever the output exceeds about one volt in either direction, one of the diodes conducts and connects R1047 and R1045 across the feedback path to reduce the gain of the stage to about unity.

The output signal from the preamplifier is connected to the source of storage gate FET Q2046. The gate of this device is controlled by transistor Q2044. Normally the circuit is tracking, so TRACKc line (Q8 of U2022) is low and Q2044 is conducting. CR2042 is cut off since the voltage drop across R2043 holds the gate of Q2046 at about 0.3 V. (The 0.3 V back bias on the source-gate junction reduces memory slewing while switching modes.) Q2044 holds the diode back-biased as long as the transistor continues to conduct. This permits Q2046 to pass the signal from the preamplifier output to the integrator input.

Integrator U2046 tracks the preamplifier output during track mode and serves as the inverting amplifier for the feedback system shown in Figure 7-26. Under normal circumstances the incoming signal is routed through R2046. To improve the amplifier's slewing rate, CR2044 and CR2045 conduct to connect R2047 in parallel with R2046 when signals in excess of one volt are applied. This speeds up the response of the circuit when large scale tuning changes are required.

When the hold mode is selected, the TRACKc line (Q8 of U2022) moves high, Q2044 cuts off and CR2044 pulls the gate of Q2046 low enough to cut off the FET. This disconnects the preamplifier from the integrator which then maintains the charge on C2046 during the approximation routine. COARSE TUNE RANGE adjustment R1032 is connected across pins 16 and 18 of U1030. It compensates for the different resistance values inside the DAC. This variation is more serious in the higher-order DAC owing to its greater effect on the output.

Write-Back Circuits

These circuits consist of amplifier U2044 and U3045, plus enabling transistors Q1039 and Q2043. Since both are identical, only the coarse circuit is described.

Following the command to shift to the hold mode, the microcomputer will interrogate the circuit to see if the DAC output and the stored voltage match. It does this by pulling ADRS 80 low. This turns Q1039 off, which enables U2044. The output of U1044 is at zero volts when its two input voltages match. If the loop error voltage is high, U2044 will pull down on DB7 line, and if the loop error voltage is low U2044 will allow DB7 to go high. This informs the microcomputer whether the bit just set is too large or too small. The output of U2044 is open collector, so it has no effect on the data line when it is not disabled.

COUNTER AND PHASE LOCK SECTION

FUNCTIONAL DESCRIPTION



This section of the 494/494P consists of a Counter, Phase Lock assembly, Phase Gate, Harmonic Mixer, and Auxiliary Synthesizer. The Counter, Harmonic Mixer, and Auxiliary Synthesizer, comprise the nucleus of the frequency control hardware for the instrument. Both the 1st LO and 2nd LO frequencies are controlled via a firmware based control loop that uses data from the Counter as feedback to control oscillator frequency. The 10 MHz IF is also counted to accurately calculate signal frequency.

The Phase Lock assembly stabilizes the 1st LO frequency. It consists of an outer and inner loop. The inner loop uses the subharmonic of the 100 MHz reference frequency, from the 3rd Converter, to mix with the output from a 25.032 to 25.095 VCO and compares this IF difference with a $\div N$ number (between 32 and 94 kHz) set by the processor. Any deviation is detected by a phase/frequency detector whose output error voltage is used to pull the VCO frequency and phase into lock with the inner loop reference. The outer loop consists of the inner loop, a Strobe Driver, Phase Gate Detector, Error Amplifier, and the 1st LO. The frequency of the inner loop VCO is divided down and applied as a strobe pulse to the Phase Gate Detector. This strobe pulse generates a spectra of equally spaced line spectra across the spectrum. One of these lines will be within 2.5 MHz of the 1st LO frequency (the other input to the Phase Gate Detector). The Phase Gate Detector outputs an error signal that is proportional to the difference between the nearest strobe and the 1st LO frequency. This error signal is amplified and filtered by the Error Amplifier and applied to the FM coil of the 1st LO to pull it into frequency and phase lock with the strobe.

The Harmonic Mixer mixes the 1st LO frequency and a harmonic of a synthesized 200-220 MHz signal from the Auxiliary Synthesizer. The exact frequency of the signal from the synthesizer is a function of the $\div N$ factor from the processor. The output of the Harmonic Mixer is a signal within the 10 to 80 MHz range. This signal is divided down in the Auxiliary Synthesizer and sent to the Counter. The microcomputer looks at the resultant count and determines which direction to move the 1st LO to bring it to frequency.

Phase Lock Assembly

As previously stated, the phase lock system consists of two frequency servo loops, called the outer loop and inner loop. In the inner loop operation, the 100 MHz reference signal from the 3rd Converter, is divided down to 25 MHz, on the Synthesizer board, and applied as the reference sig-

nal to the mixer on the Offset Mixer board. The 25 MHz signal is also applied as a clock signal to $\div N$ counter circuits, on the Synthesizer board, which output a frequency (depending on the $\div N$ number from the processor) between 32 kHz and 94 kHz. This signal is applied to the phase/frequency detector on the Offset Mixer board, where it is compared to the IF output (difference between the 25 MHz reference and the output from the VCO (voltage controlled oscillator) and any difference is output as an error voltage to the Error Amplifier.

The VCO operates between 25.032 MHz and 25.094 MHz, depending on the drive from the Error Amplifier. This signal is applied to the RF input of the mixer on the Offset Mixer board, where it mixes with the 25 MHz reference frequency. The difference frequency, which is between 32 kHz and 94 kHz, is applied to the phase/frequency detector and compared to the $\div N$ frequency. If the two signals are edge and frequency coincident, phase lock occurs. If they do not coincide, an error signal is generated, passed through the Error Amplifier, and applied to the VCO to shift the oscillator frequency until it is phase locked. This evolution typically lasts for only a few milliseconds, so the inner loop phase lock is, for all practical purposes, instantaneous.

The outer loop, which includes the inner loop circuits (Offset Mixer, Error Amplifier, and VCO) consists of the Strobe Driver, Phase Gate, Error Amplifier, and 1st LO. (The Harmonic Mixer, Auxiliary Synthesizer, and Counter, are a part of the operation, but are not considered a part of the loop.)

The signal between 25.032 MHz and 25.094 MHz from the VCO is applied to the Strobe Driver where it is divided by five, filtered, and sent to the Phase Gate Detector as a strobe signal between 5.006 MHz and 5.019 MHz. This strobe generates line spectra that are equally spaced approximately 5 MHz over the spectrum. At about the 400th line, which corresponds to approximately 2 GHz, assuming that the 1st LO is tuned to a frequency near 2 GHz, one of these lines (at about the 400th line) will be within 2.5 MHz of the 1st LO frequency. The Phase Gate Detector will then output an error signal that is proportional to the difference between the 1st LO frequency and that of the nearest strobe line, if that difference frequency is less than approximately 1 MHz.

For phase-lock acquisition, the microcomputer calculates the strobe frequency required for the desired 1st LO frequency. The strobe is set to this frequency and the 1st LO is set to the required harmonic of the strobe. The outer loop is

closed, and the microcomputer tunes the 1st LO frequency through the following sequence: up 750 kHz, down 1.5 MHz, up 1.5 MHz, and down 750 kHz. During one of these "firmware searches" the 1st LO frequency passes through the strobe harmonic frequency and the loop acquires lock.

Any frequency difference between the strobe signal and the 1st LO will generate a low frequency correction voltage. This correction voltage is filtered by the F(s) amplifier, then used to drive the oscillator FM coil to pull the oscillator frequency back to the strobe position. If the 1st LO drifts beyond the error voltage range of the F(s) amplifier, comparators on the Error Amplifier board, that monitor the error voltage, will interrupt the microcomputer and indicate the direction of drift. The microcomputer then tunes the Center Frequency Control circuits to null out any FM coil current in the phase lock loop.

Frequency Control

The 21-bit counter and its associated control circuitry, on the Counter board, plus the Harmonic Mixer and Auxiliary Synthesizer, comprise the frequency control hardware nucleus for the 494/494P. A firmware-based control loop, that uses data from the counter as feedback on the oscillator frequency, controls both the 1st LO and the 2nd LO frequencies. The 10 MHz IF is also counted by the Counter to determine the input signal frequency to the analyzer.

A mix down counting scheme is used to count the 1st LO frequency, which varies between 2 GHz and 6 GHz. The 200-220 MHz output from the Auxiliary Synthesizer is positioned so one of the signal harmonics is approximately 45 MHz above the 1st LO frequency. This output drives the LO input to the Harmonic Mixer, the 1st LO drives the RF input. One of the IF outputs from the Harmonic Mixer is within the 10 to 80 MHz range (approximately 45 MHz). This IF signal is passed through a 10-80 MHz band-pass filter, divided by 100, then counted by the Counter. Since the Processor knows the Synthesizer frequency, the 1st LO frequency can be calculated if the Processor knows which harmonic of the Synthesizer frequency was used to generate the IF frequency being counted. The harmonic of the Synthesizer frequency is calculated from the 1st LO tuning DAC (digital-to-analog converter) code, since it indicates the 1st LO frequency to within approximately ± 10 MHz.

Counting the 2nd LO frequency is much simpler. The controllable 16-20 MHz VCO in the 2nd LO assembly determines the frequency of the 2nd LO; therefore, the 2nd LO frequency is calculated by directly counting the 16-20 MHz signal. The 2nd LO frequency is then calculated from this frequency.

Controlling the Oscillator Frequency—The frequency control loop is only closed between sweeps. After the completion of each sweep, the processor switches the span/div to zero and then counts the 1st LO and the 2nd LO frequencies. If they are not at the frequency required to generate the displayed center frequency, they are set to the correct frequency by repeating the process (i.e., the DACs are changed to tune the LO, the LO is counted, etc.).

In the single sweep mode, the oscillator frequencies are corrected after each single-sweep actuation, and before the sweep starts. In the manual sweep mode, or other non-recurring sweeps, the oscillators are corrected at periodic intervals.

Counting the IF—In addition to counting the frequency of the 1st and 2nd LO, the 10 MHz IF is counted when the Counter mode is actuated; thus, the incoming signal frequency can be calculated from the frequency conversion equation for the analyzer. The 1st LO is actually phase locked before the 2nd LO and IF are counted, in order to reduce FMing in the IF signal. This allows very accurate signal counting, even in wide spans.

HARMONIC MIXER



The Harmonic Mixer combines a portion of the 2-6 GHz 1st LO signal with harmonics of the 200-220 MHz reference signal from the Auxiliary Synthesizer to provide an output signal in the 10-80 MHz range. This signal is amplified and returned to the Auxiliary Synthesizer where it is counted to get an exact computation of the oscillator frequency. The Harmonic Mixer consists of a directional coupler, an input amplifier, the mixer, and an output amplifier, all on a hybrid alumina circuit. Figure 7-27 shows a functional block diagram of the Harmonic Mixer.

Input signal level, from the 1st LO to directional coupler A25A1, is about +10 dBm. The coupling ratio is 10 dB, therefore, the coupler will deliver about 1 mW (0 dBm) to the RF input of the harmonic mixer. The through-port contributes about 0.5 dB of loss for the 2-6 GHz signal.

The 200-220 MHz reference signal, at a level of about 10 mW from the Auxiliary Synthesizer, is amplified to a level of about 100 mW (+20 dBm) by a differential amplifier Q1 and Q2. Resistor R27 couples the emitters together and the current is set by R13 and R14. Output is transformer coupled to the input of the mixer. Input signal level to the amplifier is +7 dBm minimum.

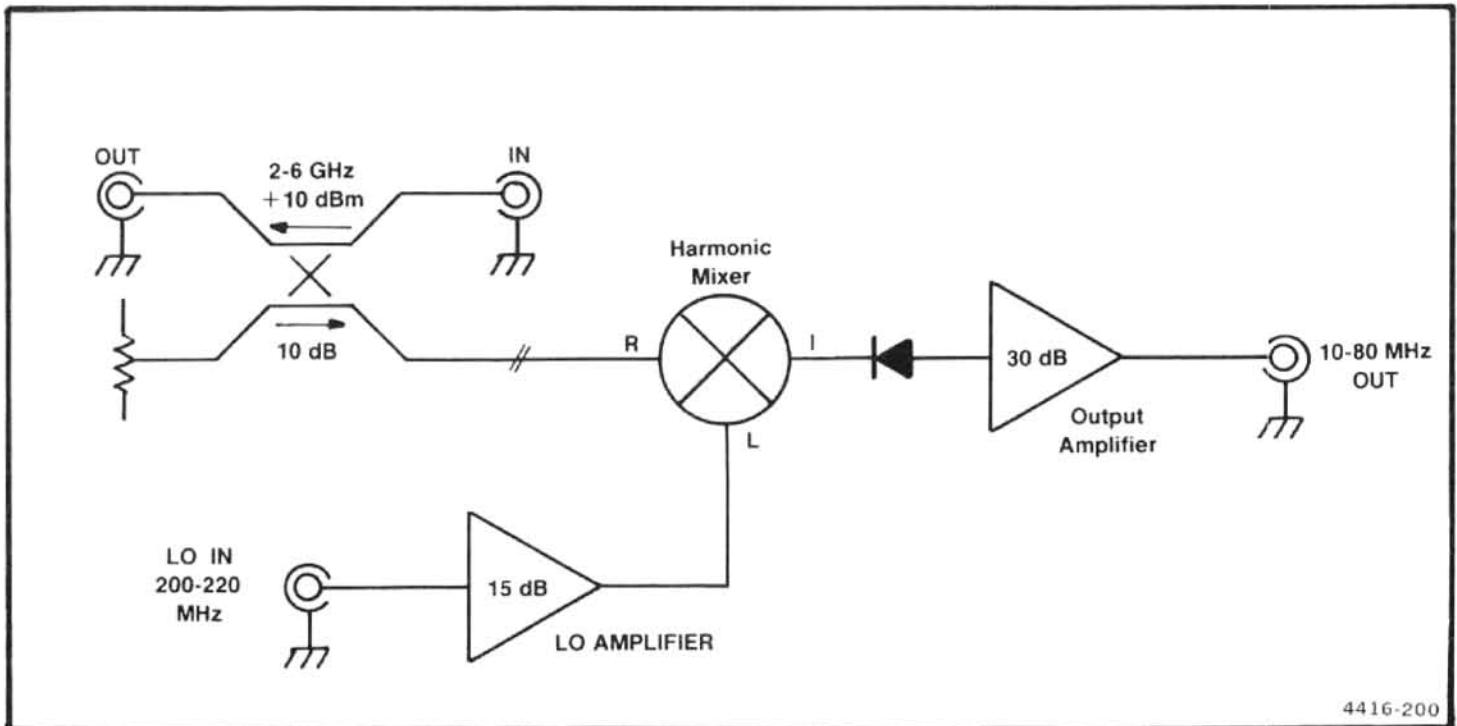


Figure 7-27. Simplified schematic of harmonic mixer.

Two additional directional couplers are used to couple the 2-6 GHz signal into the mixer circuit. A power splitter (R1, R2, R3) splits the signal into two paths. Each signal (approximately -6 dBm each) is then coupled through these couplers to the mixer. The through ports are terminated in $50\ \Omega$. Thus the 2-6 GHz signal is coupled into the mixer differentially at a power level of about -16 dBm.

The 200-220 MHz reference signal is also coupled differentially into the mixer circuit, since the output of transformer T1 is applied across the two terminating resistors R4 and R5. The level of this signal is high enough to drive the snap-off diode into its operational region. Harmonics of this 200-220 MHz signal mix with the 2-6 GHz signal to generate numerous IF products which are detected by diodes CR2 and CR3 and fed to the output amplifier.

The output amplifier is a two stage common-emitter cascade amplifier with dc coupling between stages. The standing current through the second stage (Q4) is higher than in the first stage (Q3) to provide better power and IM performance. The amplifier is designed for a 10 to 80 MHz response. Signals above 80 MHz are rejected by a low-pass filter in the Auxiliary Synthesizer. Output level of signals in the 10-80 MHz range is typically -20 dBm for input signal levels as described.

AUXILIARY SYNTHESIZER



The Auxiliary Synthesizer is part of the Direct Frequency Readout (DFR) system for the 494. This, along with a harmonic mixer, counter circuits, supporting filters and amplifiers, and appropriate firmware, make up the DFR or integrated microwave counter. The DFR provides the means for measuring and determining the frequency of all oscillators and the center of the IF, so the center screen frequency is always known. Since the IF signal can be counted, this allows direct frequency measurement of any signal applied to the input port of the 494.

A functional block diagram of a simple or basic synthesizer is shown in Figure 7-28. The VCO frequency is divided by "N" in a programmable down-counter which outputs a pulse every Nth input pulse. This frequency along with a frequency reference is then fed to a phase/frequency detector. The difference between the two signals is filtered and fed back as a control voltage to the VCO to phaselock the oscillator to the reference. The VCO frequency is related to the reference by, $F_{\text{ref}} = NF_{\text{ref}}$. As N is changed the VCO frequency will change by F_{ref} for each step in N. This produces outputs separated by F_{ref} . To get closely spaced channels, in tuning the VCO, the reference frequency must be relatively low.

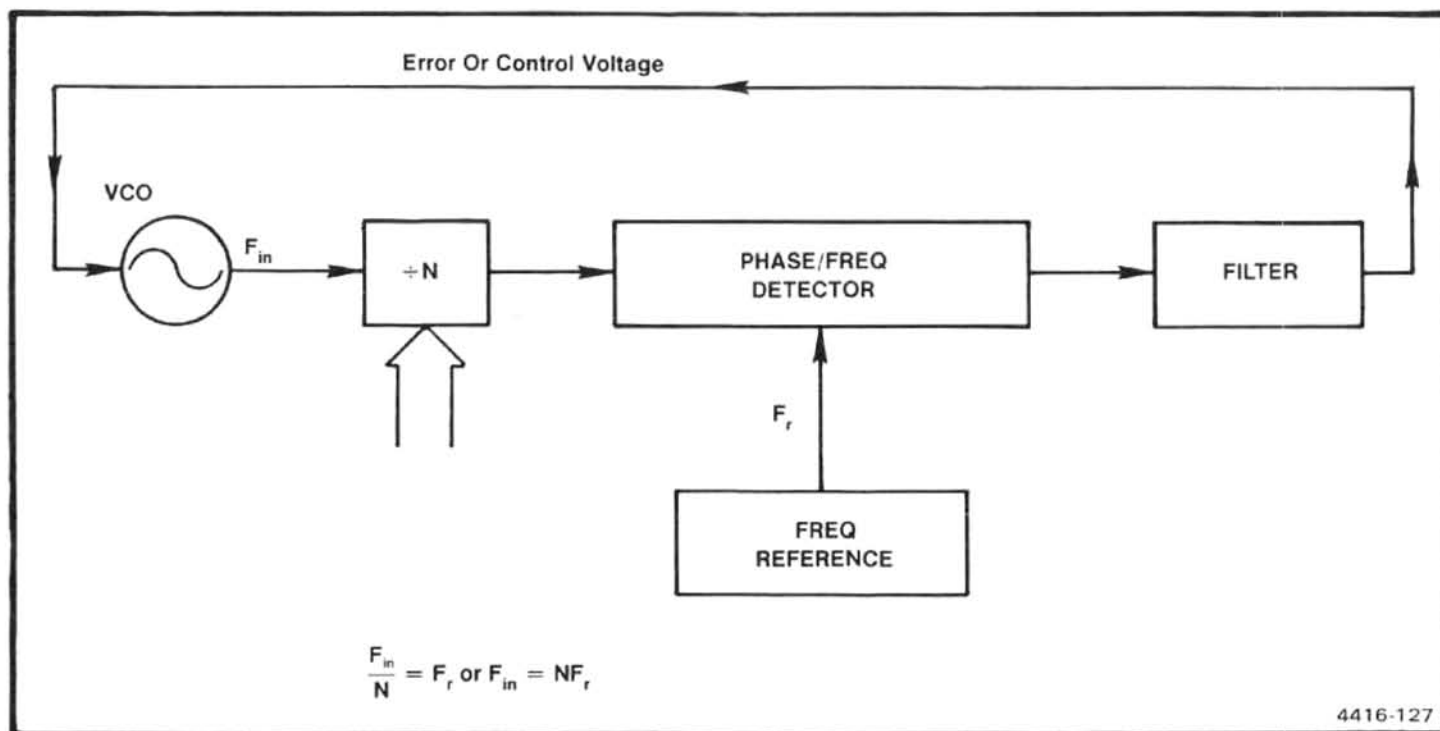


Figure 7-28. Block diagram of a basic synthesizer.

The synthesizer in the 494 uses a variable modulus prescaler to divide the frequency of the VCO down before is processed by the “ $\div N$ ” counter, such as shown in Figure 7-29. The variable modulus prescaler is controlled by a modulus control input. When the line is high the prescaler is a divide by $P + 1$ and when the line is low the division changes to P . A common type of prescaler is a divide by 10/11. A cycle of system operation starts with all programmable counters loaded and ready to count. The variable modulus prescaler initially divides by $P + 1$.

Two programmable dividers are used with this system, both triggered by the output of the prescaler. One is a $\div N$, with N being a relatively large number, the other is a “ $\div A$ ”, where A is a small number. One possible state includes $A = 0$.

The operation of this system is as follows: The lower case letters represent variables, the upper case letters represent the programmed values. At the beginning of the cycle, $p = P + 1$, $a = A$, and $n = N$. After $P + 1$ pulses from the VCO, one pulse is applied to the “ a ” and “ n ” counters and “ a ” and “ n ” decrease by 1 ($a = A - 1, n = N - 1$) This continues until $a = 0$ at which time the modulus control line changes state and $p = P$ while $n = N - A$. The counting continues until $n = 0$. Both the “ n ” and “ a ” counters now return to the programmed condition. The total number of pulses applied from the VCO is:

$$N_{total} = (P + 1)A + P(N - A) = A + PN$$

Both N and A are programmable so; $F_{vco} = (A + PN)F_{ref}$. This leads to a possible channel spacing of F_{ref} , obtained by changing A by 1.

A functional block diagram of the Auxiliary Synthesizer is shown adjacent to the schematic in the diagrams section. The VCO (Q2071) is configured in a Colpitts oscillator circuit with the inductance as a three turn air core coil with feedback provided by C2072 and C2071. Coarse tuning is accomplished with C1070, while the voltage control of the frequency comes from the varactor diode, CR2068. This diode provides a frequency shift of over 30 MHz from a voltage swing of +5 to +11 V, which is ample overlap for the 20 MHz tuning range. The output power of the oscillator is 0 dBm into 50 Ω . The oscillator is biased so it can be turned off and on rapidly.

The VCO is turned off by turning Q2076 on. In operation, the synthesizer is turned off during periods when information is presented on the crt. Synthesis and counting is done during retrace time to prevent possible interference on the display from any radiated energy from the synthesizer.

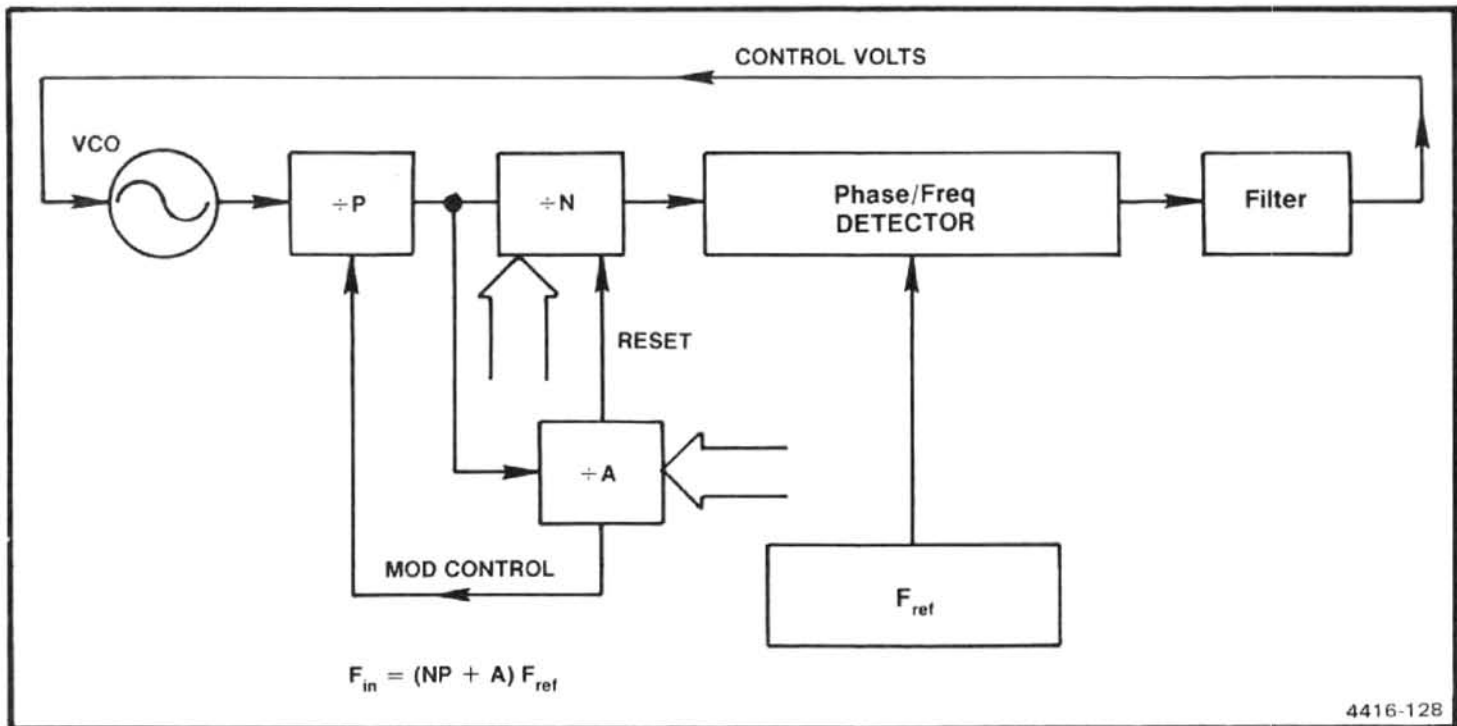


Figure 7-29. Basic block diagram of a $\div N$ synthesizer with a variable modulus prescaler.

The VCO output is split by a resistive power divider. One output drives transistor U2058, which provides +7 dBm of signal output to the Harmonic Mixer. This device is biased to a 20 mA collector current by transistor Q2055.

The other VCO output drives a low gain amplifier, Q2049, which is biased by transistor Q2051. Negative feedback, in the form of emitter degeneration and shunt current feedback, sets and stabilizes the gain to ensure stability with regards to spurious oscillations. The output of Q2049, to drive the variable modulus prescaler is 0 dBm. The variable modulus prescaler U3051, is a $\div 32/33$ IC that features an ECL input with a TTL or CMOS compatible output.

The major circuit of the synthesizer is U4041, a Motorola MC-145146. This IC is a large scale integration CMOS device intended for frequency synthesis applications with a variable modulus prescaler. U4041 contains three programmable counters; a $\div N$, a modulus control counter $\div A$, and a reference divider which divides an input from a crystal controlled source or other reference frequency down to a desired frequency. This CMOS device has a speed comparable to TTL. It also contains a phase-frequency detector which drives an external loop filter that uses an operational amplifier. U4041 will accept data for N, A, and R inputs from a 4-bit data bus while a 3-bit address bus selects the information to be loaded. Data contained on instrument bus lines DB4 to DB7 is loaded when the enable line goes high. Address information is contained on instrument bus lines DB0, DB1, and DB2. The appropriate 32 latches are also contained within this IC.

The output from the phase/frequency detector in U4041 is a chain of pulse signals at the reference frequency. The pulses contain both ac and dc components. The ac part of the signal causes reference sidebands to appear on the VCO output. These sidebands are suppressed by two active loop filters consisting of U2040A and U2040B. The outputs (0_{Ref} and 0_{Var}) from the detector, which are similar but with reversed polarity, are applied differentially to the input of U2040A. Slight differences in pulse width between the two outputs generate a dc voltage which is further filtered, to suppress frequencies above 20 kHz, by an active low-pass filter (U2040B) before it is applied to the varactor diode CR2068 in the 200-220 MHz VCO.

U2040A is an integrator with a series resistor added to the feedback capacitor. This controls the slope of the loop gain at gain crossover. To provide additional suppression of the reference sidebands, an RC active two pole filter, U2040B, is added. Cutoff frequency is about 20 kHz. The loop filter (U2040A) and the VCO provide the dominant poles that determine the system response. A damping factor near unity provides the stability. Additional filtering in the form of passive components, with a high frequency cutoff, are added between the output of U2038B and the varactor diode CR2068. CR1065 provides a clamp to prevent a control line voltage less than 5 V. Capacitor C1070 sets the low end of the control voltage to about 6 V. Range of the control voltage, over the 200-220 MHz VCO range, is about +6 to +11 V.

The off/on status of the VCO is controlled by U4074 which is activated by D3 from the data bus. The value is latched in U4074 and its output turns Q2076 off or on. The output also controls the sensitivity of divider U5015. During the period when the VCO is off and there is no input signal, the divider sensitivity is lowered so stray signals will not activate the divider. This is done by turning Q5027 on and pulling input pin 6 of U5015 low.

The 100 MHz signal from the 3rd converter is applied through a resistive power splitter to divider U2017 and to buffer amplifier Q1015. The 1 MHz output from the divider, U2017, is further divided by 5 within the synthesizer IC, to become the 200 kHz reference frequency for the synthesizer. The amplifier Q1015 has negative feedback for gain stabilization. Its output signal is applied to the counter board.

The 10-80 MHz signal from the harmonic mixer is passed through a 7-pole low-pass filter with 80 MHz cutoff. The signal is then amplified by U4021 with a broad band gain of about 24 dB.

COUNTER BOARD



The Counter board circuits and function are: 1) The address decoder which receives and decodes the talk and listen commands for the microcomputer. 2) The service request circuits that sense an impending loss of 1st LO phase lock and sends a service request to the microcomputer. it then cancels the request when directed by the microcomputer. 3) The data buffers transmit data to and from the microcomputer. 4) The input amplifiers and multiplexer amplify input signals up to TTL levels and then select which of the input signals is to be counted. 5) The $\div 2^n$ counter divides the selected input signal by some power of 2 as determined by the microcomputer. 6) The 21-bit counter counts at a 100 MHz rate for a given number of cycles of the selected input signal.

Address Decoder

The addresses from the microcomputer are decoded by address decoder U2040. The counter circuits have both a talk address, where the counter-buffer circuits are instructed to talk on the data bus, and a listen address, where U3024 is directed to receive data from the data bus. The talk address is F3; the listen address is 73.

Service Request Circuits

The service request circuits consist of multiplexer U3040, latch U3048B, and associated circuitry. This circuitry alerts the microcomputer in the event that the 1st LO has drifted too far. The UP and DOWN signals from the window com-

parator (located on the Error Amplifier board) drive NOR gate U3010C. Both signals are also sent to U3034, where their status can be read by the microcomputer. When one of these signals is high, it indicates that the Error Amplifier is approaching its operating limits and the microcomputer should adjust the 1st LO frequency so the Error Amplifier returns to the center of its range. A high at either input of U3010C produces a negative transition that is inverted by U3046C. C2050 pulls the set input of U3048B high for approximately 10 μ s. The Q output of U3048B then goes high, causing Q4052 to pull the SR (service request) line low.

The \bar{Q} output of U3048B pulls the $\bar{G1}$ and $\bar{G2}$ inputs of multiplexer U3040 low, enabling both sides. This device allows Q4034 and U3048B to respond to inquiries by the microcomputer to determine which address requested service. The microcomputer initiates the polling routine, which is to pull the POLL signal and AB7 high, then interrogate each data bus line in succession to determine which address requested service; i.e., which data line is low. To do this, the Y1 output of U3040 is set high, which causes Q4034 to pull the D2 line low. To affirm which address requested service, the microcomputer now causes the 7 address line to move low, which, via the Y2 line from U3040, clocks U3048B to the reset state as the microcomputer holds data bus line 2 low. This cancels the service request because it cuts off Q4052 permits its output to move high. In addition, the complement output of U3048B moves high, which disables the inputs to U3040. This brings the service request circuitry back to its original state.

Data Buffers

The data buffers consist of U3024, U3034, U3030, and U2026. U3024 is the listen buffer. When address decoder U2040 is addressed by the microcomputer to listen,, it enables U3024, which passes on the buffered data to the other circuits in the Counter board. The function of each data bit is as follows.

D0—This line carries the serial data that selects which input signal is to be counted and what n numbers to use in the $\div 2^n$ counter. This data is loaded into shift register U1022. D0 also carries the data for the $\div N$ counter in the Phase Lock Synthesizer circuits.

D1—The N LATCH signal for the 1st LO phase lock is sent on this line.

D2—Reserved for future applications.

D3—This line resets the buffer sequencer at the outset of a talk cycle for the counters.

D4—This line (CONTROL LATCH) latches a control word into the output buffers of U2025 on the Error Amplifier board.

D5—This signal clears all the counter stages in the counter-buffer circuits in preparation for a count sequence.

D6—This line latches the N data in U1022.

D7—This line is used as a clock to step data into U1022 and U3048A, and for the data sent in the 1st LO phase lock. R3012 and C2010 act as a delay to provide adequate setup time for the data prior to the clock signal arriving.

Buffers U3034, U3030, and U2026 are the talk buffers that send data to the microcomputer. U3018 and U2030A make up a step-enabler that enables the talk buffers one at a time when requested by the microcomputer.

Input Amplifiers and Multiplexer

Q1018 brings the -5 dBm, 16 MHz to 20 MHz signal from the 2nd LO up to TTL levels. U2010 divides the 16–20 MHz by 32 and 256 before it sends it to multiplexer U1018. U2056 amplifies the -50 dBm, 10 MHz IF. L2056 and C2056 act as a 10 MHz bandpass filter on the input of U2056. R3056 provides current to the open collector output of U2056. C3052 couples the 10 MHz signal into U4056. U4056 acts as a divide-by-128 counter. The signal then goes to U1018.

All other input signals are at TTL levels and are connected directly to U1018. The output of U3010A is connected to U1018 so that the clock can be counted for diagnostic purposes. U1018 selects one of its inputs according to the data in U1022.

$\div 2^n$ Counter

The output of U1018 goes into a series of dividers made up of U1050 and U2050A. Various outputs of these dividers are connected to multiplexer U1046 to give a $\div 2^n$ counter where $n = 1, 2, 4, 6, 8, 10, 11,$ or 12 (n is selected by the data stored in U1022). A strobe input to U1046 disables the multiplexer when pulled high.

21-Bit Counter

The 21-bit counter counts the 100 MHz reference frequency to give a measurement of the time required to complete a given number of cycles of the selected input signal. The counter itself consists of U1038, U2018, U1028, and U2034. U1038 is an ECL divider. Q1034 and Q1044 are ECL-to-TTL translators for the $\div 2$ and $\div 4$, respectively. The $\div 4$ goes to U2018 where it is counted with TTL dividers, and the divider chain continues through U2034. The output of each stage goes to an output buffer so the microcomputer can read the final number of counts. Therefore, measure the time period during which the counter was enabled. The counter is enabled by U2050B and U2046 for a time period equal to eight cycles of the output of the $\div 2^n$ counter.

At the start of a count, the microcomputer selects the input signal to be counted and selects the n number for the $\div 2^n$ counter. The COUNT/RESET line is then pulled high to reset all of the counters. U2046A is preset with Q in the high state, which disables the 21-bit counter. The COUNT/RESET line then goes high to start the measurement process. The output of U1046 goes to U2050B where it is further divided down. On the first rising edge at QA of U2050B, Q of U2046A goes low to start the 21-bit counter. On the eighth count of U2050B, U2046A steps back to its original state, which stops the 21-bit counter. At the same time, U2046B pulls the strobe to the $\div 2^n$ counter high to stop any further counts in U2050B. The microcomputer can now read the VALID COUNT line to determine when the count process is completed, and then read the data that is stored in the 21-bit counter.

PHASE LOCK SYNTHESIZER



The Phase Lock Synthesizer consists of: the Error Amplifier, the Synthesizer, Offset Mixer, Controlled Oscillator, and Strobe Driver. The following describes the circuits and their function.

Synthesizer



The Synthesizer uses the 100 MHz reference frequency from the 3rd Converter to generate the 25 MHz reference frequency for the Offset Mixer and the $\div N$ frequency (determined by the N number from the Processor) for the phase/frequency detector in the Offset Mixer. The $\div N$ number is within the 32 to 94 kHz range.

The Synthesizer can be divided into three functional blocks: the 100 MHz divider, the 50 MHz divider, and the $\div N$ counter.

The 100 MHz divider consists of flip-flop U3030 and differential pair Q3040 and Q3041. The 100 MHz signal from the 3rd Converter stage is applied to the clock input of U3030. (One-half of U3030 is used to furnish a stable bias source for the clock input.) The 50 MHz signal from the Q output is applied through buffer amplifier Q3041 to P500; it is not used in the 494. The signal from the complement output of U3030 is applied through Q3040 to U1040B, the 50 MHz divider.

The 50 MHz divider consists of the flip-flop U1040B. The 50 MHz from the collector of Q3040 is applied to the clock input of U1040B which divides the signal to 25 MHz. The signal from the Q output is sent to the Offset Mixer circuits. The complement signal is applied to the $\div N$ counter.

The $\div N$ counter consists of two shift register/latches U2020 and U2030; three counters, U2010, U1020, and U1030; and flip-flop U1040A. The circuit is controlled by three signals from the microcomputer via the Counter board. The output of the $\div N$ counter is a frequency within the range of 32 to 94 kHz which is applied to the phase/frequency detector in the Offset Mixer. When power is first applied, and before phase lock is selected, this counter typically outputs a frequency of approximately 6 kHz.

When phase lock operation is selected, the microcomputer sends data and a data clock to load a number into the latches, which accept and store serial data. The num-

bers that come from the microcomputer, range from about 3300 to 3830, so the count remaining, until the counters overflow, is from about 265 to 795. When the number is loaded, the N LATCH signal transfers the number from the input shift registers to the output registers of U2020 and U2030 where they are available to the counter stages. This presets the counters to a predetermined value, as just mentioned. Once loaded, the counters count at a 25 MHz rate to accumulate the remaining number of digits until they are full. The TC output of U1030 then moves high and U1040A changes state. This presets the N number in the counter stages for another count cycle. The TC output of U1030 is again simultaneously set low so the next cycle of the 25 MHz clocks U1040A back to the reset condition. The resultant output of U1040A is a series of positive pulses that range in period from 10 μ s to 31 μ s which is equivalent to 94 to 32 kHz. This signal is sent to the phase/frequency detector in the Offset Mixer for comparison with the difference frequency generated in the mixer circuit.

ERROR AMPLIFIER, CONTROLLED OSCILLATOR, OFFSET MIXER, AND STROBE DRIVER



Error Amplifier

The Error Amplifier: 1) Integrates the error signals from the Offset Mixer and produces a correction voltage to pull the VCO to a frequency that is synchronous with the $\div N$ signal. 2) Generates a STROBE ENABLE to enable the strobe generator in the Strobe Driver circuit. 3) Produces an UP or DOWN signal to alert the microcomputer that the drive current to the 1st LO FM coil is reaching its limit in holding the 1st LO in phase lock. 4) Generates an F ERROR signal, from the outer loop ERROR 1 signal, to be used by the Counter board for diagnostics. 5) Provides the F(s) amplifier for the outer loop.

The digital control circuits consist of shift register U2025 and quad switch U2037. Data from the microcomputer is fed serially, via the Counter board circuits, into the shift register, then transferred to the output lines by the CONTROL LATCH signal. Table 7-21 lists the purpose of the output lines.

Differential amplifier, U3075 compares the FsB and FsA outputs from the phase/frequency detector on the Offset Mixer board and furnishes the oscillator tune voltage for the VCO. Refer to the Offset Mixer description that follows, for a more detailed description of this circuit.

Table 7-21
U2025 OUTPUT LINES

Line	High	Low
Q1	Window disabled (Q5 low)	Wide window (Q5 low)
Q2	Lock (connected FM coil)	Unlock (disconnected FM coil)
Q3	Wide loop gain response	Narrow loop gain response
Q4	Strobe enabled	Strobe disabled
Q5	Narrow window	Wide window (with Q1 low)

The loop amplifier circuit consists of amplifier U2048 and surrounding components. The ERROR 1 signal from the Phase Gate Detector and Error Amplifier is applied through LOOP GAIN adjustment R3082 to the inverting input of U2048. The signal (ERROR 1) is a result of the comparison of the 1st Local Oscillator frequency and the nearest multiple of the STROBE signal from the Strobe Driver circuit. The ERROR 1 signal varies from zero to about 500 kHz, and is up to four volts peak-to-peak in amplitude.

When phase lock is not required, data into U2025 sets output Q2 and Q4 low and Q3 high. This opens the connection between pins 11 and 10 of U2037 and the connection between pins 2 and 3. STROBE ENABLE line to the Strobe Driver goes high and disables the strobe pulse. The FM coil of the oscillator is opened by U2037 which opens the outer loop.

To establish phase lock, the microprocessor sets the 1st LO near the desired lock point and loads the proper N number into the synthesizer. The 5 MHz strobe is then turned on (Q4 and Q2 output of U2025 set high) and the microprocessor tunes the 1st LO up or down 750 kHz either side of the desired lock point at a 10 Hz rate. When the oscillator frequency crosses the desired lock point, the ERROR 1 frequency is reduced to a dc voltage which results in U2048 pulling the 1st LO in the direction required to maintain a constant frequency. When the microprocessor measures the 1st LO frequency and finds it held constant, at the desired frequency, it then sets Q3 output of U2025 low to reduce the bandwidth of the phase lock loop.

Window comparator, consisting of U1015 and the associated components, is used to sense when U2048 has approached its operating limits. When the microcomputer causes the Q2 signal to close the path from U2048 to the FM coil, U2048 begins to furnish current to the coil which causes the 1st LO to track the stable strobe signal. That is, each time the 1st LO frequency drifts, the ERROR 1 signal changes and U2048 shifts the FM coil current to bring the 1st LO back to its original frequency. At the same time, the microcomputer causes lines Q1 and Q5 to be low, closing the contacts that connect the output of U2048 to the input

of the window comparator through a divider network. Now, as the 1st LO frequency drifts, the loop amplifier will compensate for the drift. If the drift is excessive, however, U2048 will approach its design limits and will be unable to furnish any more current to the FM coil.

Window comparator U1015 is a dual comparator that senses a deviation of ± 15 mV. For example, if a frequency shift forces U2048 to move positive enough (approximately 3 V), the upper half of the comparator conducts, and the UP line goes high. This triggers the service request circuits on the Counter board, which in turn alerts the microcomputer so it begins adjusting the TUNE voltage from the Center Frequency Control circuits to reduce U2048 output to zero. If the output drifts negative, the other half of U1015 conducts, causing reverse action to occur.

Normally, the input signal to the window comparator is attenuated by R2043, which reduces the voltage applied to U1015 to 0.3% of the output from U2048. This allows U2048 to drift up and down without immediately triggering either comparator. When R2043 is in the circuit, it is called "wide window" operation. When phase lock is de-selected, the microcomputer selects narrow window (which bypasses R2043). The Center Frequency Control circuit is then instructed by the microcomputer to move the 1st LO frequency until the window comparator indicates that the FM coil current is near zero. This prevents the 1st LO frequency from shifting too far from the lock point when phase lock is cancelled.

The ERROR signal filter circuit, consists of an active low-pass filter U2065 and Schmitt trigger U1035. This circuit filters and squares the incoming ERROR 1 signal for application to the Counter board. The ERROR 1 signal is applied through C2067 to an RC, 500 kHz, low-pass filter and amplifier U2065. After filtering, the signal is applied through Error Count Breakpoint adjustment R1061 to the input of U1035, a Schmitt trigger circuit. The squared output signal is then applied to circuits on the Counter board, where it is used by the microcomputer for determining the relationship between 1st LO frequency and the strobe line.

Controlled Oscillator (VCO)

The Controlled Oscillator (VCO) is a voltage-controlled crystal oscillator whose frequency is controlled by the output of the Error Amplifier. The oscillator generates a reference signal that is used to stabilize the 1st LO frequency. Refer to the block diagram adjacent to Diagram 40 for a functional description of this part.

The control voltage from the Error Amplifier, which is a function of the difference between the microcomputer controlled $\div N$ signal and the Offset Mixer difference frequency, is applied to the VCO on the Controlled Oscillator board to regulate its frequency of operation. The circuit has two outputs: the first, which is part of the inner loop of the phase lock circuits, is fed to the Offset Mixer, where it is used to derive the difference frequency that is compared against the $\div N$ signal. The second output, which is part of the outer loop, is fed to the Strobe Driver circuits, where it is divided down to become the STROBE signal that is compared against the 1st LO signal in the Phase Gate.

The VCO consists of five major circuits, four of which are connected in a positive feedback loop to sustain oscillation. These circuits are the resonator stage, the differential amplifier, the band-pass filter, the isolation amplifier, and the output amplifier. The resonator stage operates at a frequency of 25.032 MHz to 25.094 MHz. The output signal from the resonator is applied to the input of a differential amplifier which drives the output amplifier and the band-pass filter. The output from the output amplifier is fed to the Offset Mixer and the Strobe Driver. The band-pass filter strips the signal of any spurious either side of center frequency and feeds the signal to the isolation amplifier. This stage furnishes the positive feedback drive to the resonator stage and isolates the band-pass filter from the resonator stage.

The resonator stage consists of crystal Y1012, varactor diodes CR1011 and CR1012, and related components. The stage operates within the frequency range of 25.032 to 25.094 MHz, which is controlled by the voltage applied to varactor diodes CR1011 and CR1012. Feedback energy for sustaining oscillations comes from the isolation amplifier by way of coil L1025.

The resonator output signal is applied to a differential amplifier Q2033 and Q2041. The Q2033 side drives the output amplifier and serves to isolate the output load from the feedback loop. Gain from this side is less than one. The signal is fed from the collector of Q2041, following amplification, to the band-pass filter.

The band-pass filter consists of passive components, and is used to strip the signal of any frequency components more than about 40 kHz away from the center operating

frequency, which is approximately 25.06 MHz. Capacitors C1041 and C1042 are adjusted at the factory to set the bandwidth and center the frequency of the filter.

The isolation amplifier, Q1028, is a common-base configuration, in order to match the impedance of the filter to the resonator. Output current from the stage furnishes positive feedback for the resonator.

The output amplifier, consisting of transistors Q2025 and Q2026, is connected as a differential amplifier with Q2026 driving one side of the Offset Mixer and Q2025 driving the input of the Strobe Driver circuit, for eventual application to the Phase Gate circuits.

Offset Mixer

The Offset Mixer consists of a ring diode mixer circuit, a differential amplifier, and a phase/frequency detector. For explanatory purposes, assume that the Controlled Oscillator (VCO) frequency is at 25.06 MHz and the $\div N$ signal is 50 kHz. The 25.06 MHz signal from the VCO enters the board at pin N of the Offset Mixer assembly. It is applied to the base of transistor Q2021 which drives transformer T2010. The output of T2010 is connected across the ring diode mixer. The 25 MHz reference frequency is applied at pin K of the Offset Mixer and coupled through T1010 to the ring diode mixer. The four frequency components are picked off at the center tap of T2010. The two fundamental frequencies and the sum are blocked by a π filter, and the 60 kHz difference is coupled across T2030 to a differential pair Q1020/Q1030, then amplified to TTL levels by amplifier Q1040 and applied to the clock input of flip-flop U1050B (part of the phase/frequency detector).

The phase/frequency detector consists of flip-flops U1050A and U1050B, NAND gate U2050B, and inverter U2050A. Now, if the loop had been locked, the two flip-flop clock input signals would have been edge-coincident. Pin 4 and 5 inputs of U2050B would have moved high and after the signal at TP1058 goes low, the NAND gate would have reset both flip-flops. This results in a series of pulses of equal amplitude and width from each of the flip-flops which, when applied to the Error Amplifier, would not shift the frequency of the VCO.

It is assumed, however, that the $\div N$ signal is 50 kHz and the difference frequency from the collector of Q1040 is 60 kHz. Thus, the output of Q1040 is leading the $\div N$ signal. U1050B will "set" first, placing a high at the inverting input of U3075. This pulls the output of U3075 low until U1050A sets. A short time later U2050B resets both flip-flops and U3075 will switch back, until the next correction cycle. This process continues until the two signals, applied to the Phase/Frequency Detector, are edge coincident.

The correction voltage, in this example, from U3075, is applied to the frequency determining components of the VCO and its frequency shifts downward. The frequency of the oscillator will continue to decrease until the output of U3075 is stable.

The Error Amplifier, is described here because it is an integral part of the inner loop. The stage consists of differential amplifier, U3075, with its two inputs being driven by the output of U1050A and U1050B. As the signals driving the amplifier continue toward one direction, the output of U3075 continues to drive the oscillator down in frequency. VR2065, CR3069, R2067, and C2072 clamp the output of U3075 to prevent forward biasing the varactor diode and stopping the oscillator.

Strobe Driver Circuit

The Strobe Driver circuit consists of counter U1022, bandpass filter FL2064, source follower Q2091, and AND gates U1091A and U1091B.

The VCO output is applied to the clock input of a $\div 5$ counter U1022. The STROBE ENABLE line from the Error Amplifier permits the counter to operate when the line is low and is the means by which the microcomputer can turn the strobe pulses on or off. The output of the counter is coupled through an impedance matching network consisting of C2030, L1031, C2033, and C1032, to the input of bandpass filter FL2064. The impedance matching circuit raises the line impedance to about 8200 ohms. The output of the filter drives another impedance matching network for the gate input of Q2091. The output of Q2091 drives two buffer amplifiers U1091A and U1091B. U1091B drives the Phase Gate circuitry, and U1091A is reserved for future applications. Capacitors C1032 and C2105 are selected to provide maximum signal amplitude at TP2087.

DIGITAL CONTROL SECTION

The Digital Control section provides the operator/494 and digital controller/494 interfaces. It translates changes in front-panel controls and instructions received, via the accessories interface or GPIB interface (494P only), into codes that control the instrument via the instrument bus.

The Digital Control section simplifies operating and programming the 494 and 494P. Unless overridden by the operator, the microcomputer automatically selects secondary parameters. Some examples are: when the operator selects span, the microcomputer chooses an appropriate bandwidth; when the operator changes the reference level, the microcomputer trades off input attenuation and IF gain.

The microcomputer can also perform many operations automatically, such as; automatic peaking, centering signals in the span, and directing the user through a calibration procedure.

The digital control operating program is defined by the meaning of the controls and commands given in the operating and programming manuals and is not further defined here. The following description focuses on the hardware for the following major circuits that comprise the digital control section:

1. Microcomputer, including Processor and Memory boards.

2. Addressable registers on the instrument bus.

Front panel.

4. Accessories interface.

5. GPIB interface (494P only).

MICROCOMPUTER

The microcomputer consists of a Motorola 6802 microprocessor, a 6840 timer IC, a 6821 PIA IC, a 9914 GPIA interface, 48K bytes of EPROM, and 14K bytes of RAM. An additional 96K bytes of EPROM is bank-switched between addresses 4000 and 8000 (hex). Switches are provided to modify the instrument configuration for performing self diagnostics. Refer to the appropriate Motorola or Texas Instruments data sheet for descriptions of the microprocessor and the three peripheral devices.

Storage of the instrument front panel control settings and displays is provided by 6K bytes of battery-powered RAM. This is CMOS RAM in 2K x 8 chips, powered by a 5 V line when the instrument is operating and by a 3 V lithium battery when the instrument is turned off. An additional 8K of RAM is provided for use by the instrument operating system.

The microprocessor (U1034) communicates with the memory and I/O ports via the microprocessor bus and with the rest of the instrument via the instrument bus. The micro-computer bus consists of 8 data lines (D0-D8), 16 address lines (A0-A15), a VMA line, the R/W (read/write) line, the ϕ 2 clock line, and the RESET line.

The microprocessor communicates with the instrument bus through a 6821 PIA IC (U2010). The instrument bus consists of 8 data lines (DB0-DB7 Table 7-22), 8 address lines (AB0-AB7), a POLL line, a DATA VALID line and a SER REQ line.

Additional control lines connect different portions of the processor system: a GPIB SRQ line, a SWP GATE line, a PWR FAIL line, a CRT CLK line, an I/O (3XXX) line, and the INTL CONT line.

Interrupts are handled by the microprocessor in the following manner. Interrupts can be generated by hardware on the instrument bus, the GPIA interface IC, or the 6840 timer IC. The 6802 will first determine which of the three sources initiated the interrupt. If the interrupt is on the instrument bus, the 6802 initiates a poll routine to determine the particular piece of hardware, on the instrument bus, that generated the interrupt.

The instrument bus poll sequence is as follows: When an interrupt is received, from the instrument bus, the micro-computer puts an FF (hex) on the instrument address lines. This sets the poll circuits to reply. The microcomputer then raises the POLL line and asserts DATA VALID. At this point, the circuit that generated the interrupt asserts its respective bit on the instrument data bus. The microcomputer reads the data bus and remembers the bit. The poll line is lowered, then address 7F is put on the address bus. The data valid line is then raised. This sets up the poll circuits to receive the poll bit in reply. The microcomputer now writes the poll bit back on the data bus and the circuit that initiated the interrupt, resets and removes the interrupt signal. The microcomputer then services the interrupt.

TABLE 7-22
LIST OF POLL BITS

Bit 7	Not used
Bit 6	Reference Lock module
Bit 5	Not Used
Bit 4	End Of Sweep
Bit 3	CENTER FREQUENCY knob
Bit 2	Phase Lock
Bit 1	Not used
Bit 0	Front Panel

Figure 7-30 (System Memory Map) depicts the entire address range of the processor, including the bank-switched EPROM's between 4000 and 8000. The diagnostic LED's are at addresses 0800 to 3800.

Figure 7-31 (I/O Address Map) depicts the address range between 3800 and 4000. Data is transferred between the microprocessor and various external systems (instrument bus, GPIB bus, switches, etc.) within this range. Most of the addresses are unused; this is shown by the stippled areas of the address range.

Figure 7-32 (PIA & Timer Address Map) show details of the PIA and Timer address structure.

PROCESSOR BOARD

The 6802 processor (U1034) has its data lines buffered by U1026, a bi-directional bus transceiver IC. The processor address lines are buffered by U2032 and U2028. In addition, gates on U2024 are used to buffer the $\overline{R/W}$, the VMA, the CLOCK ENABLE, and the RESET lines.

The 6821 PIA IC (U2010) is used by the processor to interface with the instrument bus. This IC is buffered from the instrument bus by U2012 for the address lines, and bi-directional buffer U2018, for the PIA data lines. Other gates within U2024, buffer the POLL line and the DATA VALID line. The direction of data through U2018 is controlled by the most significant bit of the instrument address bus. (As a result, all instrument bus addresses above 7F are read addresses and all addresses including 7F and below are write addresses.)

Y1036, Q1036, and Q2038 make up a discrete device clock circuit that oscillates at a frequency of 3.4133 MHz. Q1036 and Y1036 form a Colpitts crystal oscillator which is buffered and conditioned by Q2038 to give a TTL compatible clock signal. This signal is further buffered by a gate on U2024 before is is applied to the E XTAL input of the micro-processor. This frequency is divided by four, within the microprocessor, and called the ϕ 2 (enable) clock. It is used by other devices on the microprocessor bus. The 3.4133 MHz clock is called the CRT CLK and is used by the Crt Readout board and the GPIA interface IC on the GPIB board.

U1016 is a programmable timer and counter that is used by the micro- processor U1034 as a timer to generate variable time delays. In this mode, the processor programs a given time interval into the timer and enables it. When the given time interval expires, the timer generates an interrupt and thus notifies the microprocessor. The clock signal for the timer is the ϕ 2 clock line.

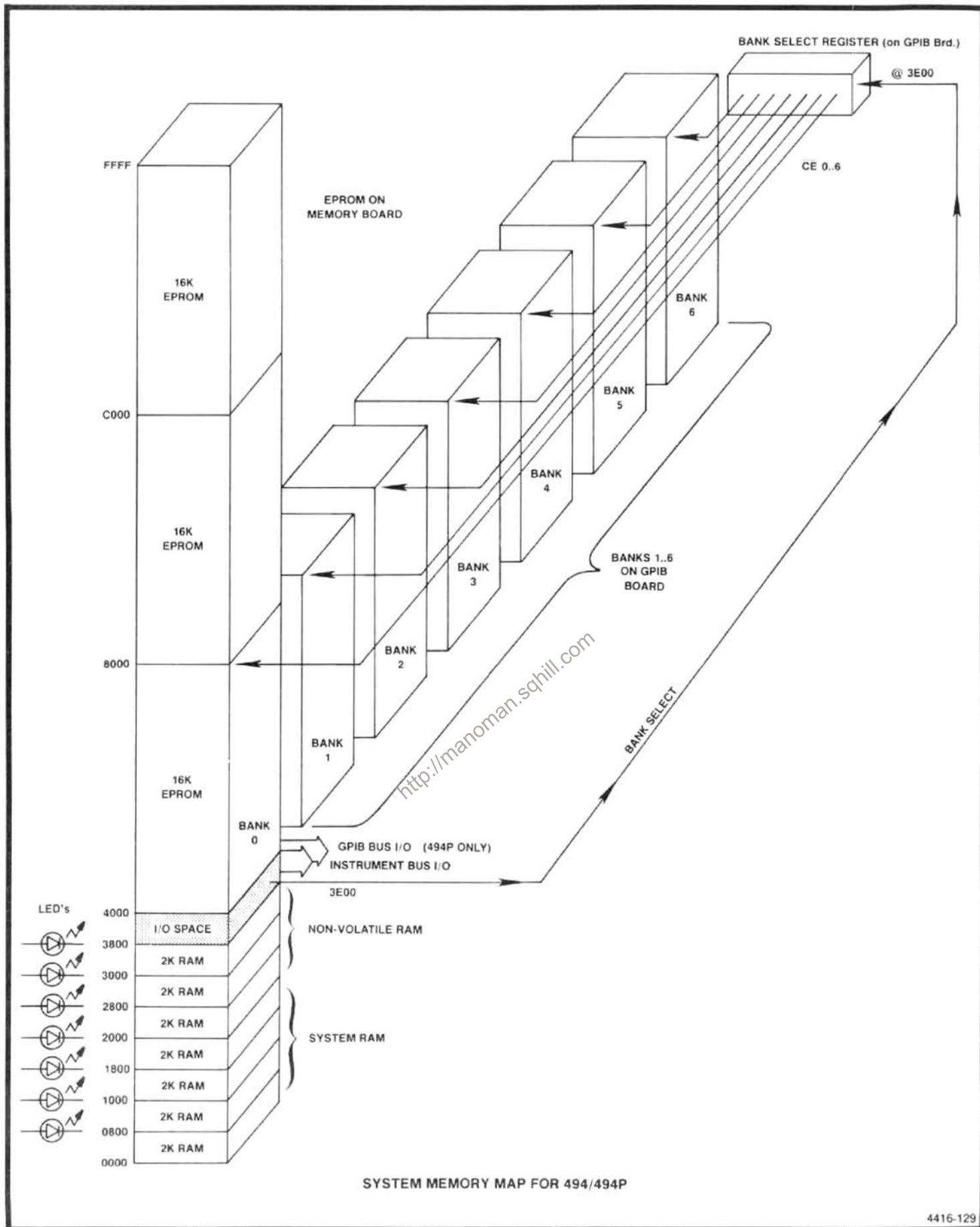


Figure 7-30. System memory map for 494/494P.

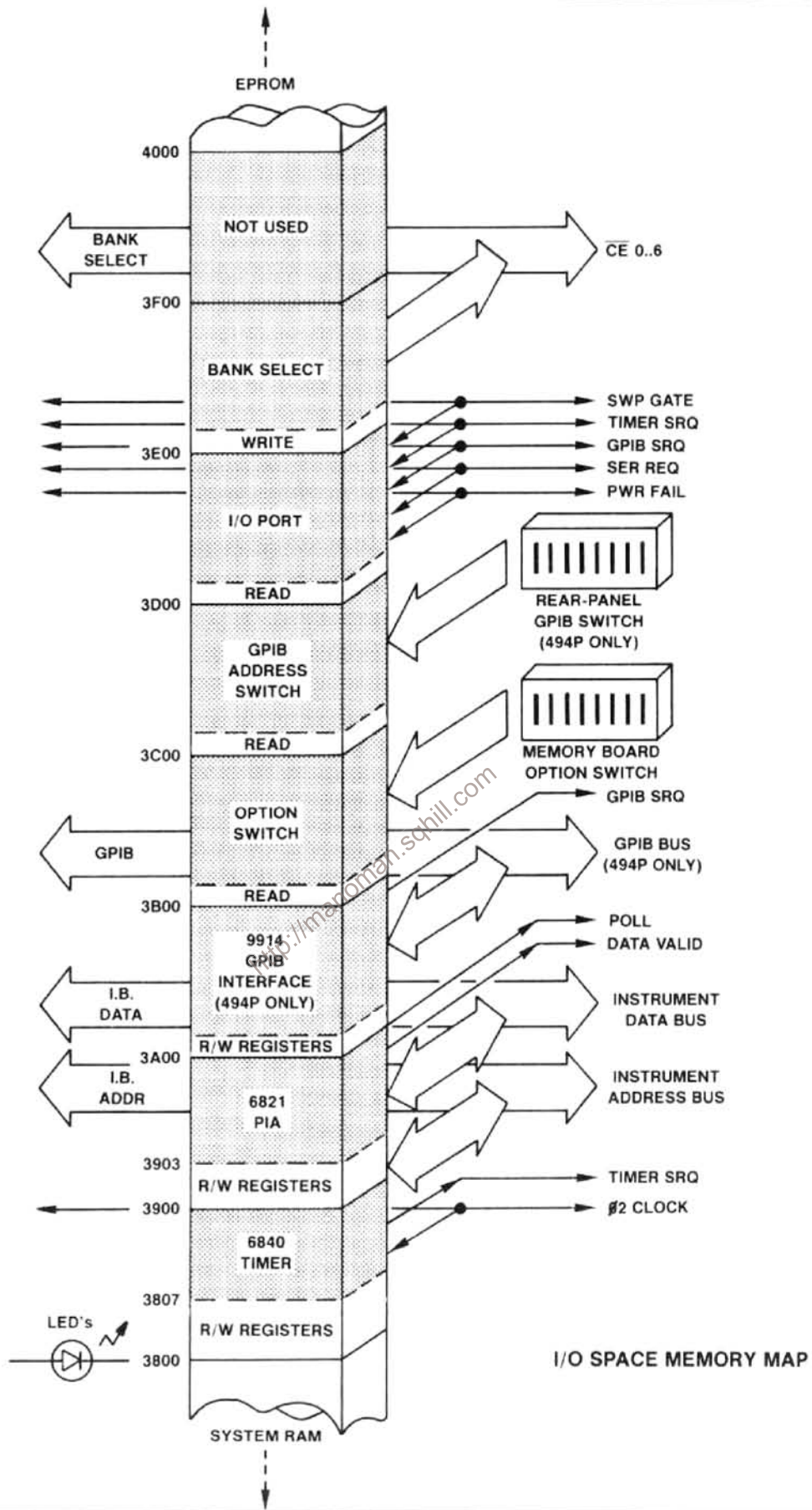


Figure 7-31. I/O space memory map.

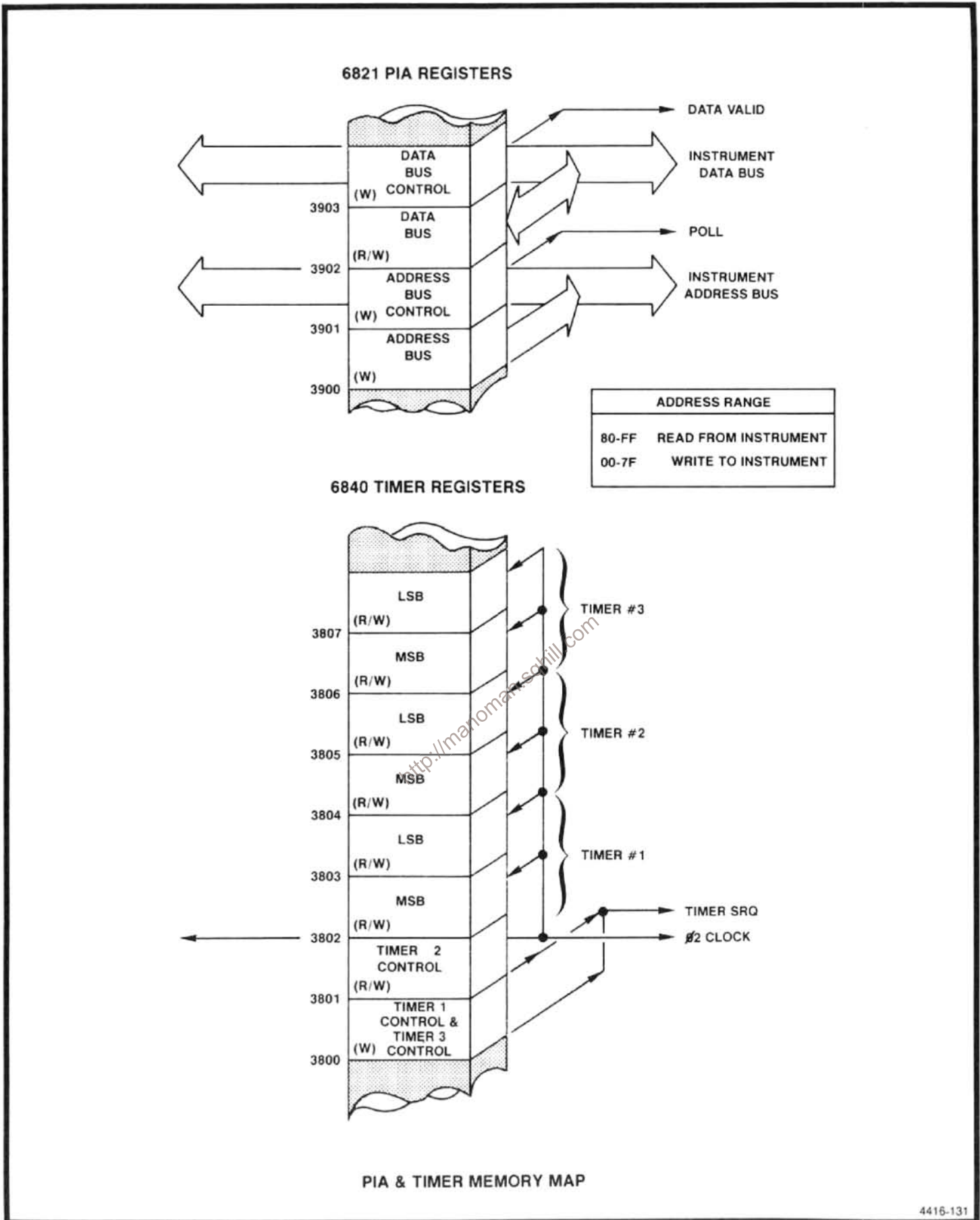


Figure 7-32. PIA and timer memory map.

U1020 is an address decoder that is activated by a signal derived from the Memory board. This signal is asserted when addresses from 3000 to 3FFF are asserted. The decoder further sorts addresses in this range and when address 38XX is asserted, the timer module is activated. When address 39XX is asserted, the PIA is activated. When address 3DXX is asserted, the I/O port (U1014) is activated.

U1014 is a tri-state buffer that is used by the micro-processor to monitor three interrupt lines and the sweep gate.

A circuit on the Z-Axis board monitors the power input ac line. If a power loss is detected, the PWR FAIL line goes low which tells the processor that power is about to fail. The PWR FAIL line is connected to the NMI (non-maskable interrupt) input on the processor and when the line goes low, the processor gets a non-maskable interrupt and starts its power-fail routine.

The PWR FAIL line is also applied, through a gate, within U2020 and Q2028, to the Reset input of U1034. When the PWR FAIL goes low, Q2028 is turned on and C1022 begins to discharge through R2022. If the line stays low for a period of time, the RESET line will also go low and the micro-processor resets itself if the power has been interrupted long enough to seriously disturb the logic power supplies. As part of its power down routine, the processor keeps checking the PWR FAIL line through U1014. If the PWR FAIL line returns to its high state, within the prescribed time, the processor will do a power-up initialization to ensure that the instrument operation will not be affected by a possibly low +5 V line to the various control latches.

MEMORY BOARD

The Memory board contains all the memory within the address range of 6802 processor. On this board are 48K bytes of ROM contained in three 16K byte EPROMs. These are Intel type 27128 EPROMs which can be programmed and then erased by exposure to ultraviolet light (see an Intel 27128 data sheet for a description of these EPROMs). There are also seven 2K byte CMOS RAMs, that comprise the read/write memory. To aid in self-diagnostics and instrument configuration, a set of LEDs and switches are provided.

The "D" flip-flop, U2049, is used by the processor to power-up and enable all the non-volatile RAMs. On initial turn-on, U2049 is reset by the RESET line. This causes the non-volatile RAM to remain in its data retention mode. After the processor has finished its initialization power-up sequence, it writes to the instrument address bus (73) to set U2049's output high. This allows C1045 to charge to +5 V and Q1042 and Q1043 are turned on. Q1042 turns on first and connects the V_{dd} input for the RAM to +5 V through Q1041. Q1043 then turns on and pulls CE2 input low to take the RAM out of the data retention mode. If for some reason the processor crashes on power up, non-volatile RAM is protected from alteration since U2049 output will remain low.

On power-down the processor, after it completes tasks required for power-down (storing power-down settings in non-volatile RAMs and switching the RF attenuator to 60 dB attenuation), will set the output of U2049 low. This takes about 10 ms after POWER FAIL goes low. C1045 discharges and turns Q1043 and Q1042 off, which switches the V_{dd} input for the RAMs to the battery voltage backup supply on the GPIB board. At the same time the RAM's are switched to the data retention mode, since CE2 is connected to V_{dd} through R1039. About 60 ms after POWER FAIL goes low, the RESET line goes low and U2049 is reset to ensure that the RAM has been switched to the data retention mode, before power fails.

U2015 (at 4000), U1021 (at 8000), and U1014 (at C000) are the 27128 EPROMs. U2015 is wired to form bank 0 of the bank-switched ROM system.

U1036, U1046, and U1041 are address decoders. U1036 decodes the higher order addresses: 0000, 4000, 8000, and C000. U1046 decodes addresses for the RAMs at 0000, 0800, 1000, 1800, 2000, 2800, and 3000. U1041 is an address decoder for the I/O space. Address 3800 is used to access the Options switch.

U1036, S1038, and pull-up resistors in R1038, comprise the Options switch. Switches within S1038 can be set to configure different instruments, inform the processor of revised hardware, or initiate self diagnostics.

DS1046, DS1047, DS1048, and DS1049, connected in the output lines of decoder U1046, are diagnostic LEDs used to indicate the results of the processor self-diagnostics.

GENERAL PURPOSE INTERFACE

The GPIB board contains ROM for the basic instrument functions as well as for the GPIB interface plus the GPIA to connect the microprocessor to the GPIB. The board also contains bank-switch circuitry for accessing additional ROM on this board and on the Memory board, plus a voltage back-up circuit for non-volatile RAM's on the Memory board.

Since the 6802 microprocessor is only capable of directly addressing 65,536 bytes of address space, 96K bytes of ROM on this board plus 16K on the Memory board, are addressed by a process called bank switching.

32K bytes of ROM (8000 to FFFF) on the Memory board are directly addressed by the processor. The remaining 112K bytes, stacked in banks 16K bytes wide and 7 deep, are accessed by means of bank switching. The bank number, from 0 to 6, is written by the processor to register U1033 at address 3E00. The number in the register is decoded by U1032 and its output turns the appropriate EPROM on. The processor can now access that EPROM in the usual manner at addresses 4000 to 7FFF. If the processor wishes to access another bank, it must first put a new number in the bank switch register U1033.

U1012, U1018, U1022, U1024, U2013, U2018, and U2022 comprise the bank-switched ROMs and consist of 16K byte EPROMs (Intel 27128's). These, plus U2015 on the Memory board, comprise the seven level bank as depicted in Table 7-23.

TABLE 7-23
LEVELS OF MEMORY BANK

Level 0	U2015 Memory board
Level 1	U1012 GPIB board
Level 2	U1018 GPIB board
Level 3	U1022 GPIB board
Level 4	U1024 GPIB board
Level 5	U2013 GPIB board
Level 6	U2018 GPIB board
Level 7	U2022 GPIB board

in the I/O space. It is driven from a decoder on the Memory board. Address 3E00 will access the bank switch register, address 3C00 the GPIB switches, and address 3A00 the GPIB interface IC U2036.

Tristate buffer U2027 is used to read the rear panel GPIB switches. Each input line is decoupled by a resistor capacitor combination to minimize noise and unwanted pulses. R2030 contains pull-up resistors for the lines. This buffer is accessed at address 3C00.

U2036 translates microprocessor commands, on the microcomputer bus, into appropriate codes and protocol for the GPIB bus. It also decodes data from the GPIB for the microcomputer bus. Interrupts are generated by pulling down on the GPIB SRQ line. The CRT CLK line provides the clock reference. This IC is accessed at address 3A00.

The voltage backup supply for the non-volatile RAM, consists of a small, high-energy, 3 V lithium battery (BT1022). During normal operation, when +5 V for the non-volatile RAM is supplied from the power supply, via Q1041 on the Memory board, CR1025 is reverse biased so the battery is protected from reverse charge. When a power failure occurs, the 5 V supply to the non-volatile RAM's on the Memory board deteriorates. CR1025 is then forward biased so power is provided from the battery for power-off data retention in the RAM's.

ACCESSORIES INTERFACE BOARD

The Accessories Interface board provides access to the instrument bus and input and output for two analog signals. This access, to the instrument bus, can be used for diagnostics or by other accessories.

The two analog signals are; an input MARKER/VIDEO, through a coaxial connector, an output EXT PRESEL and a EXT PRESEL RETURN (a differential signal on the ACCESSORIES connector). To display an external signal that is applied to the MARKER/VIDEO input, pull the EXT VIDEO SELECT line (pin 1 of the ACCESSORIES connector) low. The EXT PRESEL output will drive an external preselector. It is valid only in preselector bands (1.7 GHz to 21 GHz). This signal tracks the instantaneous frequency at a nominal 2.1 GHz/V with zero output corresponding to 2.072 GHz.

The instrument bus is buffered and brought out to the rear panel with the lines named to indicate their relation to the internal bus: ADV for DATA VALID, APOLL for POLL, etc.

the 494/external device interface. INTL CONT is asserted low by an external controller to disable the internal microcomputer's instrument bus buffers. This sets the address buffer U2033 and control-lines buffer U2015, to drive the

address lines, DATA VALID and POLL lines, and listen to SER REQ. It also sets U2038 to indicate the direction of data through the data lines buffer U2025, depending on the sense of the MSB of address AB7. When INTL CONT line goes low, U2038 is set to drive the buffer in a manner similar to the Processor board data buffer—a write to the internal bus if AB7 is low and a read if AB7 is high. When INTL CONT is high, the buffer is enabled to write to the external bus when AB7 is low and read when AB7 is high.

The DATA BUS ENABLE line is asserted low by an external device to enable the data buffer. As long as this line is unasserted, the data buffer is set to its high impedance state and the data direction input has no effect on its output.

FRONT PANEL

The Front Panel board is an interface between the user and the instrument. It translates an operator action, of a front panel control, into data for the microcomputer to read and implement. It outputs data showing current operating modes to the user, via LED's and Crt readout.

NOTE

In this description, the front panel CPU (8741) or slave, is referred to as CPU. The instrument processor (6802) is the master processor or master microcomputer.

Output of data is provided by five shift registers that drive LED's (light emitting diodes) to illuminate various front panel push buttons and indicators to show the instrument operating mode. Operator input information, via push buttons or rotary switches, is read by the CPU. The front panel CPU then outputs the data to the master processor for action. The front panel CPU scans all push buttons and rotary selectors, on the keyboard matrix, plus the coder for the FREQUENCY knob, looking for changes in the keyboard codes or frequency coder. It then translates these changes into an appropriate code for the master processor so it can take appropriate action. The following is a description of the hardware and a brief description of the software used by the front panel CPU.

Potentiometers

The following controls or adjustments generate analog signals that are used by other functions of the instrument. These controls are non-programmable.

INTENSITY is an input to the Z-Axis/RF Interface board to control trace brightness.

PEAK/AVERAGE is a digital storage input that causes signals to be either peak detected above or averaged below a displayed cursor line that tracks this control.

MANUAL SCAN sweeps the spectrum or display in manual sweep mode.

POSITION centers the horizontal and vertical deflection on the crt.

LOG/AMPL CAL varies the video signal level prior to the Video Processor board and adjusts 10 MHz IF gain to calibrate the log display.

PEAKING controls the front-end response of the analyzer by fine tuning the internal preselector or by varying the bias on an external mixer.

Output Mode Shift Registers and LED's

As previously described the mode of operation is illuminated by LED's that are mounted behind a pushbutton or below some front-panel nomenclature. There are 35 of these LED's. Some 49X versions may not use all indicators; for example, the non-programmable versions do not have a RESET TO LOCAL button.

The LED's are driven by shift registers (U5045, U6081, U6028, U6045, and U1049) that reside at address 74 on the instrument bus. The shift registers that drive the LEDs are reloaded each time a LED changes state. The master processor changes the appropriate bit in the LED code then reloads all registers. The shift register U6081 that drives the GRAT ILLUM, LED, also controls the voltage regulator U6090, which provides power for the graticule lights DS1011 and DS1013.

Processor

The CPU (Intel 8741) is a self-contained 8-bit processor with on-chip EPROM and RAM. (Refer to Intel UPI Users manual for a complete description of the 8741)

The IC has a self contained clock that uses Y3030 (a 6 MHz crystal) as the resonator, and a timer that functions either as a programmable timer or counter. The CPU has two input/output ports. Port P10-P17 is input only and P20-P27 in an input/output port. Each port is 8-bits wide. In addition, the CPU has an 8-bit data port (D0-D7) called the output buffer, which talks to the master processor. In this application all data is output only with U4030 being a buffer

between the CPU and the instrument bus. Information that the CPU wishes to relay to the master processor, is loaded into a latch connected to the output buffer U4030. The master processor accesses the CPU by pulling address F4, out of decoder U6024, low to activate the output buffer and enable U4030 so data is passed onto the instrument bus.

The CPU is reset by the master processor. When DB3 is selected for more than 10 ms (same as writing 08 at address 74) C1016 charges and U1024A output resets the CPU.

Scanning the Keyboard

The front panel keyboard contains 74 keys arranged in a matrix of 4 rows of 8 columns and 6 rows of 7 columns (see Figure 7-33). The RESOLUTION BANDWIDTH, SPAN/DIV, TIME/DIV, MIN RF ATTEN dB, and REFERENCE LEVEL selectors are rotary switches where each contact occupies a position in the keyboard switch matrix. The TIME/DIV and MIN RF ATTEN are position dependent. The master processor notes the current setting of these selectors by noting which contacts are closed. When a change is made the master microcomputer notes which direction the selector was moved by noting the relative position of the current contact closure with the previous setting. Pull-up resistors, within R2041 plus R2044, on each column of the row currently being read, will pull that column high if the switch is open. The basic algorithm of scanning is to pull one row at a time down and note which columns have a 1 or 0. Port one, P10-P17, (pins 27-34) read the columns. Part of port two (pins 21-24) are responsible for activating the rows. Basically the process consists of pulling one row at a time down to a logic 0 and then reading all the columns. If a switch contact is open it reads a "1" and if it is closed it reads a "0".

Since there are 10 rows to scan and only 4 pins (P20-P23) available at the number 2 port, the output is multiplexed through U4021 and U5021. These IC's are open collector output, TTL compatible multiplexers. They decode data out of P20, P21, P22, and P23 (pins 21-24) and their output pulls the appropriate row of keys down. Figure 7-33 is a chart showing the switch matrix codes, and which keys correspond to a given address in the matrix code. Note that column 6 contains the MIN RF ATTEN settings, column 7 the SPAN/DIV and RESOLUTION BANDWIDTH settings, column 8 the REFERENCE LEVEL settings, and columns 1 & 2 are devoted entirely to the TIME/DIV selections.

Due to the characteristics of the switch matrix, if two keys, in any row or column are closed, and a third is closed so three corners of a rectangle are established in the key matrix, the CPU will see a phantom closure at the fourth corner. For example; if Y6/X3, Y6/X7 are closed, and then Y3/X7 is closed, the CPU will see a phantom closure at Y2/X3 as it scans the key matrix. To suppress these phan-

tom key closures, diodes have been added in series with the RESOLUTION BANDWIDTH, MIN RF ATTEN, SPAN/DIV, and certain other keys in column 6 and 7 of the key matrix. In addition, an error detection algorithm is used in the CPU to eliminate additional phantom key closures that might occur.

Scanning the FREQUENCY Control Coder

The FREQUENCY control contains a pair of phototransistors that output a gray code through U1024B and U1024C to P27 and P26 (pins 37 & 38) of the CPU. This gray code signifies the direction the control is turned. During a scan cycle, the CPU looks at the status of the FREQUENCY control code and if it detects a change, the CPU performs a shift and exclusive-OR operation which derives the correct code to output over the instrument bus to the master processor to tell it which direction to tune the center frequency.

Outputting the Correct code

The remaining two bits out of port 2 (P24 and P25) drive the appropriate hardware and initiate an SRQ on the instrument bus. When the SER REQ line is pulled down, the master processor will service either the keyboard or the frequency coder. The front panel CPU (U3039) initiates a SRQ by pulling down P24 or P25. A low out of P24 (pin 35) will initiate a keyboard SRQ. The master processor will now service the request by reading the keyboard data in output buffer U4030. A low out of P25 (pin 36) initiates a FREQUENCY control SRQ and causes the master processor to service the request by reading the frequency code in the output buffer.

A low out of P24 is inverted by U2020C so it clocks the flip-flop U3013B. The resultant low on the \bar{Q} output pulls the SER REQ line down. (Refer to the instrument bus POLL sequence described under the master processor description for the service request sequence.) The master processor now raises both the POLL line and AB7. This is gated through U4014A as a low to DB0 on the instrument bus. The master processor reads the bus and sees a low on DB0. This indicates that a keyboard interrupt has occurred and it must read the new keyboard code. The master processor first clears the interrupt by pulling AB7 and then the POLL line low. DB0 now goes high. The processor now writes a 0 to DB0, the same as it read, and raises the POLL line. This clocks U3013A and resets U3013B which removes the \bar{SRQ} . The instrument processor now reads the data in the output buffer, U4030, at address F4. The front panel CPU now recognizes that its output buffer has been read and it resets P24 to a 1. It is now ready for another cycle.

COL	ROW							
	X1	X2	X3	X4	X5	X6	X7	X8
Y1	TIME/DIV 20 μ s 00	50 ms 0A	EXT 14	INT 1E	READOUT 28	MIN RF ATTEN 0 dB 32	FREQ SPAN/DIV 3C	R E F E R E N C E L E V E L R E S O L U T I O N B A N D W I D T H
	Y2	50 μ s 01	0.1 s 0B	SINGLE SWEEP 15	FREE RUN 1F	GRAT ILLUM 29	10 dB 33	
Y3		0.1 ms 02	0.2 s 0C	SAVE A 2 20	NARROW 5 22	MAX HOLD • 2B	20 dB 34	
	Y4	0.2 ms 03	0.5 s 0D	2 dB/DIV 4 17	LIN 1 21	PULSE STRETCHER 0 30	30 dB 35	
Y5		0.5 ms 04	1 s 0E	B-SAVE A 3 16	VIEW B RECALL 6 18	BASELINE CLIP 2C	40 dB 40	
	Y6	1 ms 05	2 s 0F	10 dB/DIV 7 19	WIDE 8 23	VIEW A STORE DISP 9 24	50 dB 41	
Y7		2 ms 06	5 s 10	HELP 1A	ZERO SPAN dB/DIV Hz/dB 2A	SHIFT 2D	60 dB 42	
	Y8	5 ms 07	AUTO 11	MAX SPAN REF LEVEL kHz/-dBm 2F	AUTO RESOLN SPAN/DIV MHZ/+dBm 25	IDENT FREQ GHz 27	RECALL SETTINGS STORE BACKSPACE 39	
Y9		10 ms 08	MNL 12	FREQUENCY RANGE ▼ 1C	FREQUENCY RANGE ▲ 26	COUNTER COUNT RESOLN 2E	Δ F ALTERNATE LANGUAGE 3A	
	Y10	20 ms 09	EXT 13	FINE CAL 1D	MIN NOISE MIN DISTORTION 1B	AUTO PEAK EXT MIXER 31	COUNT-CF 3B	

Figure 7-33. Front panel switch matrix code.

A similar process occurs when P25 (pin 36) of the CPU is pulled low by a FREQUENCY coder interrupt. A low on P25 is propagated through U2020B, U2013A, U2013B, and U4014C; only this time DB3 is involved in the poll. U2020A and U4014B decode a low on AB7 and high on POLL line to clock U2013A and 3013A.

Software

The algorithm that the CPU follows consists of a main scan routine, which is an endless loop, and four subroutines that can be called. One sub-routine runs the on-chip timer that is used to debounce the keys, another reads the frequency knob coder and derives the proper code to output to the master processor, the third subroutine reads the keyboard and stores the address of all keys that were closed, and the fourth subroutine looks at the keycode from the key addresses that were stored, and outputs the key codes and/or frequency code for the master processor. There are also a number of checks and tests that have to be done in each routine in addition to the obvious tasks.

Main Scan Routine

There are two types of scan; the first is made after a reset, the second type consists of the following scans; the keyboard, frequency coder, and the output data. During the first scan, data in the CPU is initialized. The CPU reserves part of its RAM to store and remember all key and frequency knob coder settings. During all scans, the CPU reads the frequency code and each row of keys on the keyboard. It compares what it read to that stored in RAM and if there is a difference, the CPU calls the appropriate subroutine for either the keyboard or the frequency coder knob. After a complete scan, the CPU checks to see if new information needs to be output to the instrument processor. If it does the CPU calls up the output subroutine.

Prior to the first scan, after reset, the CPU puts all 1's (highs) into its keyboard memory. This corresponds to open keys. On the first scan, the CPU will note five apparent closures due to the TIME/DIV, MIN RF ATTN, SPAN/DIV, RESOLUTION BANDWIDTH, and REFERENCE LEVEL selectors. These closures are noted and output to the master processor. Because the master processor memory knows the position of each selector to close a key, the processor calls these the power-up settings. When a front panel knob changes position the master processor can determine which direction the knob changed and what it must do to respond to the change. A complete scan, without detecting any key closures takes about 800 μ s.

Keyboard Check Subroutine

This subroutine is called when the main scan routine detects a change in the keyboard matrix which occurs when a key opens or closes. A key opening usually signifies that an

action has been completed, whereas a closure indicates that an operation or action is requested by the user; therefore, the two are treated differently by the CPU.

Because mechanical keys tend to bounce when they open or close, the subroutine must debounce each key change. To debounce, the subroutine calls up the timer subroutine. This sets a number into the internal timer and starts it running. When the timer has timed out, in about a millisecond, the keyboard subroutine again scans the row and compares this scan with the scan before the debounce check. If the scan does not compare, the routine assumes the key change was a bounce or fluke, and it returns to the main scan routine. If it does compare, the routine then recognizes that a key state has changed. It then checks to see if this is the first scan that looked for a key change after it has outputted previous information to the master processor. If it is the first pass then the routine causes the CPU to re-scan the full keyboard matrix to ensure that there is not a phantom key closure. If this is the second or subsequent pass and an actual key change has occurred, the routine then notes if the key change was an opening or closure. If it was an opening the CPU memory is updated to the fact that the key is open. If a closure has occurred, the routine will then check the column that has the closure and output a new key address onto the output stack. This address consists of the key's row and column location. After outputting the address, the subroutine returns to scanning the remainder of the keyboard matrix.

Frequency Coder Subroutine Check

This subroutine is called when the main scan routine detects a change in the frequency coder switch. Like the keyboard subroutine, this routine also debounces the frequency coder switch after every change to ensure that the switch code has changed. If a real change is noted, the routine proceeds to determine the direction of the change. The frequency knob outputs a two-bit code with only one bit at a time changing as the control is rotated. The direction the knob is rotated is determined by the property of a gray code, generated by an exclusive-OR logical operation within the CPU. The previous state of one bit is compared with the current state of the other bit. Down (counterclockwise rotation) yields unequal inputs, while up (clockwise rotation) yields the opposite. The bit that indicates direction is inserted as the MSB for the frequency coder byte. This byte is then loaded into the output stack. The subroutine then returns to the main scan routine.

Output Subroutine

After each scan, the CPU checks its output register to see if any information needs to be output. If it needs to be output, the output subroutine is called up; if not, another scan is started. The output subroutine checks a number of things before it outputs any information to the output regis-

ter. It first determines if the CPU is on its first or initial scan after a reset. The first scan will contain more than one closure. All of these closures must be output before it continues. On all scans that follow, the routine looks for more than one closure by checking the number of entries into the output stack. If more than one closure has been entered, the output routine aborts. This eliminates outputting phantom key closures.

The routine is now ready to output information. It pulls a key address from the output stack and looks up the code from a look-up table in ROM. This key code is loaded into the data port or output buffer. The appropriate port P24 or P25 (pins 35 & 36) is pulled low. The routine continuously reads the frequency coder and updates its memory while it is waiting for the master processor to read the data in the output buffer. Once the data has been read, P24 or P25 goes high and the subroutine starts to check the output stack for more key closures. When the output stack is empty, the first scan flag is rescinded and the CPU returns to its main scanning routine.

POWER SUPPLY

The Main Power Supply furnishes all the regulated voltages for the 494/494P, except the crt high-voltage supply. The high-efficiency design of the Main Power Supply reduces total weight and conserves energy. The power supply consists of the following: the line input circuit, which rectifies and filters the incoming line voltage; the inverter, which drives the primary of the power transformer; the rectifier-filter circuit, which rectifies and filters the secondary voltages; the voltage reference circuit, which furnishes a stable and precise reference for the regulators; and the regulator circuits, which control the voltage and current for the supplies that require precise regulation.

The Fan Driver board houses the Fan Driver circuit, which furnishes the appropriate drive current for the fan motor. It also contains the Over-Voltage Protection circuit, which shuts down the +5 V supply in case of over-voltage. Refer to Diagram 46.

Line Input Circuits

Power is applied through line filter FL301, line Fuse F301, and through FL302 (for additional normal mode/common mode EMI filtering) to POWER switch S300. The power is then sent through line selector connector J1091. The line filter prevents power-line interference from entering the power supply, and it also prevents internally-generated signals from radiating out the power cord.

Line selector switch S302 allows instrument operation from either a 115 V nominal or 230 V nominal line voltage source. With S302 is in the 115 V position, pins 1 and 2 of P1091 are connected to the input power, and rectifiers CR3096 and CR4094 operate in conjunction with energy storage filter capacitors C6101 and C6111 as a full-wave doubler; thus, the voltage across the two capacitors is the peak-to-peak value of the line voltage. With S302 in the 230 V position, pins 2 and 3 of P1091 are connected to the input power and CR3096, CR4095, CR3098, and CR4094

operate as a bridge rectifier. As a result, the output voltage applied to the inverter is about the same for 115 V or 230 V operation.

Thermistors RT2093 and RT2097 limit current surge at turn on. After the instrument warms up, the current demand drops. The increase in temperature decreases the resistance value of the thermistors so they have minimum affect on the circuit.

WARNING

Because C6011 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the POWER switch is turned off. A relaxation oscillator formed by C5113, R5111, and DS5112, indicates the presence of voltages in the circuit until the potential across the filter capacitors is below 80 V.

Thermal cutout switch S2103 opens if the interior of the instrument reaches 103°C to prevent overheating in case the cooling fan fails.

E1094 and E2095 are surge voltage protectors. When the line selector switch is in the 115 V position, only E1094 is connected across the line input. If a peak voltage surge in excess of 230 V occurs across the input, or if the instrument is accidentally connected to a 230 V source, E1094 will break down and demand enough current to open the line fuse. When the instrument is operated with the line selector at 230 V, E1094 and E2095 operate in series to protect the input against line surges of approximately 460 V peak.

The voltage for the line trigger is taken across CR3096. This 48 Hz to 440 Hz voltage drives optical isolator U5043.

The pulsating 5 V output is ac coupled, then sent both to the Sweep circuit to provide instrument triggering at the line frequencies and to the Z-Axis board for the Power-Fail Detector circuit.

Inverter Circuit

The inverter consists of a multivibrator that produces a rectangular shaped signal to drive the ramp generator and the inverter logic circuits. The ramp generator produces a low-level sawtooth ramp that is applied to the primary regulator circuit. The inverter logic circuits control the duty cycle of the inverter driver and the inverter output stage. The primary regulator circuit compares the +17 V supply output with a reference voltage, then gates the inverter logic circuits off and on to control the inverter duty cycle and the effective primary voltage. The inverter driver stage amplifies the signal from the inverter logic circuit and drives the output stage. The output stage consists of two power switching transistors that drive the primary of main power transformer T4071. The primary over-current sense and soft start circuits add protection.

Multivibrator. U6059, a low-power 555 timer, is a multivibrator that operates at approximately 66 kHz and 90% duty cycle. Oscillator frequency is adjusted by R6061. The output rectangular shaped signal is applied through R6052 to the primary of T6044 in the ramp generator and also directly to U6053, U6063A, U6063B, and U6069.

Ramp Generator. The ramp generator circuit is a gated sawtooth generator that consists of T6044, Q5023, Q6034, Q5032, and related components. The negative excursion of the rectangular shaped signal from U6059 is coupled across T6044 to force Q6034 into conduction. This forward-biases Q5032. Its collector moves toward +17 V to charge C5038 to this value. Q6034 loses drive (since the pulse coupled across T6044 has died away) and the two transistors cut off. Q5023 acts as a constant-current drain to linearly discharge C5038. This signal is coupled across divider R5036/R6032, then applied through C6039 to the input of comparator U6036, which is part of the primary regulator.

Primary Regulator. The primary regulator circuit consists of comparator U6036 and U6046, photocoupler U6043, and related components. The circuit varies the duty cycle of the driving signal for the inverter. The +17 V is divided by R6038 and R6037 to approximately +4.8 V and applied to the inverting input of U6036. The +5 V reference is applied through R6022 to the non-inverting input of U6036, where it is combined with the ramp signal from the ramp generator stage. The non-inverting input receives a sawtooth signal of approximately 500 mV peak-to-peak superimposed on a +5 Vdc level. This is compared with the +4.8 V on the other input, so the comparator switches with each sawtooth cycle. Note in Figure 7-34 that as the level at

pin 3 (which corresponds to the +17 V supply variations) rises and falls, the duty cycle of the output waveform varies accordingly.

The output signal of U6036 is applied to optical isolator U6043, which drives the input of U6069.

Inverter Logic. This stage consists of steering flip-flop U6063B and dual quad input NAND gate U6069. The flip-flop is connected so it toggles to enable first one gate then the other. The square-wave output from the multivibrator drives the clock input of U6063B. The signal also enables each gate to ready it for the other signals that arrive later. The output state of U6063 determines whether the upper or lower section of U6069 will be ready for the enabling signal. Assume that the Q output of U6063B is holding pin 2 of U6069 high. This means that the complement output of the latch is holding the opposite side of the gated pair disabled. When the output of U6043 moves high (U6043 controls the duty cycle of the inverter, the upper section of U6069 produces a low state. This causes current to flow through half the primary and Q6078 only. On the opposite cycle of the multivibrator signal, the latch is reset, so the lower half of U6069 is enabled and Q6077 is now in the conduction path.

Inverter Driver. The inverter driver consists of transistors Q6077 and Q6078, transformer T6081, and related components. This is a push-pull amplifier with diode protection in the collector circuits to prevent damage from voltage transients during operation. The drive signal is induced into the two secondary windings of T6081 and coupled to the output stage.

Output Stage. This circuit consists of transistors Q2071 and Q2061, series LC tank L1081/C1063, and transformer T4071. The output transistors are connected in a half-bridge configuration. The two transistors drive the series tank, which acts as an energy storage element and an averaging circuit. Output transformer T4071 is driven by the tank circuit, and it, in turn, drives the secondary circuits.

Primary regulation, as discussed previously, occurs when the duty cycle of the inverter driver main switching transistors is varied. Maximum duty cycle occurs at low input line (90 V) and fully loaded output. At maximum duty cycle, both transistors are off for only 10% of the period, or 1.5 μ s. This short interval allows any stored base charge to deplete, so there is no chance both transistors will conduct at the same time. Minimum duty cycle occurs at high input line (132 V) and minimum loaded output. At minimum duty cycle, each transistor is off for approximately 6 μ s, or 40% of the total period.

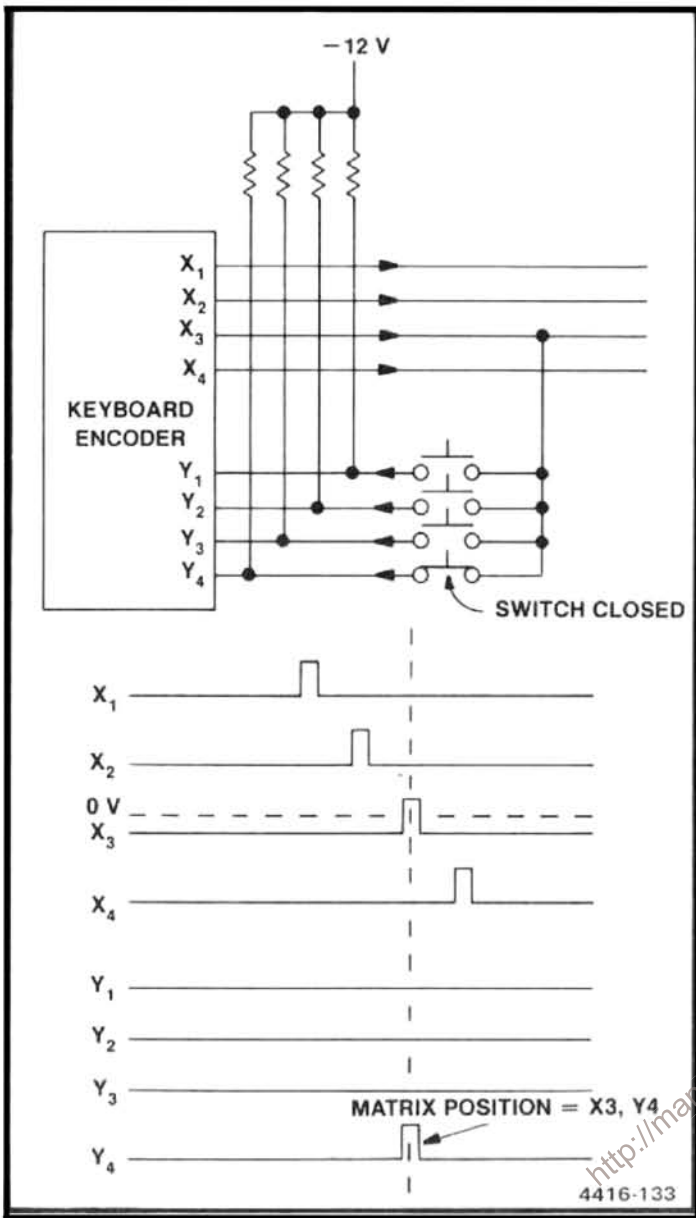


Figure 7-34. Primary regulator input/output waveform (stylized).

Soft Start and Primary Over-Current Circuits. The soft start circuit consists of U6053 and associated components. Soft start gradually increases the switching transistor's duty cycle at turn-on or after over-current shutdown to prevent excessive transistor current due to charging output capacitors. Refer to Figure 7-35 for timing waveforms.

The primary over-current circuit protects against secondary shorts that could destroy the switching transistors. T2080 senses the collector current in Q2071 and creates a voltage on pin 5 of U6046B. If the bias on pin 5 surpasses the 2.5 V reference on pin 6, at approximately 6 A through Q2071, the output of U6046B sets U6063A. U6063A is a D-type flip-flop used as a timer to shut down the inverter logic for approximately 1 sec and to reset the soft start circuit.

Rectifier-Filter Circuits (secondary section).

Transformer T4071 has three secondary windings. The first furnishes current to the +300 V and +100 V supplies; the second furnishes current to the -7 V, +7 V, and +9 V supplies; and the third furnishes current to the +17 V and -17 V supplies. The linear regulated supplies (+5 V reference, +5 V, -5 V, +15 V, and -15 V) derive their current from the rectifier-filter circuits.

The ac voltage from pins 7 and 8 of T4071 is applied to a bridge rectifier composed of CR3053, CR3056, CR3055, and CR3054. The output of this rectifier is filtered, then applied to the remainder of the instrument as the +100 V supply.

The +300 V supply is derived by stacking a 2X multiplier on the +100 V supply. CR3052, CR1042, CR1034, CR1022 and associated capacitors, compose this circuit.

The ac voltage from pins 9 and 10 supply current to full-wave rectifier CR4061/CR4062. The output is filtered and sent to the rest of the instrument as the +9 V supply. Two other taps off the same winding (pins 11 and 12) supply current to the bridge rectifier that consists of CR4063, CR4057, CR4053, and CR4065. The output divides across filter capacitors C3051 and C4051 to become the +7 V and -7 V supplies. The +7 V supply is only used on the Main Power Supply board; the -7 V supply is used by other circuits in the instrument.

The third winding of T4071 (pins 13, 14, and 15) furnishes current to full-wave bridge rectifier CR5052, CR5062, CR5065, and CR5055. The output is divided to become the +17 V and -17 V supplies. The -17 V supply is used only on the Main Power Supply board; the +17 V supply is used both on the Main Power Supply board and elsewhere in the instrument.

+5 V Voltage Reference Supply. The +17 V is divided down by a voltage divider to Zener diode VR6026. The 6.2 V from VR6026 is divided across R6029, R6028, and R6023. CR5031 provides a regulated source of bias to VR6026 after +15 V comes up. The +5 V REF adjustment, R6028, is set by monitoring the +15 V supply and setting it for a precise +15.00 V.

Regulator Circuits. The +15 V, -15 V, +5 V, and -5 V are regulated. Since all four regulators are basically the same, only the +5 V regulator is described. Significant differences are discussed following this description.

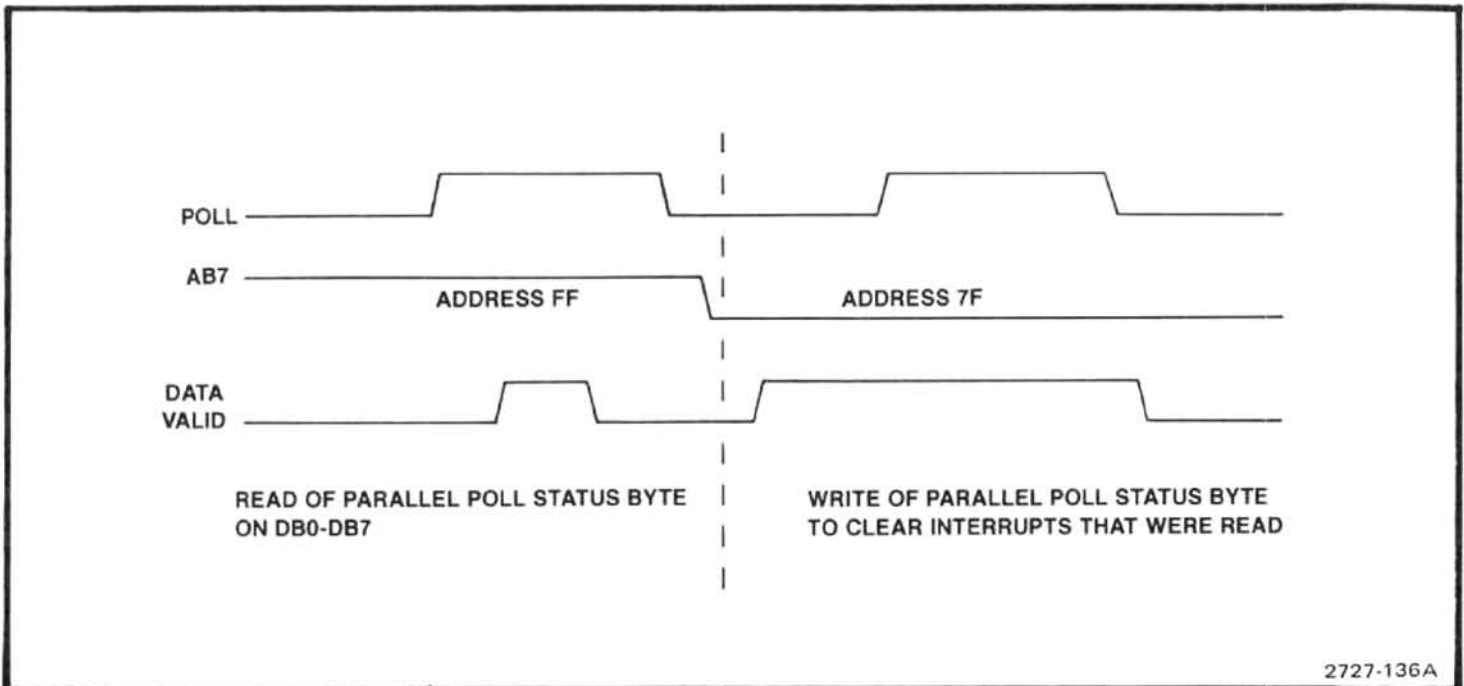


Figure 7-35. Timing waveform (stylized) for soft-start circuit.

U2037A, the voltage regulator part of the circuit, compares the $+5 V_{REF}$ and $+5 V$ SENSE voltages, amplifies the difference, and applies the change to driver transistor Q2023. The change is amplified by this stage and applied to the base of series-pass transistor Q2024 to change its conduction and correct for the original change to the $+5 V$. The $+5 V$ sense samples the $+5 V$ at a distribution point on the Mother board. This signal compensates for voltage (IR) losses to that point.

U2037B is the current limiter portion of the regulator. The amplifier detects the voltage differential across the current sensing resistor R2017, which is in series with the output load. When the overload threshold is reached, as set by R2017, R2039, R3032, and R3031. U2037B removes bias current from driver transistor Q2023 and Q2024. The negative bias on R3031 allows the limiter to remain active under short circuit conditions.

The $+15 V$ regulator is the same as the $+5 V$ regulator, except that the current limiter, U2037D supplies additional positive bias for Q2031 when it is not active. The $-15 V$ regulator is virtually identical to the $+5 V$ regulator. The $-5 V$ regulator differs from the others in that a driver stage is not required, so the preamplifiers drive series-pass transistor Q5013 directly.

$+5 V$ Over-Voltage Protection Circuit. Zener diode VR1015 and SCR Q1010 form the over-voltage protection

circuit. If the $+5 V$ supply passes $+6 V$, the potential on the gate of Q1010 biases it into conduction. This forces the $+5 V$ supply to ground; it remains at ground potential until the analyzer is de-energized and turned on again.

Fan Drive Circuit. The fan drive circuit provides a temperature-controlled current drive to the fan motor. The circuit produces a three-phase drive current of approximately 240 Hz operating frequency. The actual drive circuit operates as a ring counter.

Transistors Q1038 and Q1044 form a voltage regulator controlled by thermistor RT2045. The value of RT2045 varies inversely with the internal temperature of the analyzer. The thermistor and a companion resistor, R2042, fix the turn-on voltage at the emitter of Q1044 at approximately $-13 V$; the voltage goes more positive as the analyzer warms up. VR 2038 is connected with jumper P2043 when the rackmount fan is used to prevent the output voltage from going below approximately 9 V.

The ring counter consists of three stages: Q1025 and Q1020, with R1031/C1032 and R1027/C1018 as the frequency-determining components; Q2025 and Q1018, with R1033/C1033 and R2019/C1019 as the frequency-determining components; and Q2030 and Q2020, with R2014/C2012 and R2016/C2018 as the frequency-determining components. When the analyzer is energized, one of the three ring counter stages begins to conduct before the

others; owing to circuit imbalances. Assume that the upper stage (Q1025 and Q1020) begins to conduct first. The collector voltage of Q1025 is near -17 V, which fixes that point as the most negative in a ring consisting of R1032, R1029, R1028, R2036, R2034, and R1036. Since the emitter voltage of the three control transistors (Q1020, Q1018, and Q2020) is the same, the voltage division around the resistive ring is such that Q1018 and Q2020 remain cut off. When the capacitive charge that holds Q1020 in conduction bleeds off, the transistor cuts off and the next stage can begin to conduct. Operation of the other two stages is prevented until the RC combination discharges. The fan motor inductance works in conjunction with the RC components to regulate the switching of the stages.

This ring-counter action builds up slowly until the circuit produces a three-phase drive signal of approximately 240 Hz. The inductance of the motor coils round off the otherwise sharp corners of the drive signal, so the current waveform looks a great deal like the output of a half-wave rectifier at P2020 pins 1, 2, and 3. Each drive signal is approximately 120° apart, so as to drive the motor.

The rackmount/benchtop versions of the 494/494P require an external fan, B200. When this fan is installed, the internal fan, B100, is removed.

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OPTIONS

The following describes the various options that are available for the 494/494P. Information on or about some of these options may also be integrated within the appropriate sections of the manual(s). Options are factory installed and supplied, except as noted.

**Table 8-1
POWER CORD OPTIONS**

Option	Description	Tektronix Part No.
A1	Universal Euro, 220 V/50 Hz @ 16A	161-0132-00
A2	United Kingdom U.K., 240 V/50 Hz @ 13A	161-0133-00
A3	Australian, 240 V/50 Hz, @ 10A	161-0135-00
A4	North American, 240 V/60 Hz @ 12A	161-0134-00
A5	Swiss, 250 V/50 Hz @ 6A	161-0167-00

OPTION 08

Deletes external mixer capability. Standard accessories do not include the Diplexer. Frequency range is 10 kHz to 21 GHz.

OPTION 12

Contains dual language in firmware that provides English and German for display messages.

OPTION 13

Contains dual language in firmware that provides English and French for display messages.

OPTION 14

Contains dual language in firmware that provides English and Spanish for display messages.

OPTION 20

Includes General Purpose Waveguide Mixers; frequency range 12.5 to 40 GHz, as listed in Table 8-2.

Table 8-2
OPTION 20 (GENERAL PURPOSE WAVEGUIDE MIXERS) CHARACTERISTICS
TEKTRONIX PART NO. 016-0640-00

Frequency Range	Part No.	Sensitivity: Equivalent Input Noise @ 1 kHz Bandwidth (Typical)
12.4-18 GHz	119-0097-00	-75 dBm
18-26.5 GHz	119-0098-00	-70 dBm
26.5-40 GHz	119-0090-00	-60 dBm

OPTION 21

Includes High Performance Waveguide Mixers; frequency range 18-40 GHz as described in Table 8-3.

Table 8-3
OPTION 21 (WM 490-2) CHARACTERISTICS

Frequency Range	Nomenclature	Sensitivity: Equivalent Input Noise @ 1 kHz Bandwidth (maximum)	Frequency Response	Referenced to 100 MHz
18-26.5 GHz	WM 490K	-100 dBm	± 3.0 dB	± 6.0 dB
26.5-40 GHz	WM 490A	-95 dBm	± 3.0 dB	± 6.0 dB

Cable: SMA to SMA connector; 012-0649-00

OPTION 22

Includes High Performance Waveguide Mixers that cover the frequency range 18-60 GHz as listed in Table 8-4.

Table 8-4
OPTION 22 (WM 490-3) CHARACTERISTICS

Frequency Range	Nomenclature	Sensitivity: Equivalent Input Noise @ 1 kHz Bandwidth (maximum)	Frequency Response	Referenced to 100 MHz
18-26.5 GHz	WM 490K	-100 dBm	± 3.0 dB	± 6.0 dB
26.5-40 GHz	WM 490A	-95 dBm	± 3.0 dB	± 6.0 dB
40-60 GHz	WM 490U	-95 dBm	± 3.0 dB	± 6.0 dB

Cable: SMA to SMA male connectors, 012-0649-00

NOTE

These characteristics assume that the waveguide mixer is connected to a cw signal source and that the PEAKING control is adjusted for maximum signal amplitude. The signal must be stable (not frequency modulated more than the resolution bandwidth); otherwise, frequency response performance cannot be met.

OPTIONS 30 AND 31

Introduction

Option 30 is the rackmount version of the 494/494P Spectrum Analyzer. It is designed to mount in a standard 19-inch rack. A larger fan is installed to provide additional cooling. Option 31 is the Option 30 with added semi-rigid cables to provide access to all front-panel connections via the cabinet rear panel. Pull-out cards are not included with these options.

Electrical Characteristics

Electrical characteristics for the 494/494P are applicable for both options, except residual (FM'ing) response, and frequency response when Option 31 is included. If these instruments are subject to externally-induced vibrations from rack cooling fans or the surrounding equipment, they may show degradation of the FM'ing characteristic. Because of different rack configurations, this degradation cannot be specified. In a typical fan-cooled rack, degradation increases by a factor of two.

With Option 31, the frequency response and display flatness performance typically degrades up to 2 dB in the negative direction, above 3.0 GHz.

Environmental and Physical Characteristics

Option 30 and 31 instruments meet MIL T-28800C, type III, class 5, style F specifications. Some of the details are shown in Table 8-5.

The physical characteristics for Option 30 are listed in Table 8-6.

Table 8-5
ENVIRONMENTAL CHARACTERISTICS
OPTION 30 AND 31

Characteristic	Description	
Temperature and Humidity Operating	Temperature °C	Relative Humidity %
	0 to 25	95% +5, -0
	25 to 40	75% ± 5
	40 to 50	45% ± 5
Non-operating	-55 to 75	95% +5, -0
Altitude		
Operating	10,000 feet	
Non-operating	40,000 feet	
Vibration		
Operating	Method 514 Procedure X (modified MIL-STD-810C). The vibration limit is 1 G. Resonance searches along all three axes at 0.0065 inch; frequency varied from 10 to 55 Hz, 15 minutes per axis, plus dwell at resonant frequency of 33 Hz for 10 minutes per axis. Total vibration time is 75 minutes with the instrument secured to a rack during the test. The semi-rigid cables between the front-panel connectors and the front-grill connectors for Option 31 must be removed for this test.	
Shock	The semi-rigid cables between the front-panel connectors and the front-grill connectors for Option 31 must be removed for this test.	
Transit Drop	Not applicable	
Bench Handling	The semi-rigid cables between the front-panel connectors and the front-grill connectors for Option 31 must be removed for this test.	
Transportation		
Package Vibration	Meets National Safe Transit Association's pre-shipment test (project 1A-B-1) when correctly packaged. One hour of vibration at 1 G.	
Package Drop	Operable after a 24-inch drop on any corner or flat surface.	
Electromagnetic Interference (EMI)	Within the limits described in MIL-STD-461.	

Table 8-6
PHYSICAL CHARACTERISTICS
OPTION 30 AND 31

Characteristic	Description
Weight (standard accessories except manuals)	72 pounds maximum
Dimensions without side rails	8.75 × 16.89 × 25.00 inches (22.23 × 42.9 × 63.5 cm)

Safety Requirements

The safety requirements are the same as for the standard 494/494P.

Accessories

The standard accessories are the same as for the 494/494P with the addition of rack slides. An accessories drawer is provided for storage space in lieu of the front cover. Option 31 includes semi-rigid cabling to connect the front-panel connectors to the cabinet rear connectors; and a front-panel grill.

The optional accessories available for the 494/494P are listed in the current Tektronix catalog. These same optional accessories are available for Options 30 and 31, except that the transit case is not offered.

Installation Dimensions (Table 8-7)

The Options 30 and 31 require at least nine inches of vertical space to be mounted in a cabinet rack. At least 17.9 inches is required between the left and right front rails of the rack. This minimum width allows room on each side of the instrument for the slide-out tracks to operate freely, permitting smooth movement in and out of the rack. At least 25 inches are required behind the front rails for the instrument and necessary mounting hardware to fit with adequate air circulation and power cord availability.

Table 8-7
INSTALLATION DIMENSIONS
OPTION 30 AND 31

Characteristic	Dimension
Height	At least 9 inches
Width	17.9 inches minimum between left and right front rails of the rack
Depth	At least 25 inches behind the front rails

Slide-Out Tracks

WARNING

If the left and right slide-out tracks are reversed, the safety latch can be defeated, allowing the instrument to be pulled out of the rack. There are green labels on each track near the mounting flange that are stamped with LH or RH to indicate left hand and right hand, respectively. Be sure to mount the tracks on the correct sides, and only as directed in these instructions.

The slide-out tracks consist of a complete assembly for the left side of the instrument and one for the right side. Each assembly consists of three sections. See Figure 8-1. The stationary section of each assembly attaches to the front and rear rails of the cabinet rack. The chassis section is attached to the instrument at the factory. The intermediate section slides between the stationary and chassis sections and allows the instrument to be extended out of the track. When the instrument is shipped, the stationary and intermediate sections of the tracks are packaged as matched sets and should not be separated. When mounted in the cabinet rack, the automatic latch should be at the top of both assemblies.

Extra hardware is provided with the slide-out track assemblies. Since the hardware is intended to make the tracks compatible with a variety of cabinet racks and installation methods, not all of the hardware will be used for any installation procedure.

Installation Procedure

The following procedure describes how to mount the slide-out tracks to untapped rack rails, using the hardware provided. If the rack rails are tapped for 10-32 screws, the slide-out tracks can be mounted in front of the front rails and in back of the rear rack rails using pan head screws. The flat bar nuts are not needed.

1. Mount the stationary sections to the untapped front rack rails using either of the following methods.

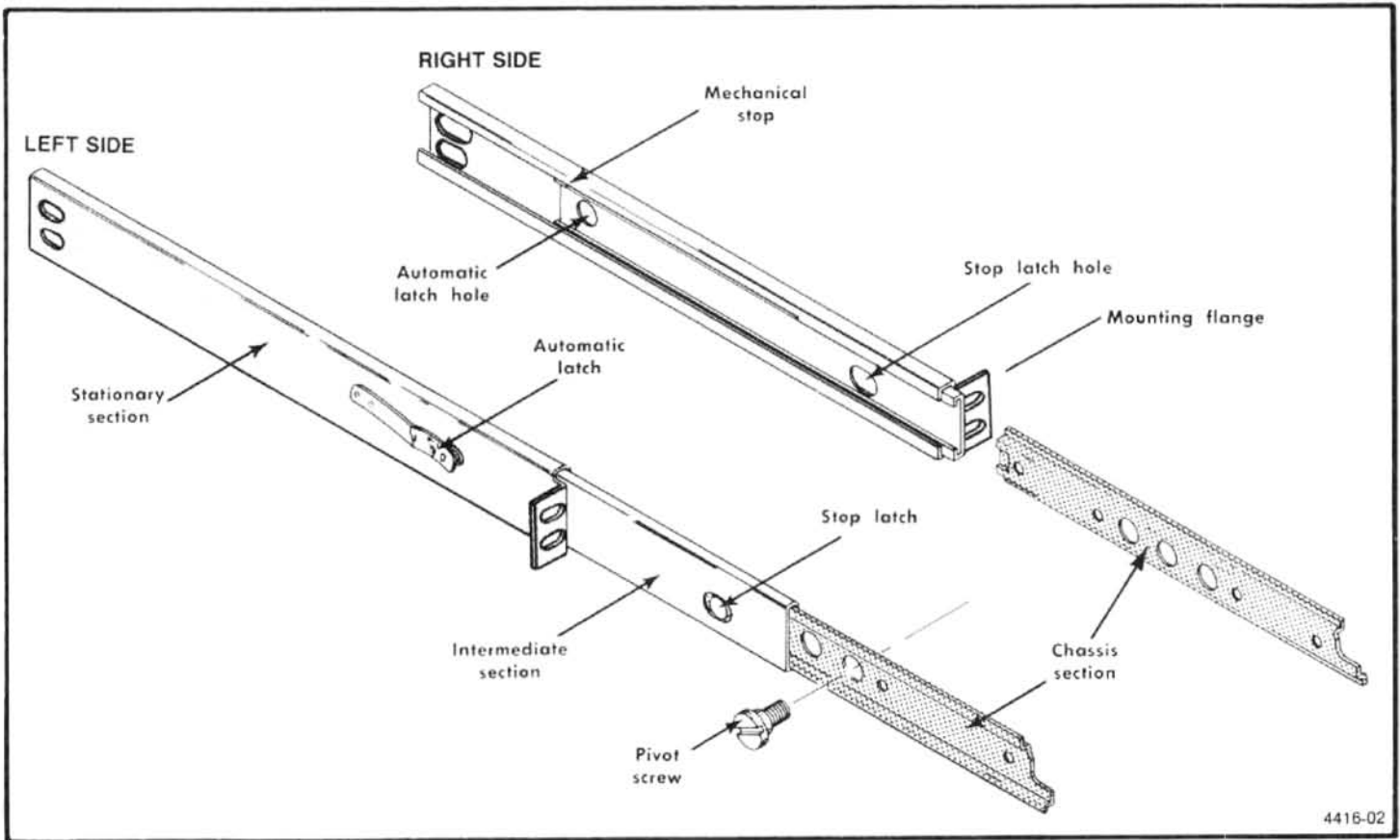


Figure 8-1. Slide-out track assemblies.

a. If the front rails are not countersunk, use the truss head screws and bar nuts, using Figure 8-2 as a guide.

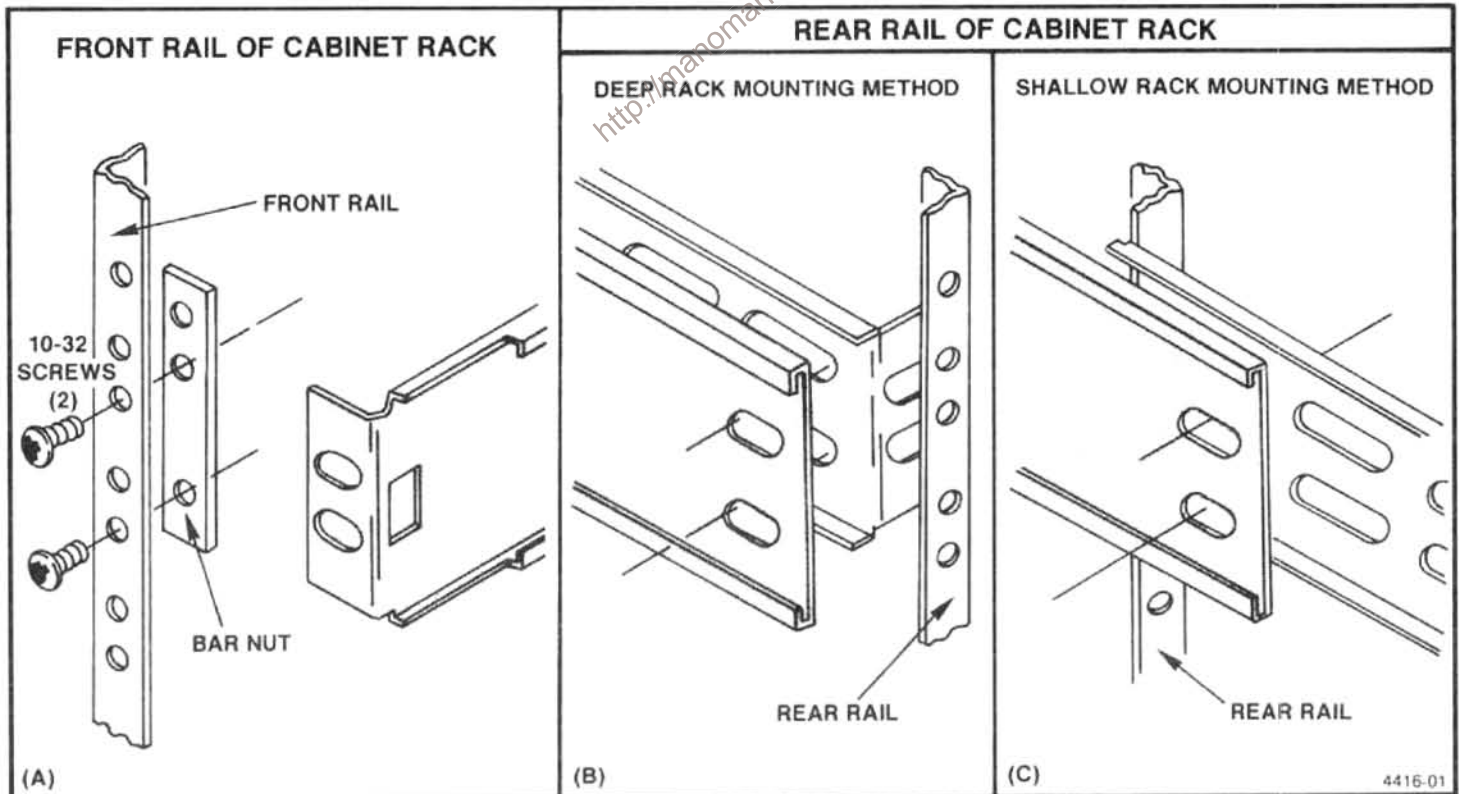


Figure 8-2. Installing the stationary sections (A) and alternative installation methods using rear-support brackets (B), (C).

b. If the front rails are countersunk, use the flat head screws and bar nuts.

- Refer to Figure 8-3 to insert the instrument into the rack. Do not connect the power cord or install the securing screws until all adjustments have been made.

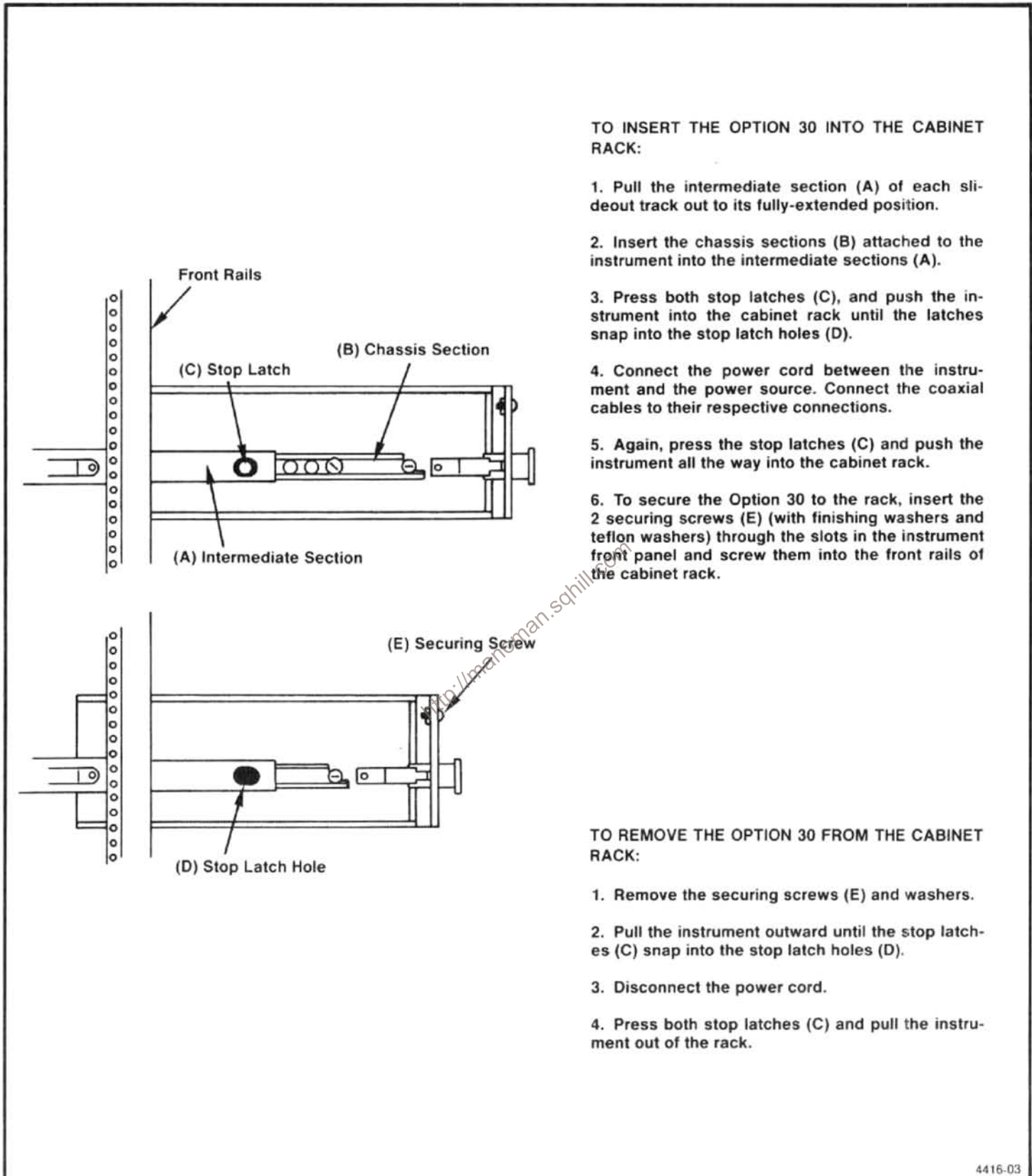


Figure 8-3. Installing and removing Option 30 from the cabinet rack.

3. Position the instrument so the pivot screws (widest part of instrument) are approximately even with the front rails, and adjust the alignment of the stationary sections according to the following procedure.
 - a. Position the instrument with the pivot screws approximately even with the front rails.
 - b. Loosen the mounting screws at the front of both stationary sections (left side shown).
 - c. Allow the tracks to seek their normal positions with the instrument centered in the rack.
 - d. Tighten the mounting screws.
 - e. Push the instrument all the way into the rack. If tracks do not slide smoothly, check for correct spacing between the rear supports.
 - f. Check the vertical positioning of the instrument front panel with respect to adjacent instruments or panels. If not correct, reposition as necessary.
4. When track operation is smooth, connect the power cord to the power source.
5. Push the instrument fully into the rack and latch.
6. The instruments are shipped with vinyl trim strips on the cabinet flange. These strips cover two holes in the flange that can be used to insert screws to secure the cabinet to the rack frame. If you need the instrument secured better than the latches on each side provide, cut out the vinyl cover around the hole with a sharp knife. Install the securing screws as shown in Figure 8-2C.

The slide-out tracks permit it to be extended out of the rack for access to the back connectors. Before attempting to operate the instrument in the extended position, be sure the power cord and any interconnecting cables are long enough for this purpose.

CAUTION

If the instrument is extended out of the rack and tipped up to gain access to the bottom or back panels of the instrument, it can swing past center and fall back into the rack unless it is held. Use care when doing this to avoid damaging the front panel or equipment that may be mounted above Options 30 or 31.

Alternate Installation Procedures

CAUTION

While the following methods provide satisfactory installation under normal conditions, they do not provide solid support for the rear of the instrument. If the instrument might be subjected to severe shock or vibration, consult your local Tektronix Field Engineer for information on a more substantial procedure.

An alternate procedure for securing Options 30 and 31 using rear-support brackets is shown in Figure 8-2. The rear support brackets that are supplied with the instrument are to be used in a rack with 15 to 26 inches of space between the front and rear rails. (If the depth of the rack is less than 22 inches, the instrument will stick out of the back of the rack.)

Mount the stationary sections to the untapped rear rails as shown in Figure 8-2B or 8-2C. Note that the rear mounting bracket can be installed either way so the slide-out tracks will fit a deep or shallow cabinet rack. Be sure that the stationary sections are aligned horizontally, i.e., level and parallel with each other.

If the rack does not have a rear rail, or if the distance between the front and rear rails is too great, the instrument may be installed without the use of the slide-out tracks. Fasten the instrument to the front rails of the rack with the securing screws, and provide a means of securing the rear of the instrument. This method should be used only if the instrument will not be subjected to shock or vibration and it is installed in a stationary location.

Slide-Out Track Lubrication

The special finish on the sliding surfaces of the tracks provides permanent lubrication. However, if the tracks do not slide smoothly even after proper adjustment, a thin coating of paraffin rubbed onto the sliding surfaces may improve operation.

Removing the Side, Top, and Bottom Panels

To remove the side, top, or bottom panels from the Option 30 or 31, follow the instructions in Figure 8-3 to remove the instrument from the rack. Then, perform the following procedure.

1. Use a Torx "T20" screwdriver to remove the fillister screws that hold the feet on the back four corners of Options 30 and 31.
2. On the cabinet side panels, remove the pivot screw for the side rail track assembly.
3. Slide the panel back and off the cabinet.
4. To remove the EMI strip, remove the back feet mounting plate and slide the strip out of its channel.

Replacement

To replace the side, top, and bottom panels, perform steps 3 through 1. Be sure to start the EMI strip under the panel before sliding the panel forward. If this is not done, the panel will catch the strip and bend the end. Use a pointed object, such as a screwdriver, to push the end of the EMI strip down while pushing the panel forward.

Installing Semi-Rigid Coaxial Cables (Option 31)

Perform the following steps to install the semi-rigid coaxial cables of Option 31. These cables permit rear-panel access to the instrument front-panel connectors.

1. Remove the instrument from the rack, and slide the bottom panel off according to the instructions on removing the panels.
2. Remove the horizontal support bar across the front section of the cabinet to gain access to the mounting nuts that hold the front panel grill in place. Remove the mounting nuts.

3. Install the SMA coaxial connectors in the Option 31 grill.
4. Remove the front-panel grill and install the Option 31 grill.
5. Position the cables with RF connectors in their appropriate back-panel access hole. Install the mounting nuts for each connector and secure.
6. Connect the semi-rigid cables to the SMA connectors mounted in the front-panel grill, and tighten to 8-10 inch-pounds.



Do not overtighten coaxial connectors beyond the recommended 8 to 10 inch-pounds torque. Use a second wrench to hold the connector or cable nut as the other nut is tightened.

7. Attach the cable clamps to hold the cables to the mounting posts on the bottom of the instrument housing.
8. Reinstall the horizontal support bar, and reinstall the bottom panel.
9. Reinstall the instrument in the rack and install the semi-rigid cables between the front-panel connectors and the connectors on the cabinet grill.
 - a. Ensure that the plugs and receptacles are clean and free of any foreign matter.
 - b. Insert the plug connectors fully into the receptacle. Since the cables are all approximately the same length, the cables for the 1st and 2nd LOs are labeled to avoid confusion. Do not force a cable in place if it does not fit easily.
 - c. Screw the mounting nut on finger tight to ensure it is not cross-threaded.
 - d. Use a 5/16 inch open-end wrench to tighten the nut to 8-10 inch-pounds torque.

Preparing the Instrument for Adjustment or Repair

The fan assembly must be removed before the instrument can be removed from the cabinet. After the instrument is removed from the cabinet, the fan must be reconnected before power can be applied to allow the instrument to be turned on. The following steps prepare the instrument for adjustment or repair.

1. If the Option 31 is installed in a rack with the semi-rigid cables to the back panel, disconnect the cables between the instrument front panel and the connectors on the front grill of the cabinet.
2. Disconnect all external connections to the instrument, including the power cord, and remove the instrument from the rack.
3. Place the instrument face-down on a bench.

4. Loosen the two fan assembly mounting screws and remove the fan assembly.
5. Use a 5/32-inch Allen wrench to loosen and remove the four screws that hold the instrument to the cabinet back panel and remove the instrument from the cabinet.
6. Carefully align the fan assembly power connector pins to the receptacle on the back panel of the instrument and reinstall the fan assembly. Reconnect the power cord.
7. The instrument is now ready for adjustment or repair.

OPTION 32

Introduction

Option 32 is the benchtop version of the 494/494P Spectrum Analyzer. The Option 32 configuration adds feet to the bottom of the instrument and also adds side panels with handles. A larger fan is installed to provide additional cooling. Pull-out cards are not included with this option.

Electrical, Environmental, and Physical Characteristics

The electrical characteristics for the 494/494P are applicable for Option 32.

Option 32 instruments meet MIL T-28800C, type III, class 5, style E specifications. Some of the details are shown in Table 8-8.

The physical characteristics for Option 32 are listed in Table 8-9.

Table 8-8
ENVIRONMENTAL CHARACTERISTICS
OPTION 32

Characteristic	Description	
Temperature and Humidity Operating	Temperature °C	Relative Humidity
	0 to 25	95% +5, -0
	25 to 40	75% ±5
	40 to 50	45% ±5
Non-operating	-55 to 75	95% +5, -0
Altitude		
Operating	10,000 feet	
Non-operating	40,000 feet	
Vibration		
Operating	Method 514 Procedure X (modified MIL-STD-810C). The vibration limit is 1 G. Resonance searches along all three axes at 0.0065 inch; frequency varied from 10 to 55 Hz, 15 minutes per axis, plus dwell at resonant frequency of 33 Hz for 10 minutes per axis. Total vibration time is 75 minutes with the instrument secured to a vibration platform during the test. The bail for tilting must be folded for this test.	
Shock	The bail for tilting must be folded for this test.	
Transit Drop	Not applicable	
Bench Handling	The bail for tilting must be folded for this test.	
Transportation		
Package Vibration	Meets National Safe Transit Association's pre-shipment test (project 1A-B-1) when correctly packaged. One hour of vibration at 1 G.	
Package Drop	Operable after a 24-inch drop on any corner or flat surface.	
Electromagnetic Interference (EMI)	Within the limits described in MIL-STD-461.	

Table 8-9
PHYSICAL CHARACTERISTICS
OPTION 32

Characteristic	Description
Weight (standard accessories except manuals)	70 pounds maximum
Dimensions	
with feet and handles	9.25 × 17.9 × 25.00 inches (23.5 × 45.47 × 63.5 cm)
without feet and handles	8.75 × 16.89 × 25.00 inches (22.23 × 42.90 × 63.5 cm)

Safety Requirements

The safety requirements are the same as for the standard 494/494P.

Accessories

The standard accessories are the same as for the 494/494P instrument. An accessories drawer is provided for storage space in lieu of the front cover. The optional accessories available for the 494/494P are listed in the current Tektronix catalog. These same optional accessories are available for Option 32, except that the transit case is not offered.

Removing the Instrument From the Cabinet

Before attempting any adjustment or repair, the Option 32 must be removed from its cabinet.

1. Place the instrument face-down on a bench.
2. Loosen the two fan assembly mounting screws and remove the fan assembly.
3. Use a 5/32 Allen wrench to loosen and remove the four screws that hold the instrument to the cabinet back panel.
4. Push or pull the instrument from the cabinet.
5. Carefully align the fan assembly power connector pins to the receptacle on the back panel of the instrument and reinstall the fan assembly. Reconnect the power cord.

Replacement

To replace the Option 32 in the cabinet, perform steps 4 through 1 of this procedure.

OPTION 41

Provides enhanced measurement capability for Digital Microwave Radio. These include: 1) A wider bandwidth preselector for better signal symmetry in the digital radio bands; 2) A narrow video filter (approximately 1/3000th of the resolution bandwidth) to improve amplitude variation analyses, at specific frequency spans that are unique to the digital radio measurements; 3) Improved frequency span/div accuracy at 5 MHz/DIV span, to make accurate signal band-width measurements.

OPTION 52

North American 220 V configuration with standard power cord. Fuses are replaced with 2A slow blow.

GLOSSARY

The following glossary is presented as an aid to better understand the terms as they are used in this document and with reference to spectrum analyzers.

GENERAL TERMS

Baseline Clipper (Intensifier). Increasing the brightness of the signal relative to the baseline portion of the display.

Center Frequency. That frequency which corresponds to the center of a frequency span, expressed in hertz.

Effective Frequency Range. That range of frequency over which the instrument performance is specified. The lower and upper limits are expressed in hertz.

Envelope Display. The display produced on a spectrum analyzer when the resolution bandwidth is greater than the spacing of the individual frequency components.

dBc. dB below carrier level.

Frequency Band. A part of effective frequency range over which the frequency can be adjusted, expressed in hertz.

Full Span (Maximum Span). A mode of operation in which the spectrum analyzer scans an entire frequency band.

Zero Span. A mode of operation in which the frequency span is reduced to zero.

Line Display. The display produced on a spectrum analyzer when the resolution bandwidth is less than the spacing of the signal amplitudes of the individual frequency components.

Line Spectrum. A spectrum composed of signal amplitudes of the discrete frequency components.

Maximum Safe Input Power

WITHOUT DAMAGE. The maximum power applied at the input which will not cause degradation of the instrument characteristics.

WITH DAMAGE. The minimum power applied at the input which will damage the instrument.

Intermodulation Spurious Response (Intermodulation Distortion). An unwanted spectrum analyzer response resulting from the mixing of the n th order frequencies, due to non-linear elements of the spectrum analyzer, the resultant unwanted response being displayed.

Pulse Stretcher. A pulse shaper that produces an output pulse, whose duration is greater than that of the input pulse, and whose amplitude is proportional to that of the peak amplitude of the input pulse.

Spectrum Analyzer. An apparatus which is generally used to display the power distribution of an incoming signal as a function of frequency.

NOTE

It is useful in analyzing the characteristics of repetitive electrical waveforms in general, since repetitively sweeping through the frequency range of interest will display all components of the signal.

Signal Identifier. A means to identify the spectrum of the input signal when spurious responses are possible.

Scanning Velocity. Frequency span divided by sweep time and expressed in hertz per second.

Video Filter. A post detection lowpass filter.

TERMS RELATED TO FREQUENCY

Display Frequency. The input frequency as indicated by the spectrum analyzer and expressed in hertz.

Frequency Span (Dispersion). The magnitude of the frequency band displayed, expressed in hertz or hertz per division.

Frequency Linearity Error. The error of the relationship between the frequency of the input signal and the frequency displayed (expressed as a ratio).

Frequency Drift. Gradual shift or change in displayed frequency over the specified time due to internal changes in the spectrum analyzer, and expressed in hertz per second, where other conditions remain constant.

Residual FM (Incidental FM). Short term displayed frequency instability or jitter due to instability in the spectrum analyzer local oscillators, given in terms of peak-to-peak frequency deviation and expressed in hertz or percent of the displayed frequency.

Impulse Bandwidth. The displayed spectral level of an applied pulse divided by its spectral voltage density level assumed to be flat within the pass-band.

Static (Amplifier) Resolution Bandwidth. The specified bandwidth of the spectrum analyzer's response to a cw signal, if sweep time is kept substantially long.

NOTE

This bandwidth is the frequency separation of two down points, usually 6 dB, on the response curve, if it is measured either by manual scan (true static method) or by using a very low speed sweep (quasi-static method).

Shape Factor (Skirt Selectivity). The ratio of the frequency separation of the two (60 dB/6 dB) down points on the response curve to the static resolution bandwidth.

Zero Pip (Response). An output indication which corresponds to zero input frequency.

TERMS RELATED TO AMPLITUDE

Deflection Coefficient. The ratio of the input signal magnitude to the resultant output indication.

NOTE

The ratio may be expressed in terms of volts (rms) per division, decibels per division, watts per division, or any other specified factor.

Display Reference Level. A designated vertical position representing a specified input level.

NOTE

The level may be expressed in decibels (e.g., 1 mW), volts, or any other units.

Sensitivity. Measure of a spectrum analyzer's ability to display minimum level signals, at a given IF bandwidth, display mode, and any other influencing factors, and expressed in decibels (e.g., 1 mW).

Equivalent Input Noise Sensitivity. The average level of a spectrum analyzer's internally generated noise referenced to the input.

Display Flatness. The unwanted variation of the displayed amplitude over a specified frequency span, expressed in decibels.

Relative Display Flatness. The display flatness measured relative to the display amplitude at a fixed frequency within the frequency span, expressed in decibels.

NOTE

Display flatness is closely related to frequency response. The main difference is that the spectrum display is not recentered.

Frequency Response. The unwanted variation of the displayed amplitude over a specified center frequency range, measured at the center frequency, expressed in decibels.

Display Law. The mathematical law that defines the input-output function of the instrument.

NOTE

The following cases apply:

- 1. Linear—A display in which the scale divisions are a linear function of the input signal voltage;*
- 2. Square law (power)—A display in which the scale divisions are a linear function of the input signal power;*
- 3. Logarithmic—A display in which the scale divisions are a logarithmic function of the input signal voltage.*

Dynamic Range. The maximum ratio of the levels of two signals simultaneously present at the input which can be measured to a specified accuracy.

Display Dynamic Range. The maximum ratio of the levels of two non-harmonically related sinusoidal signals each

of which can be simultaneously measured on the screen to a specified accuracy.

Gain Compression. Maximum input level where the scale linearity error is below that specified.

Spurious Response. A response of a spectrum analyzer wherein the displayed frequency does not conform to the input frequency.

Hum Sidebands. Undesired responses created within the spectrum analyzer, appearing on the display, that are separated from the desired response by the fundamental or harmonic of the power line frequency.

Noise Sidebands. Undesired response caused by noise internal to the spectrum analyzer appearing on the display around a desired response.

Residual Response. A spurious response in the absence of an input signal. (Noise and zero pip are excluded.)

Input Impedance. The impedance at the desired input terminal.

NOTE

Usually expressed in terms of vswr, return loss, or other related terms for low impedance devices and resistance-capacitance parameters for high impedance devices.

TERMS RELATED TO DIGITAL STORAGE FOR SPECTRUM ANALYZERS

Digitally Stored Display. A display method whereby the displayed function is held in a digital memory. The display is generated by reading the data out of memory.

Digitally Averaged Display. A display of the average value of digitized data computed by combining serial samples in a defined manner.

Multiple Display Memory. A digitally stored display having multiple memory sections which can be displayed separately or simultaneously.

Clear (Erase). Presets memory to a prescribed state, usually that denoting zero.

Save. A function which inhibits storage update, saving existing data in a section of a multiple memory (e.g., Save A).

View (Display). Enables viewing of contents of the chosen memory section (e.g., "View A" displays the contents of memory A; "View B" displays the contents of memory B).

Max Hold (Peak Mode). Digitally stored display mode which, at each frequency address, compares the incoming signal level to the stored level and retains the greater. In this mode, the display indicates the peak level at each frequency after several successive sweeps.

Scan Address. A number representing each horizontal data position increment on a directed beam type display. An address in a memory is associated with each scan address.

Volatile/Non-volatile Storage. A volatile storage system is one where any total loss of power to the system will result in a loss of the stored information.

<http://manoman.sghill.com>

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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TEKTRONIX MANUALS CHANGE INFORMATION

Date: 11-14-83
Product: 494/494P Serv. Vol. 1 Manual Part No.: 070-4416-00
Change Ref. C1/11B3 Rev. #2 Product Group: 26

DESCRIPTION

Revised 12-20-83
Revised 5-16-84

TEXT CHANGES

MAINTENANCE Section, page 6-73, preceding the Theory of Operation;
ADD the following:

FIRMWARE OPERATING NOTES

The following exceptions apply to 494P instruments with firmware
version 2.2.

Using the Tektronix 4662 Option 31 Plotter

The 4662 Option 31 Plotter does not respond to the first "move" command
that immediately follows a "pen selection" or "pen change" command,
consequently the pen starts to draw from its "home" position instead
of the selected position. This can be averted by using either a
one-pen (one-color) plot or by manually selecting the second pen.
The following procedure describes how to make a two-color plot.

1. Switch the GRAT ILLUM on, READOUT and Digital Storage off.
2. Manually select a pen, then plot the graticule.
3. Switch the GRAT ILLUM off, READOUT and Digital Storage on.
4. Manually select the second pen, then plot the stored display
and crt readout.

Auto Peaking Function with External Mixers

With instruments that have version 2.2 the Auto Peak function
does not always set the bias for external mixers to the correct peak
value. To ensure maximum peaking, use the PEAK/AVERAGE control or
use a "peak" command with specific numeric arguments.

TEKTRONIX MANUAL CHANGE NOTICE

Date: 7-31-84
Product: 494/494P Ser. 1 Manual Part No.: 070-4416-00
Change Ref: C2/884 Product Group: 26

DESCRIPTION

TEXT CHANGES

REPLACE step c. of the procedure to check the Reference Oscillator Accuracy on page 4-13 with the following:

c. If the Reference Oscillator needs adjustment, unscrew the protective screw on the Oscillator. Turn the oscillator frequency adjustment carefully and slowly with a small screwdriver or adjustment tool to 100 MHz, +/- 10 Hz on the counter. Replace the protective screw. Disconnect the counter from the CAL OUT connector.

NOTE

If the Reference Oscillator has not been powered up for a long period of time, additional warm-up time may be needed before the final frequency adjustment is made.

<http://manoman.sghill.com>

TEKTRONIX MANUAL CHANGE NOTICE

Date: 11-16-84
Product: 494/494P Ser. 1 Manual Part No.: 070-4416-00
Change Ref: C3/1184 Product Group: 26

DESCRIPTION

TEXT CHANGES

REMOVE the last two paragraphs from the right-hand column of Page 6-30.

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DESCRIPTION	Product Group 26
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Page 8-13, after Option 41 , ADD:

OPTION 42

In Option 42 instruments the MARKER/VIDEO input port on the rear panel is replaced with an 110 MHz IF output port. It provides a signal with a bandwidth greater than 5 MHz, which makes the spectrum analyzer suitable for broadband swept-receiver applications.

ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
110 MHz center frequency	108.5 MHz-111.5 MHz	
3 dB bandwidth	>5 MHz	
bandpass ripple	</=0.5 dB	
symmetry about 110 MHz	+/-1.0 MHz	
power output with -30 dB input and signal at full screen (band 1)	</= 0 dBm	nominal output impedance 50 ohm
(band 5)	>/= -40 dBm	in MIN DISTORTION mode only
		1 dB compression of output >/= 0 dBm

Page 4-3, ADD to Equipment Required for the Performance Check:

Tracking Generator with logic cable	Frequency Range 100 kHz to 1.8 GHz	TEKTRONIX TR502 (used to check Option 42)
2 RF Cable Assemblies		Tektronix Part No 012-0649-00

Page 4-4, ADD to Equipment Required for the Adjustment Procedure:

50 Ohm Termination		011-0049-01
3 Bnc-SMB Flexible Cables		

DESCRIPTION

Page 4-45, ADD after the 494P GPIB Verification Program:

32. For Option 42 instruments. Check Power Output at the 110 MHz OUT Connector on Band 1 (≤ 0 dBm)

- a. Using the flatness data for the instrument being tested, find the signal with the highest amplitude.
- b. Connect a signal generator to the frequency determined in step a and power level to -30 dBm.
- c. Set the 494/494P Option 42 REFERENCE LEVEL to -30 dBm and RF ATTENUATION to 0 dB.
- d. Keeping the signal centered with the CENTER FREQUENCY control, switch the FREQUENCY SPAN/DIV to 0 (the crt FREQ SPAN/DIV will indicate 10 ms).
- e. Adjust the CENTER FREQUENCY control of the 494 Option 42 to center the signal displayed on the 7L14.
- f. Check that the 110 MHz IF OUT output power is ≤ 0 dBm.

33. For Option 42 instruments. Check Power Output at the 110 MHz OUT Connector on Band 5 (≥ -40 dBm)

- a. Using the flatness data for the instrument being tested, find the signal with the lowest amplitude on Band 5.
- b. Connect a signal generator capable of the frequency determined in step a to the 494 Option 42 RF INPUT.
- c. Set the signal generator to the frequency determined in step a and the power level to -30 dBm.
- d. Set the 494 Option 42 REFERENCE LEVEL to -30 dBm and RF ATTENUATION to 0 dB.
- e. Keeping the signal centered with the CENTER FREQUENCY control, switch the FREQ SPAN/DIV to 0 (the crt Freq Span/Div will indicate 10 ms).
- f. Adjust the CENTER FREQUENCY control of the 494 Option 42 to center the signal displayed on the 7L14.
- g. Check that the 110 MHz IF OUT output power is ≥ -40 dBm

DESCRIPTION

34. For Option 42 instruments. Check Bandwidth (>5 MHz), Center Frequency (109.5 MHz–111.5 MHz), Bandpass ripple (≤ 0.5 dB), and Symmetry about 110 MHz (± 1.0 MHz)

a. Connect the test equipment as shown in Fig. 4-24A.

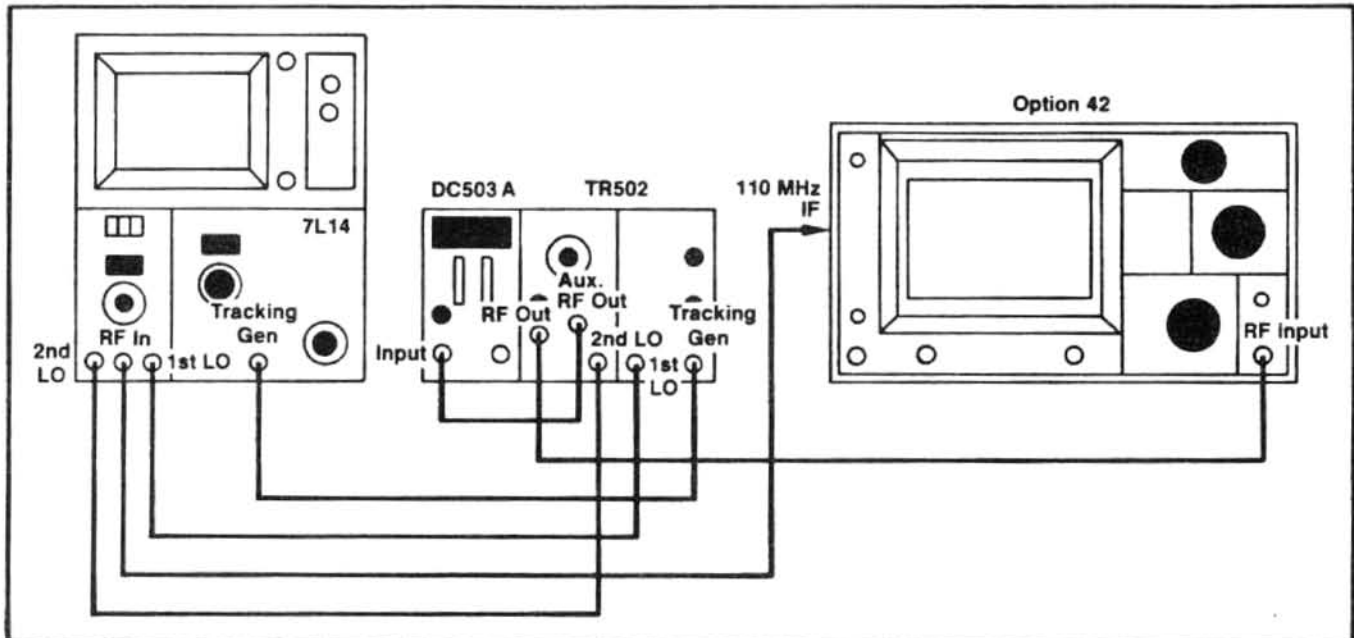


Fig. 4-24A

b. Set the instrument front-panel controls as follows:

TR502	Output level -dBm	30
	Var dB	0
	Dot intensity	off
7L14	Center frequency	0110
	Freq span/div	1 MHz
	Hz Resolution	3 MHz
	Reference level	0 dBm
	Reference level mode	2 dB/Div
	Digital storage	off
	Time/Div	manual
	Triggering	
	Source	free run
	Mode	norm
	Video filter	on
DC510	Function	Frequency A
	Auto Trig	on
	Channel A	
	Attn	X1
	Coupl	dc
	Term	50 Ohm

DESCRIPTION

494/494P Option 42

REFERENCE LEVEL	-30 dBm
CENTER FREQUENCY	110 MHz
FREQUENCY SPAN/DIV	1 MHz
Hz RESOLUTION	1 MHz
VERTICAL DISPLAY	2 dB/DIV
MIN RF ATTEN	0 dB

- c. Set the 7L14 Time/Div to Mnl and adjust the dot to center screen with the Manual Scan control.
- d. Adjust the 7L14 Center Frequency control for an indication of 110.0 on the Frequency Counter.
- e. While keeping the signal centered with the CENTER FREQUENCY control, set the 494 Option 42 FREQUENCY SPAN/DIV control to 0 (the Frequency Span/Div on the crt will indicate 10 ms).
- f. Set the 7L14 Time/Div for a calibrated display and adjust the Reference Level and TR502 Var dB for full screen signal.
- g. Switch the TR502 Dot Intensity to "on", and adjust the 7L14 Center Frequency for an indication of 110.0 on the Frequency Counter.
- h. Check the bandwidth at a point 3 dB (1.5 divisions) from the peak of the signal to be ≥ 5 MHz.
- i. Check that any ripple present on the waveform is ≤ 0.5 dB (≤ 0.25 divisions).
- j. Check that the waveform symmetry is ± 1.0 MHz (± 1.0 division) by assuring that the 3dB and 6dB points on the waveform are equidistant from center screen. (The peak of the signal may not be at center of the screen).

This concludes the Performance Check part of the Calibration Procedure.

DESCRIPTION

Page 5-35. ADD after the adjustment for Phaselock Calibration:

14. For Option 42 instruments. Adjustment of Option 42 Module. This adjustment need only be done after the circuit board in the module has been replaced.

a. Connect the test equipment as shown in Fig. 5-35.

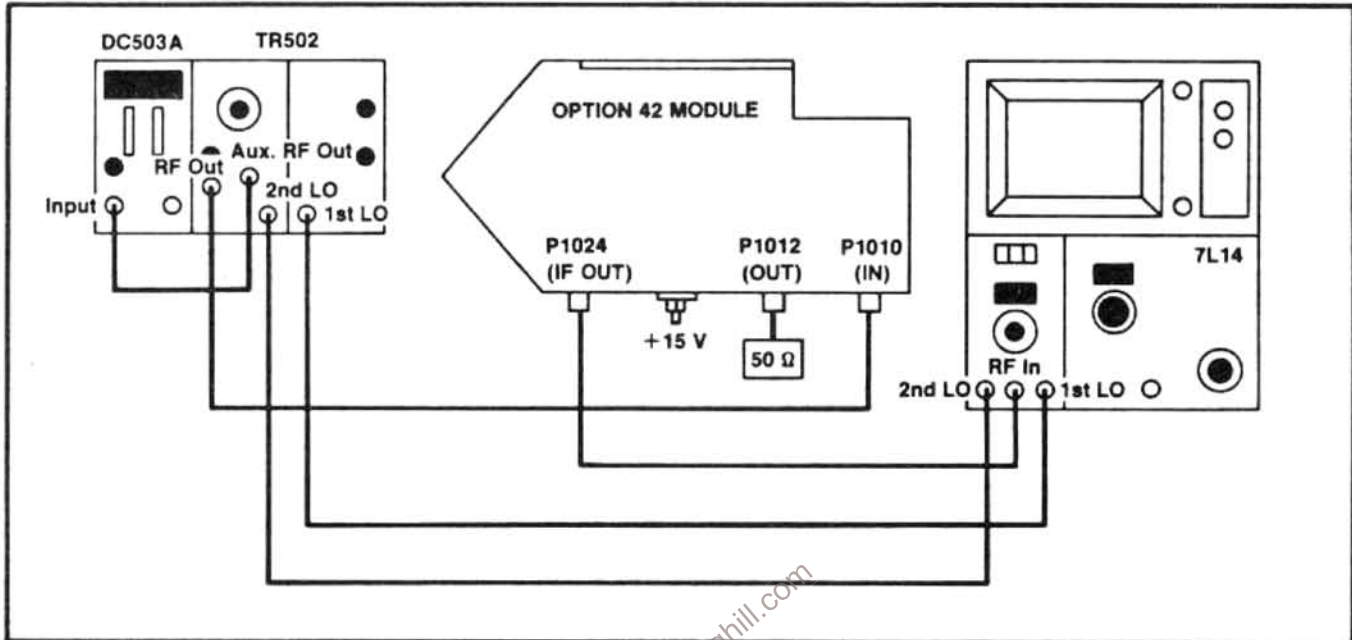


Fig. 5-35

b. Set the instrument front-panel controls as follows:

TR502	Output level -dBm	25
	Var dB	0
7L14	Center frequency	0110
	Freq span/div	2 MHz
	Hz Resolution	3 MHz
	Vertical display	2 dB
	Reference Level	0
	Display A and B	off
DC510	Ch A	
	Term	50 ohm
	Slope	+
	Atten	X1
	Coupl	dc
	Frequency A	
	Autotrig	

c. Set the 7L14 Time/Div to Manual, and adjust the crt beam (dot) to center screen.

DESCRIPTION

- d. The DC503A readout should indicate approximately 110.000 MHz. Adjust Level as necessary, and adjust the 7L14 Center Frequency for an indication 110.0 MHz.
- e. Set the 7L14 Time/Div to calibrated display.
- f. Adjust variable capacitors C1016, C1020 and C1024 for maximum amplitude symmetry and bandpass (3dB and 6dB points).
 1. Adjust the bandwidth symmetry +/- 0.5 divisions (+/- 0.5 MHz) at the 3 dB and 6 dB points.

NOTE

Check that points 3 dB (1.5 divisions) and 6 dB (3 divisions) down from the top of the signal are equidistant (+/- 0.5 divisions) from center screen.

2. Check that bandwidth at the 3 dB point is 7.5 MHz, +/- 1.5 MHz.
3. Check that any ripple present on the waveform is <= 0.2 div (0.4 dB).

NOTE

A slight change in display may be observed when the cover is reinstalled on the module.

- g. Check the Coupled Forward Gain (IF OUT port - P1024)
 1. Set the 7L14 Spectrum Analyzer Reference Level to 0 dBm.
 2. Check that the display on the 7L14 is between 4 and 7 divisions in amplitude (-5 dBm, +/-3 dBm).

h. Check the Input Compression.

1. Set the TR503 Output Level and 494 REFERENCE LEVEL in one dB increments, to higher power level (-24 dbm, -23 dBm etc.)
2. Continue changing the power level until the signal displayed by the 7L14 amplitude decreases (compresses 1 dB) 0.5 division.
3. Check that the signal displayed on the 7L14 indicates >= 0 dBm.

i. Check Forward Gain

1. Return the TR502 Output Level to -25 and remove the connection to the module IF OUT.

DESCRIPTION

2. Connect a 50 ohm termination to the IF DUT (P1024) connector.
3. Connect the DUT (P1012) connector to the 7L14 RF Input with a 50 ohm cable.
4. Adjust the 7L14 Reference Level until the displayed signal is near full screen (8 divisions).
5. Check that the signal displayed on the 7L14 indicates -20dBm to -23 dBm (-21.5 dBm +/-1.5 dBm).

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TEKTRONIX MANUAL CHANGE NOTICE

Date: 2-25-85
Product: 494 Ser.1
Change Ref: C102/285

Manual Part No.: 070-4416-00
Product Group: 26

DESCRIPTION

TEXT CHANGES

ADD on Page 6-29, REPLACING ASSEMBLIES AND SUBASSEMBLIES in the Maintenance Section, after the procedure on Removing or Replacing Semi-rigid Coaxial Cables:

Replacing the Dual Diode Assembly in the 1st Converter

The diode subassembly, which houses the Schottky mixer diodes, is held in place by four 0-80 screws. An 8-32 threaded hole is provided to facilitate insertion and removal of the subassembly. There are three contact points located on the substrate side of the subassembly. Use care when mounting and orienting these contacts with the mating contacts in the mixer assembly, to ensure proper fit and function. Insertion and removal of the subassembly more than twice is not recommended due to the gold ribbon attach technique used in fabrication.

A tuning screw, mounted through the top of the diode assembly, and adjacent to the 8-32 screw, is adjusted to null a start spur on band 1 as described in the Adjustment Procedure section. Although pre-calibrated, care should be taken to not force the tuning screw after it bottoms out on the surface of the quartz-suspended substrate.

The diode subassembly is packaged in a static-free package. Keep the diode subassembly in this package until ready to install. The following procedure should be used when replacing the subassembly.

CAUTION

The diodes are beam-lead devices mounted on a quartz-suspended substrate; these diodes are extremely static sensitive. Refer to the Caution note on static that precedes this section. Do not expose the diode assembly to any RF field.

1. Loosen and disconnect the three coaxial cable connections to the 1st Converter assembly, then remove the two mounting screws and remove the assembly from the 494/494P.

2. Remove the four 0-80 screws that hold the diode subassembly in the 1st Converter and insert a 8-32 screw into the threaded hole provided in the center of the diode assembly.

3. Lift the diode assembly out of the mixer assembly by means of the 8-32 screw, then remove the screw.

4. Open the diode package, grasp the diode assembly by its side with tweezers and place it on a static-free surface. Grasp the side of the assembly with the fingers to avoid contact with the diodes, and insert the 8-32 screw.

5. Orient the diode assembly so the three contact tips are aligned with their respective contacts in the mixer; then using the index fingers of both hands so equal pressure is applied, press the sub-assembly into place.

6. Insert the four mounting screws, tighten, then replace and tighten the three coaxial connectors to 8 inch lbs. Remount the 1st Converter assembly by installing the two mounting screws that hold the assembly to the RF deck of the 494/494P.

7. A procedure to adjust the First Converter Bias and Start Spur Amplitude is provided in the Maintenance Adjustments section.

NOTE

After replacement of the A12A1 Dual Diode Assembly in First Converter 119-1017-01, the 494/494P Spectrum Analyzer may not meet the flatness specification.

After replacement of the A12A1 Dual Diode Assembly in First Converter 119-1017-00, the 494/494P Spectrum Analyzer may not meet the flatness or the start spur specification.

ADD on Page 6-49, after Troubleshooting Aids for the 2182 MHz Phase-locked 2nd LO Assembly:

First Converter Bias and Start Spur Amplitude

NOTE

After replacement of the A12A1 Dual Diode Assembly in First Converter 119-1017-01, the 494/494P Spectrum Analyzer may not meet the flatness specification.

After replacement of the A12A1 Dual Diode Assembly in First Converter 119-1017-00, the 494/494P Spectrum Analyzer may not meet the flatness or the start spur specification.

Table 6-7A

EQUIPMENT REQUIRED FOR ADJUSTING FIRST CONVERTER BIAS
AND START SPUR AMPLITUDE

Test Equipment	Characteristics	Recommended Type
Digital Multimeter	$</=10$ uV to $>/=350$ Vdc	TEKTRONIX DM502A and TM 500-Series Power Module
Sinewave Generator	2.0 MHz, 0 dBm +10 dBm to -100 dBm	TEKTRONIX SG503
Power Meter	must measure 0 dBm	Hewlett-Packard 435B
Power Sensor	must measure 0 dBm @2 MHz	Hewlett-Packard 8482A
Attenuator (13 dB)		TEKTRONIX 2701
Coaxial Cable (50 ohm)		Tektronix Part No. 175-2765-00
Coaxial Cable (50 ohm)		Tektronix Part No. 175-2337-00
Coaxial Cable (50 ohm)		Tektronix Part No. 175-3310-00

1. Preparation

a. Remove the First Converter assembly from the spectrum analyzer, and connect the cables as shown in Fig.6-26A.

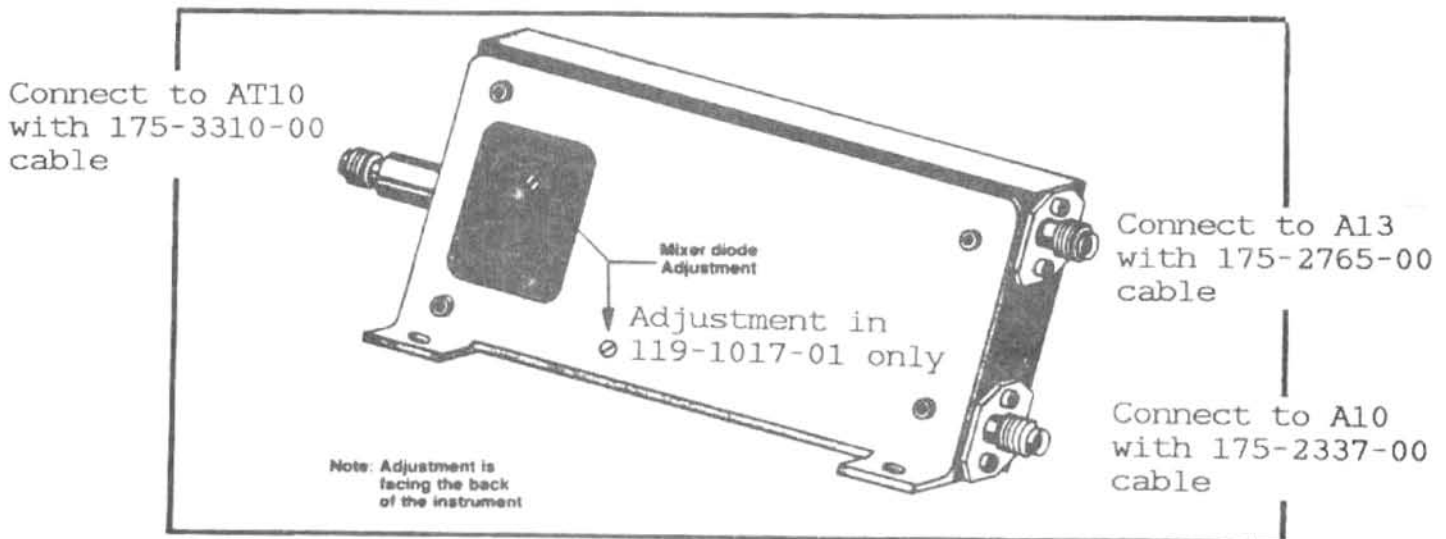


Fig.6-26A First Converter test equipment setup.

b. Set the spectrum analyzer front-panel controls as follows:

TIME/DIV	AUTO
REFERENCE LEVEL	-30 dBm
FREQUENCY RANGE ▲	5.4-18 GHz (band 4)
FREQ SPAN/DIV	MAX
DIGITAL STORAGE	
DISPLAY A	off
DISPLAY B	off
MIN RF ATTEN	0
PEAK/AVERAGE	clockwise

c. Set the DM502 controls as follows:

Range Switch	20 DC Volts
DB pushbutton	out
Int pushbutton	out

d. Connect the DM502 red test lead to TP1011 on the 1st LO Driver board, and the black test lead to the instrument chassis, see Fig.6-26B.

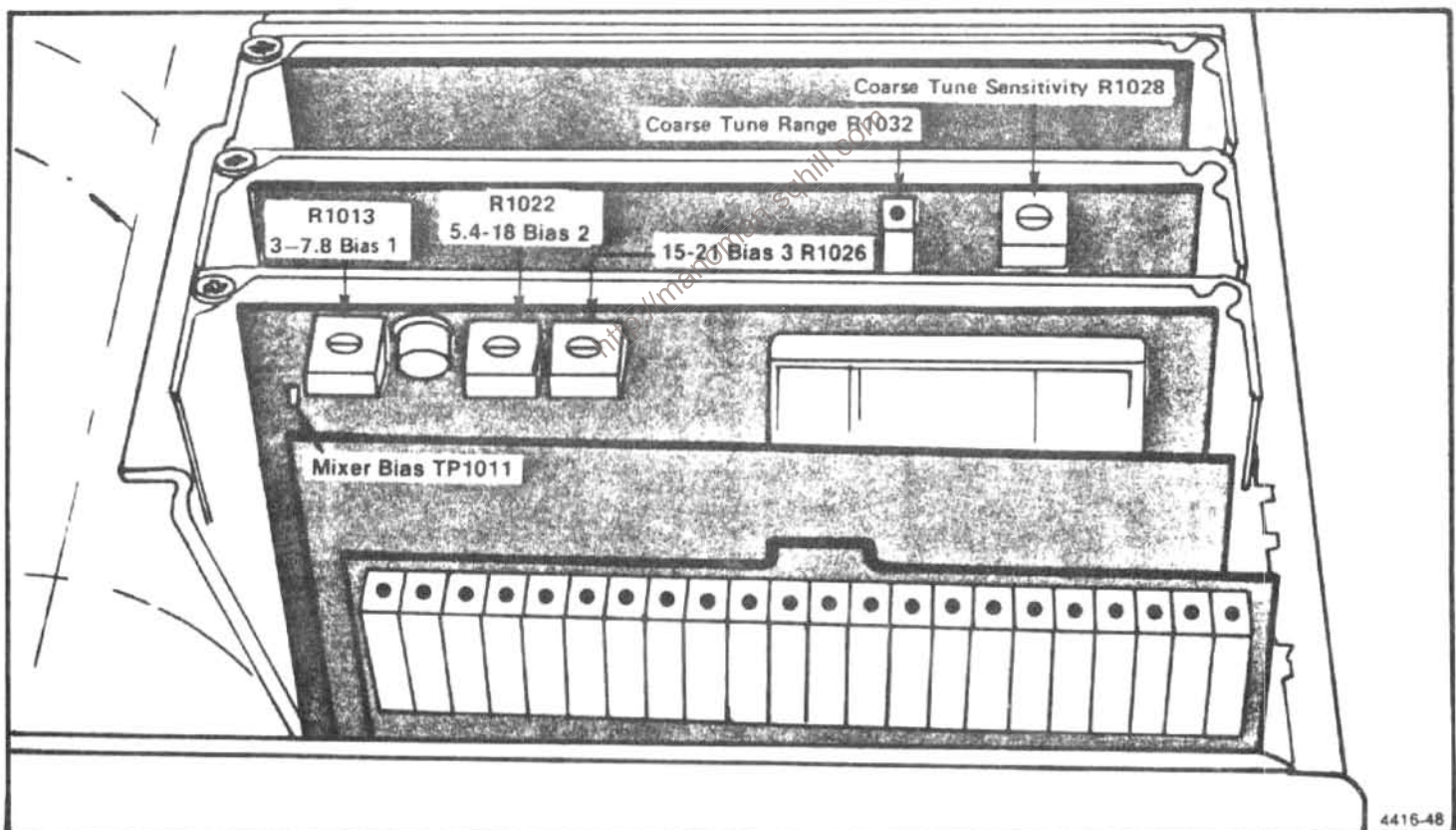


Fig.6-26B Adjustments and test points on the 1st LO Driver board.

2. Bias Adjustment

a. Adjust R1022 (see Fig.6-26B) for a reading of -0.25 on the DM502.

b. Push FREQUENCY RANGE ▲ to band 5 (15-21 GHz), and adjust R1026 (see Fig.6-26B) for a reading of -0.25 on the DM502.

3. Start Spurious Amplitude and Band 1 Bias Adjustment.

a. Push FREQUENCY RANGE ▼ to band 1 (0-4.2 GHz), and adjust the CENTER FREQUENCY to 0 MHz.

b. Connect a 50 ohm cable from the SG503 Output to the 2701 Port 1/Input, and connect a second 50 ohm cable to the Power Sensor.

NOTE

Calibrate the Power Meter before making measurements.

c. Set front-panel controls as follows:

- 2701 0 0, DC
- SG503
 - Frequency Range 1-2.5
 - Frequency Variable for an indication of 2.00 MHz on the readout
 - Amplitude Multiplier x1
 - Output Amplitude counterclockwise
- Power Meter
 - Line on
 - Range 0 (on the dBm scale)

d. Adjust the SG503 Output Amp control for an indication of 0 on the Power Meter dBm scale.

e. Disconnect the Power Meter from the 50 ohm cable and connect the 50 ohm cable from the 2701 Port 2/Output connector to the 494 RF INPUT connector.

f. While keeping the 2 MHz signal centered with the CENTER FREQUENCY control, set the 494 FREQUENCY SPAN/DIV to 200 kHz.

g. Set the front-panel controls as follows:

2701 13 dB
494
RESOLUTION BANDWIDTH 100 kHz
VIDEO FILTER (WIDE) on

h. Measure and record for reference the bandwidth of the 2 MHz signal at a point 6 divisions down from the top graticule line.

i. Adjust R1013 on the 1st LO Driver board for approximately -1.0 V at TP1011.

NOTE

During the following procedure, do not allow this voltage to go more positive than 0.1 V.

j. Bring the Start Spur signal to center screen with the CENTER FREQUENCY control. Frequency readout will indicate 0.00 MHz.

NOTE

For the least overall signal variations with frequency (flatness), the adjustments on the 1st Converter must be made in conjunction with R1013 (bias for bands 1, 2, and 3).

k. Alternately adjust R1013 and the adjustments on the 1st Converter (see Fig.4-23A) until the bandwidth, at the 6 dB point, matches the bandwidth of the previously displayed 2 MHz signal.

NOTE

It will be necessary to alternate between the above adjustments to decrease the amplitude of the start spur. While this is being done, assure that the voltage at TP1011 does not exceed +1.0 V.

It will not be possible to null the start spur to a point where the top of the signal will be on screen. To assure that the signal meets the specification (-13 dBm), the bandwidth is matched to the bandwidth of the previously displayed 2 MHz signal. Do not adjust the start spur lower than -13 dBm.

l. Remove all test leads from the test setup.